

Memory Interfacing and I/O interfacing:

The Memory Interfacing in 8085 is used to access memory quite frequently to read instruction codes and data stored in memory. This read/write operations are monitored by control signals. The microprocessor activates these signals when it wants to read from and write into memory.

Memory is an integral part of a microprocessor system, and in this section, we will discuss how to interface a memory device with the microprocessor. The Memory Interfacing in 8085 is used to access memory quite frequently to read instruction codes and data stored in memory. This read/write operations are monitored by control signals. The microprocessor activates these signals when it wants to read from and write into memory. In the last section we have already seen the memory read and memory write machine cycles, and status of the RD, WR and IO/M status signals for read/write operation. In the following section we will see memory structure and its requirements, concepts in Memory Interfacing in 8085 and interfacing examples.

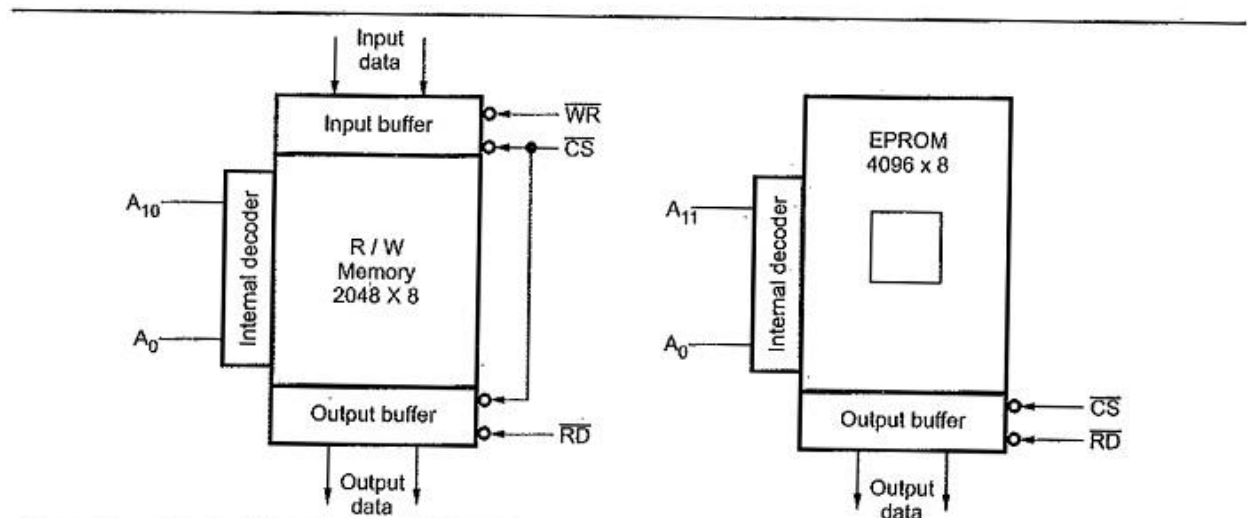


Fig. 4.13 (a) Logic diagram for RAM Fig. 4.13 (b) Logic diagram for EPROM

Basic Concepts in Memory Interfacing:

For Memory Interfacing in 8085, following important points are to be kept in mind.

1. Microprocessor 8085 can access 64Kbytes memory since address bus is 16-bit. But it is not always necessary to use full 64Kbytes address space. The total memory size depends upon the application.
2. Generally EPROM (or EPROMs) is used as a program memory and RAM (or RAMs) as a data memory. When both, EPROM and RAM are used, the total address space 64Kbytes is shared by them.
3. The capacity of program memory and data memory depends on the application.
4. It is not always necessary to select 1 EPROM and 1 RAM. We can have multiple EPROMs and multiple RAMs as per the requirement of application.
5. We can place EPROM/RAM anywhere in full 64 Kbytes address space. But program memory (EPROM) should be located from address 0000H since reset address of 8085 microprocessor is 0000H.
6. It is not always necessary to locate EPROM and RAM in consecutive memory For example : If the mapping of EPROM is from 0000H to 0FFFH, it is not must to locate RAM from 1000H. We can locate it anywhere between 1000H and FFFFH. Where to locate memory component totally depends on the application.

The memory interfacing requires to :

- **Select the chip**
- **Identify the register**
- **Enable the appropriate buffer.**

Microprocessor system includes memory devices and I/O devices. It is important to note that microprocessor can communicate (read/write) with only one device at a time, since the data, address and control buses are common for all the devices. In order to communicate with memory or I/O devices, it is necessary to decode the address from the microprocessor. Due to this each device (memory or I/O) can be accessed independently. The following section describes common address decoding techniques.

Address Decoding Techniques :

- **Absolute decoding/Full Decoding**

- **Linear decoding/Partial Decoding**

Absolute decoding:

In absolute decoding technique, all the higher address lines are decoded to select the memory chip, and the memory chip is selected only for the specified logic levels on these high-order address lines; no other logic levels can select the chip. Fig. 4.14 shows the Memory Interfacing in 8085 with absolute decoding. This addressing technique is normally used in large memory systems.

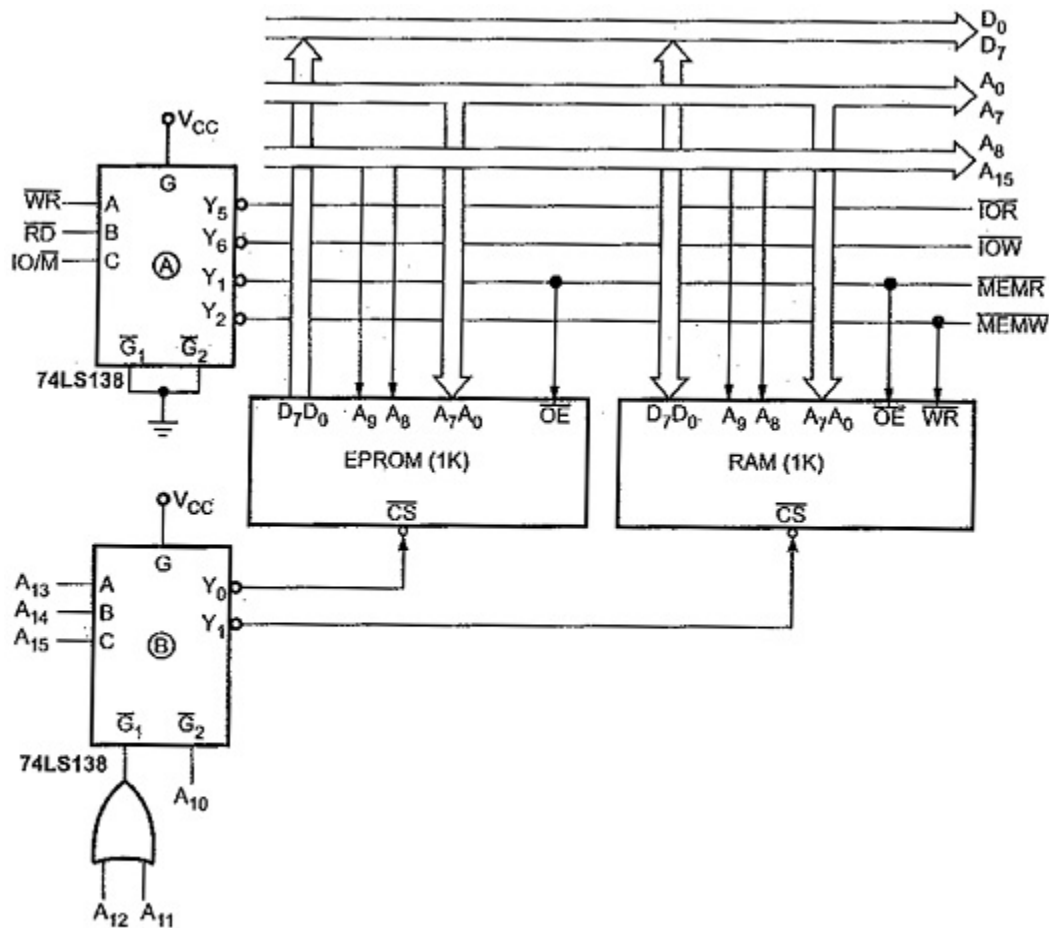


Fig. 4.14 Absolute decoding technique

Linear decoding:

In small systems, hardware for the decoding logic can be eliminated by using individual high-order address lines to select memory chips. This is referred to as linear decoding. Fig. 4.15 shows the addressing of RAM with linear

decoding technique. This technique is also called **partial decoding**. It reduces the cost of decoding circuit, but it has a drawback of multiple addresses (shadow addresses).

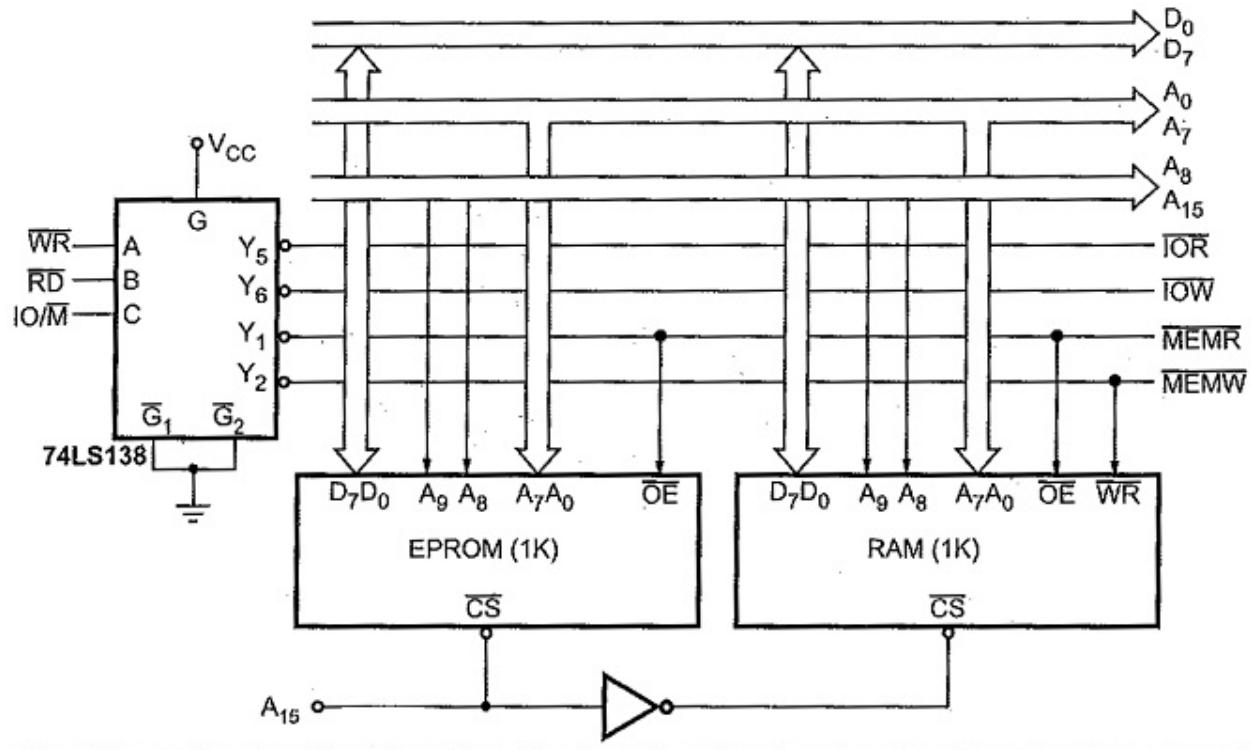


Fig. 4.15 Linear decoding

Wait State Generator:

We have seen that wait states can be introduced in the machine cycles using READY signal to interface slower memory devices. In this section we are going to see the circuits for wait state generator and applications of those circuits to interface slower memories.

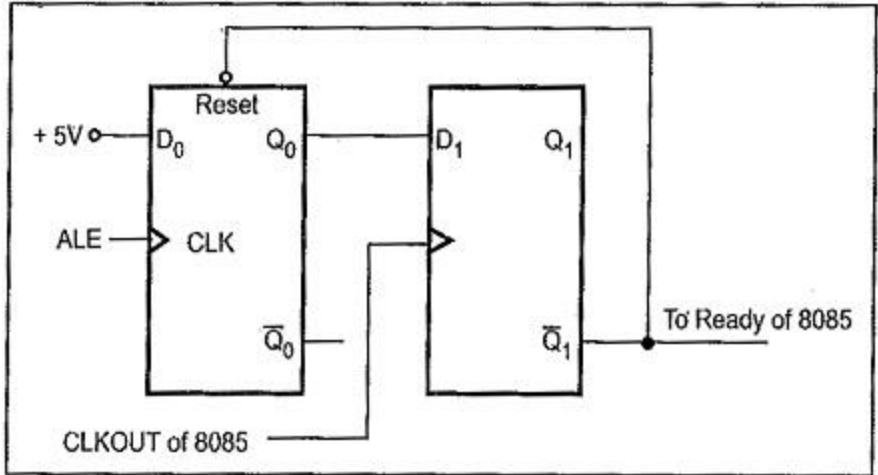


Fig. 4.22 Wait state generator

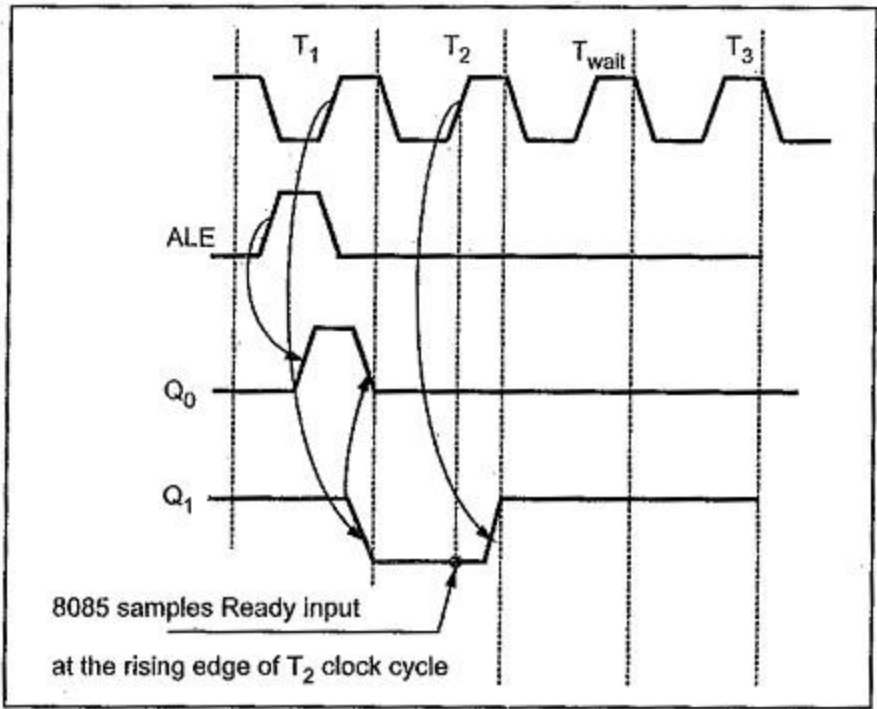


Fig. 4.23 Timing waveforms for wait state generator circuit

This circuit can be modified to introduce wait states for a particular machine cycle. The modified circuit of wait state generator is shown in Fig. 4.24. The modified circuit will generate a single WAIT state for any machine cycle for which the WAIT output of the machine cycle select circuit is logic 0.

The Fig. 4.22 shows the circuit for wait state generator. This circuit generates single wait state in every machine cycle. The circuit operation is given below.

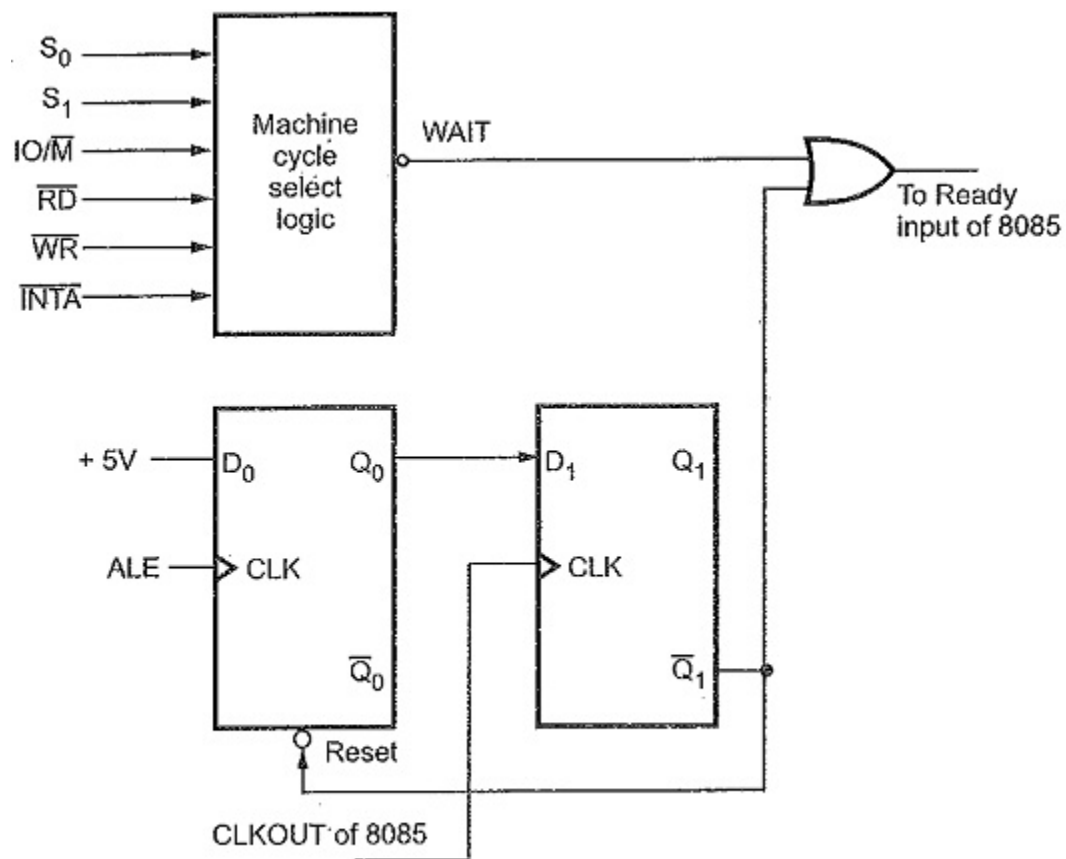


Fig. 4.24 Modified Wait State Generator Circuit

