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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECT221 – MICROPROCESSORS AND MICROCONTROLLERS

II YEAR - IV SEM

UNIT 3– 8051 MICROCONTROLLER

Arithmetic Instruction of 8051

ADC	add with 32-bit values and carry	Rd=Rn+N+carry
ADD	add two 32-bit values	Rd=Rn+N
RSB	reverse subtract of two 32-bit values	Rd=N-Rn
RSC	reverse subtract with carry of two 32-bit values	Rd=N-Rn-!(Carry flag)
SBC	subtract with carry of two 32-bit values	Rd=Rn-N-!(Carry flag)
SUB	subtract two 322-bit values	Rd=Rn-N

N is the result of the shift operation.

Logical Instruction

Logical instructions perform bitwise logical operations on the two source registers.

Syntax: <instruction>{<cond>} {S} Rd, Rn, N

AND	logical bitwise AND of two 32-bit values	Rd = Rn & N
ORR	logical bitwise OR of two 32-bit values	Rd = Rn | N
EOR	logical exclusive OR of two 32-bit values	Rd = Rn ^ N
BIC	logical bit clear (AND NOT)	Rd = Rn &~ N

Multiply Instruction

The multiply instructions multiply the contents of a pair of registers depending upon the instruction, and accumulate the result along with another register. The long multiplies accumulate onto a pair of registers representing a 64-bit value. The final result is placed on a destination register or pair of registers.

Syntax – MLA{<cond>}{S} Rd, Rm, Rs, Rn

MUL{<cond>}{S} Rd, Rm, Rs

MLA	Multiply and accumulate	Rd = (Rm * Rs) + Rn
MUL	multiply	Rd = Rm * Rs

Syntax – <instruction>{<cond>}{S} RdLo, RdHi, Rm, Rs

SMLAL	signed multiply accumulate long	[RdHi, RdLo] = [RdHi, RdLo] + (Rm * Rs)
SMULL	signed multiply long	[RdHi, RdLo] = Rm * Rs
UMLAL	unsigned multiply accumulate long	[RdHi, RdLo] = [RdHi, RdLo] + (Rm * Rs)
UMULL	unsigned multiply long	[RdHi, RdLo] = Rm * Rs

Comparison Instruction

These instructions are used to compare or test a register with a 32-bit value. They update the cpsr flag bits according to the result, but do not affect other registers. After the bits have been set, the information can then be used to change program flow by using conditional execution.

Syntax – <instruction>{<cond>} Rn, N

CMN	compare negated	flags set as a result of Rn + N
CMP	compare	flags set as a result of Rn – N
TEQ	test for quality of two 32 – bit values	flags set as a result of Rn ∧ N
TST	test bits of a 32-bit value	flags set as a result of Rn & N

N is the result of the shifter operation.

References

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