



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB211 – MICROCONTROLLER PROGRAMMING & INTERFACING

II YEAR IV SEM

UNIT II – PIC TIMER, SERIAL PORT AND INTERRUPT

TOPIC 5 – Basics of Serial Communication



Digital Communication



- Digital communication can be considered as the communication happening between two (or more) devices in terms of bits.
- This transferring of data, either wirelessly or through wires, can be either one bit at a time or the entire data (depending on the size of the processor inside i.e., 8 bit, 16 bit etc.) at once.
- Based on this, we can have the following classification namely, **Serial Communication** and **Parallel Communication**.

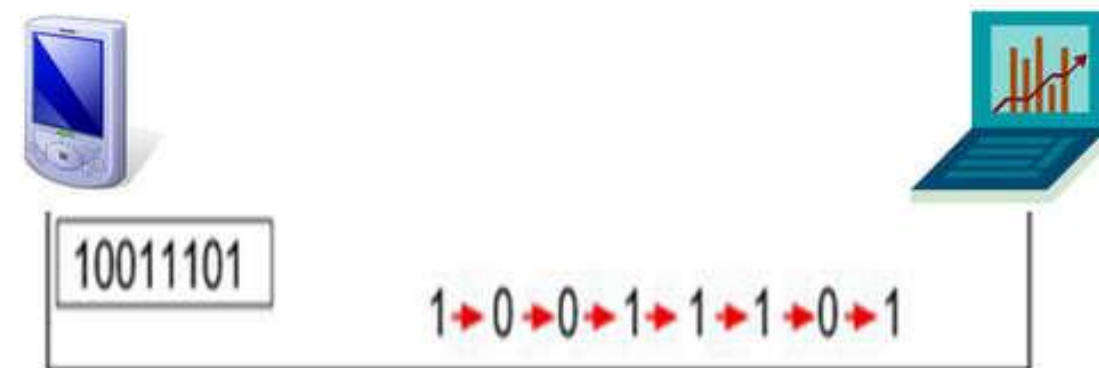


Types of communication



Serial Communication

- Serial Communication implies transferring of data bit by bit, sequentially.
- This is the most common form of communication used in the digital world. Contrary to the parallel communication, serial communication needs only one line for the data transfer.
- Thereby, the cost for the communication line as well as the space required is reduced.



MicrocontrollerBoard.com

Transmitting the word 10011101 using serial communication.

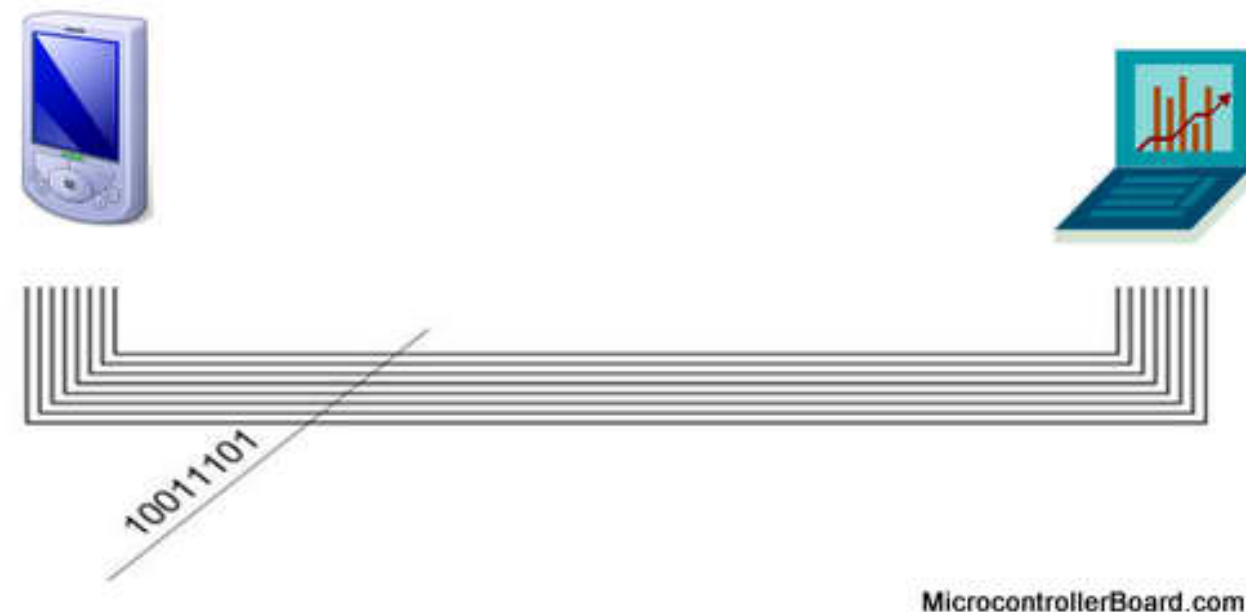


Types of communication



Parallel Communication

- Parallel communication implies transferring of the bits in a parallel fashion at a time. This communication comes for rescue when speed rather than space is the main objective.
- The transfer of data is at high speed owing to the fact that no bus buffer is present.



Transmitting the word 10011101 using parallel communication.



Synchronous & Asynchronous Communication



When using the synchronous communication – the information is transmitted from the transmitter to the receiver:

- in sequence
- bit after bit
- with fixed baud rate
- and the clock frequency is transmitted along with the bits



Synchronous & Asynchronous Communication



- When using the asynchronous communication - the transmitter and the receiver refraining to transmit long sequences of bits because **there isn't a full synchronization between the transmitter**, that sends the data, and the receiver, that receives the data.
- In this case, the information is divided into frames, in the size of byte.
- Each one of the frame has:
- “Start” bit marks the beginning of a new frame.
- “Stop” bit marks the end of the frame.



PIC –Serial Communication

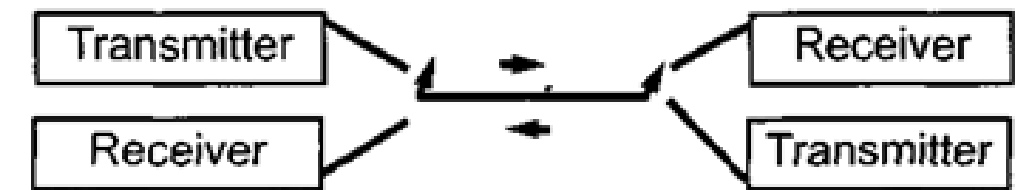
The TMR0 module is an 8-bit timer/counter with the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Simplex



Half Duplex



Full Duplex

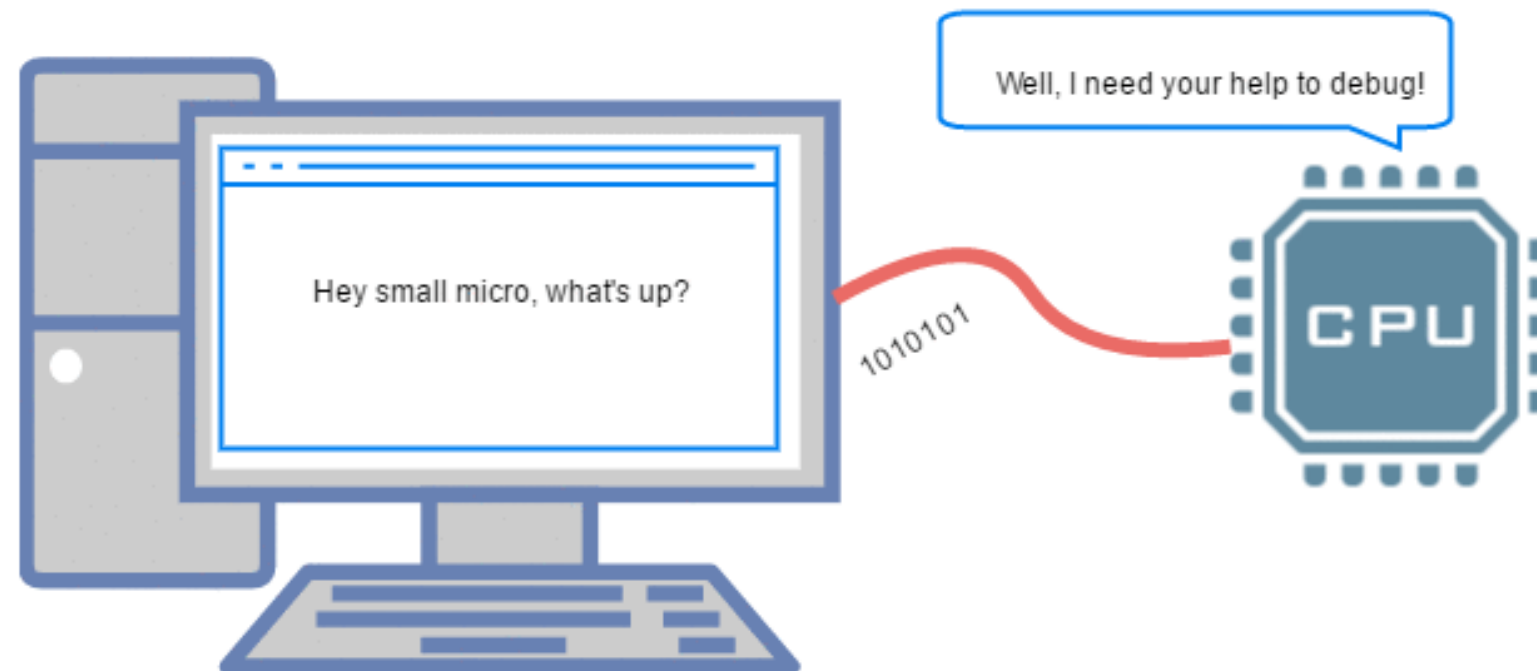




Serial Communication- USART



- PIC16F877A comes with inbuilt USART which can be used for Synchronous/Asynchronous communication.
- USART (Universal Synchronous Asynchronous Receiver Transmitter) are one of the basic interfaces which provide a cost effective simple and reliable communication between one controller to another controller or between a controller and PC.





USART -Registers



- PIC16F877A comes with inbuilt USART which can be used for Synchronous/Asynchronous communication.
- USART is a two wire communication system in which the data flow serially.
- USART is also a full-duplex communication, means you can send and receive data at the same time which can be used to communicate with peripheral devices, such as CRT terminals and personal computers

Register	Description
TXSTA	Transmit Status And Control Register
RCSTA	Receive Status And Control Register
SPBRG	USART Baud Rate Generator
TXREG	USART Transmit Register. Holds the data to to be transmitted on UART
RCREG	USART Transmit Register. Holds the data received from UART



USART -Registers



- The **USART** can be configured in the following modes:
- Asynchronous (full-duplex)
- Synchronous – Master (half-duplex)
- Synchronous – Slave (half-duplex)

Register	Description
TXSTA	Transmit Status And Control Register
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SPBRG	USART Baud Rate Generator
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TXSTA (Transmit Status And Control Register)



This register is used to configure the Serial communication for TX.

TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D
bit 7							bit 0

CSRC: Clock Source Select bit (Asynchronous mode:Don't care).

TX9: 9-bit Transmit Enable bit

1 = Selects 9-bit transmission

0 = Selects 8-bit transmission

TXEN: Transmit Enable bit



TXSTA (Transmit Status And Control Register)



SYNC: USART Mode Select bit

1 = Synchronous mode

0 = Asynchronous mode

BRGH: High Baud Rate Select bit

1 = High speed

0 = Low speed

TRMT: Transmit Shift Register Status bit

1 = TSR empty

0 = TSR full

TX9D: 9th bit of Transmit Data, can be Parity bit



RCSTA (Receive Status And Control Register)



This register is used to configure the Serial communication for RX.

RCSTA: RECEIVE STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7				bit 0			

SPEN: Serial Port Enable bit

1 = Serial port enabled (configures RC7/RX/DT and RC6/TX/CK pins as serial port pins)

0 = Serial port disabled

RX9: 9-bit Receive Enable bit

1 = Selects 9-bit reception

0 = Selects 8-bit reception

SREN: Single Receive Enable bit (Asynchronous mode:Don't care)

CREN: Continuous Receive Enable bit

Asynchronous mode:

1 = Enables continuous receive

0 = Disables continuous receive



RCSTA (Receive Status And Control Register)



ADDEN: Address Detect Enable bit

➤ Asynchronous mode 9-bit (RX9 = 1):

1 = Enables address detection, enables interrupt and load of the receive buffer when RSR is set

0 = Disables address detection, all bytes are received and ninth bit can be used as parity bit

FERR: Framing Error bit

➤ 1 = Framing error (can be updated by reading RCREG register and receive next valid byte)

0 = No framing error

OERR: Overrun Error bit

➤ 1 = Overrun error (can be cleared by clearing bit CREN)

0 = No overrun error

RX9D: 9th bit of Received Data (can be parity bit but must be calculated by user firmware)



SPBRG (USART Baud Rate Generator)



- The main criteria for UART communication is its baud rate.
- Both the devices Rx/Tx should be set to same baud rate for successful communication.
- This can be achieved by SPBRG register.
- SPBRG is a 8-bit register which controls the baud rate generation.
- The SPBRG register controls the period of a free running 8-bit timer.
- In Asynchronous mode, bit BRGH (TXSTA<2>) also controls the baud rate.
- In Synchronous mode, bit BRGH is ignored.
- Given the desired baud rate and FOSC, the nearest integer value for the SPBRG register can be calculated using the below formula.

BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = $F_{osc}/(64 (X + 1))$	Baud Rate = $F_{osc}/(16 (X + 1))$
1	(Synchronous) Baud Rate = $F_{osc}/(4 (X + 1))$	N/A

Legend: X = value in SPBRG (0 to 255)



References

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Thank You