SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A++' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECT312 – EMBEDDED SYSTEM DESIGN

III YEAR/ VI SEMESTER

1

UNIT 1 – **INTRODUCTION TO EMBEDDED SYSTEMS**

TOPIC 7 –EMBEDDED MEMORY

EMBEDDED MEMORY

1.Basic Memory types

2.Basic Memory Organization

3.Definitions of RAM, ROM and Cache Memory

4.Difference between Static and Dynamic RAM

5.Various Memory Control Signals

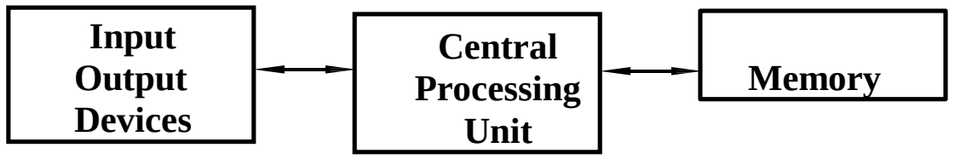
6.Memory Specifications

7.Basics of Memory Interfacing

EMBEDDED MEMORY

Processor Memory , Primary Memory , Memory Interfacing

Most of the modern computer system has been designed on the basis of an architecture called Von-Neumann Architecture1



The Von Neumann Architecture

The Memory stores the instructions as well as data. No one can distinguish an instruction and data. The CPU has to be directed to the address of the instruction codes.

The memory is connected to the CPU through the following lines

1.Address

2.Data

3.Control

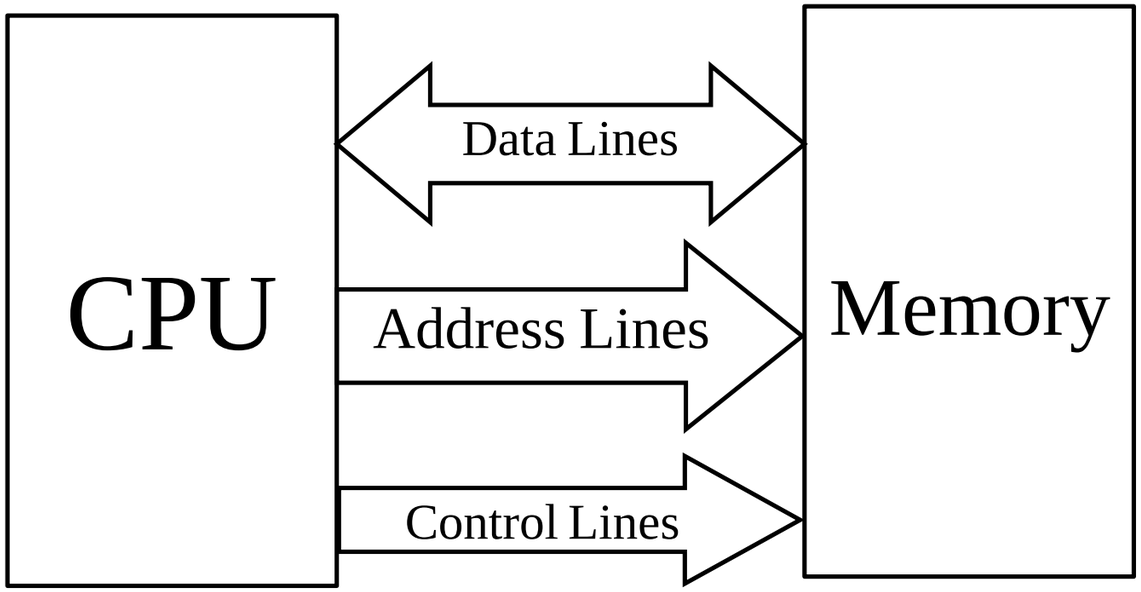
EMBEDDED MEMORY

- von Neumann architecture is a model for a computing machine that uses a single storage structure to hold both the set of instructions on how to perform the computation and the data required or generated by the computation.
- Such machines are also known as stored- program computers. The separation of storage from the processing unit is implicit in this model.

- By treating the instructions in the same way as the data, a stored-program machine can easily change the instructions.

- In other words the machine is reprogrammable. One important motivation for such a facility was the need for a program to increment or otherwise modify the address portion of instructions.
- This became less important when index registers and indirect addressing became customary features of machine architecture.

EMBEDDED MEMORY



In a memory read operation

- the CPU loads the address onto the address bus.
- Most cases these lines are fed to a decoder which selects the proper memory location.
- The CPU then sends a read control signal.
- The data is stored in that location is transferred to the processor via the data lines.

EMBEDDED MEMORY

In the memory write operation after the address is loaded the CPU sends the write control signal followed by the data to the requested memory location.

The memory can be classified in various ways i.e. based on the location, power consumption, way of data storage etc

The memory at the basic level can be classified as

1.Processor Memory (Register Array)

2.Internal on-chip Memory

3.Primary Memory

4.Cache Memory

5.Secondary Memory

EMBEDDED MEMORY

Processor Memory (Register Array)

- Most processors have some registers associated with the arithmetic logic units.
- They store the operands and the result of an instruction.
- The data transfer rates are much faster without needing any additional clock cycles.
- The number of registers varies from processor to processor.
- The more is the number the faster is the instruction execution.
- But the complexity of the architecture puts a limit on the amount of the processor memory.

EMBEDDED MEMORY

Internal on-chip Memory

•In some processors there may be a block of memory location.

•They are treated as the same way as the external memory. However it is very fast.

Primary Memory

•This is the one which sits just out side the CPU.

•It can also stay in the same chip as of CPU.

•These memories can be static or dynamic.

Cache Memory

•This is situated in between the processor and the primary memory.

•This serves as a buffer to the immediate instructions or data which the processor anticipates. There can be more than one levels of cache memory.

EMBEDDED MEMORY

Secondary Memory

•These are generally treated as Input/Output devices.

•They are much cheaper mass storage and slower devices connected through some input/output interface circuits.

•They are generally magnetic or optical memories such as Hard Disk and CDROM devices.

•The memory can also be divided into Volatile and Non-volatile memory.

Volatile Memory

•The contents are erased when the power is switched off.

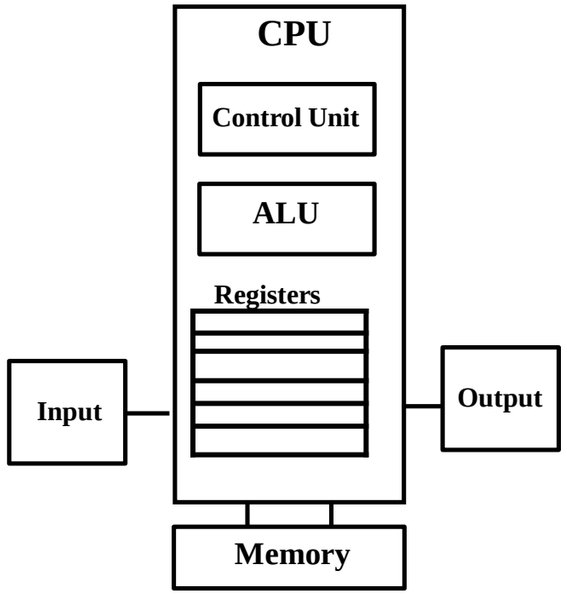
•Semiconductor Random Access Memories fall into this category.

Non-volatile Memory

The contents are intact even of the power is switched off. Magnetic Memories (Hard Disks), Optical Disks (CDROMs), Read Only Memories (ROM) fall under this category.

EMBEDDED MEMORY

The Internal Registers



Data Storage

An *m* word memory can store *m* x *n*: *m* words of *n* bits each. One word is located at one address therefore to address *m* words we need.

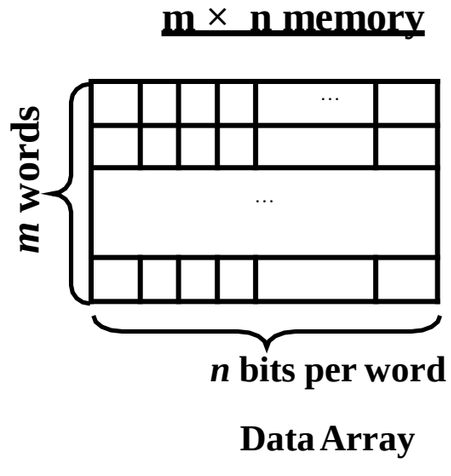
k = Log2(*m*) address input signals

or k number address lines can address $m = 2^k$ words

Example

4,096 x 8 memory:

- 32,768 bits ,
- 12 address input signals,
- 8 input/output data signals

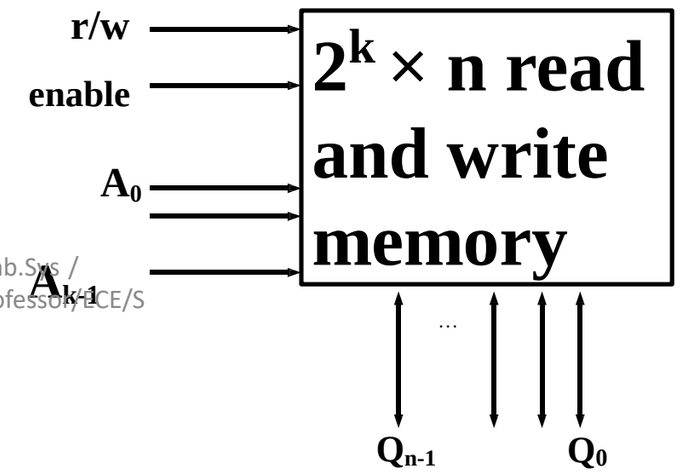


EMBEDDED MEMORY

Memory access

The memory location can be accessed by placing the address on the address lines. The control lines read/write selects read or write. Some memory devices are multi-port i.e. multiple accesses to different locations simultaneously

memory external view



Memory Array

EMBEDDED MEMORY

Memory Specifications

•The storage capacity: The number of bits/bytes or words it can store

•The memory access time (read access and write access):

- How long the memory takes to load the data on to its data lines after it has been addressed or how fast it can store the data upon supplied through its data lines. This reciprocal of the memory access time is known as Memory

Bandwidth

•The Power Consumption and Voltage Levels:

•The power consumption is a major factor in embedded systems.

•The lesser is the power consumption the more is packing density.

- Size: Size is directly related to the power consumption and data storage capacity.

EMBEDDED MEMORY

Generation 1

Generation 2

Generation 3

Generation 4

Four Generations of RAM chips

EMBEDDED MEMORY

There are two important specifications for the Memory as far as Real Time Embedded Systems are concerned.
–Write Ability
–Storage Performance

Write ability

It is the manner and speed that a particular memory can be written

- Ranges of write ability
  - High end
    - processor writes to memory simply and quickly e.g., RAM
  - Middle range
    - processor writes to memory, but slower e.g., FLASH, EEPROM (Electrically Erasable and Programmable Read Only Memory)
  - Lower range
    - special equipment, “programmer”, must be used to write to memory e.g., EPROM, OTP ROM (One Time Programmable Read Only Memory)
  - Low end
    - bits stored only during fabrication e.g., Mask-programmed ROM

EMBEDDED MEMORY

- In-system programmable memory
  - Can be written to by a processor in the embedded system using the memory
  - Memories in high end and middle range of write ability

Storage permanence

It is the ability to hold the stored bits. Range of storage permanence

- High end
  - essentially never loses bits
  - e.g., mask-programmed ROM

EMBEDDED MEMORY

- Middle range
  - holds bits days, months, or years after memory's power source turned off
  - e.g., NVRAM
- Lower range
  - holds bits as long as power supplied to memory
  - e.g., SRAM
- Low end
  - begins to lose bits almost immediately after written
  - e.g., DRAM Nonvolatile memory
- Holds bits after power is no longer supplied
- High end and middle range of storage permanence

COMMON MEMORY TYPES

Read Only Memory (ROM)

This is a nonvolatile memory. It can only be read from but not written to, by a processor in an embedded system. Traditionally written to, "programmed", before inserting to embedded system *Uses*

—Store software program for general-purpose processor

- program instructions can be one or more ROM words

—Store constant data needed by system

—Implement combinational circuit

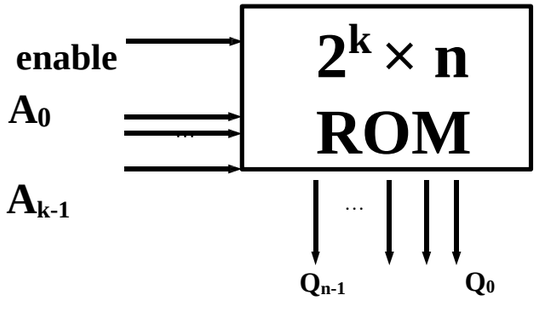
Horizontal lines represents the words.

The vertical lines give out data.

These lines are connected only at circles.

If address input is 010 the decoder sets 2nd word line to 1.

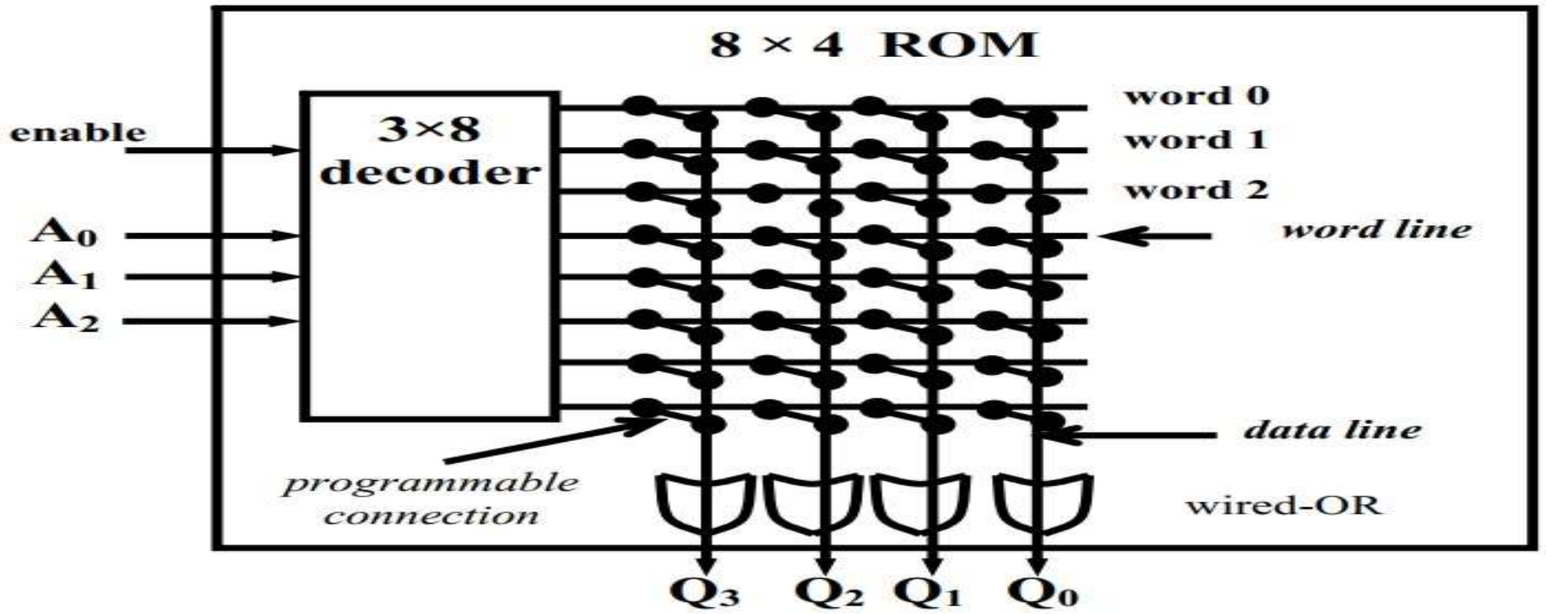
The data lines Q3 and Q1 are set to 1 because there is a "programmed"



The ROM Structure

EMBEDDED MEMORY

Internal view



The example of a ROM with decoder and data storage

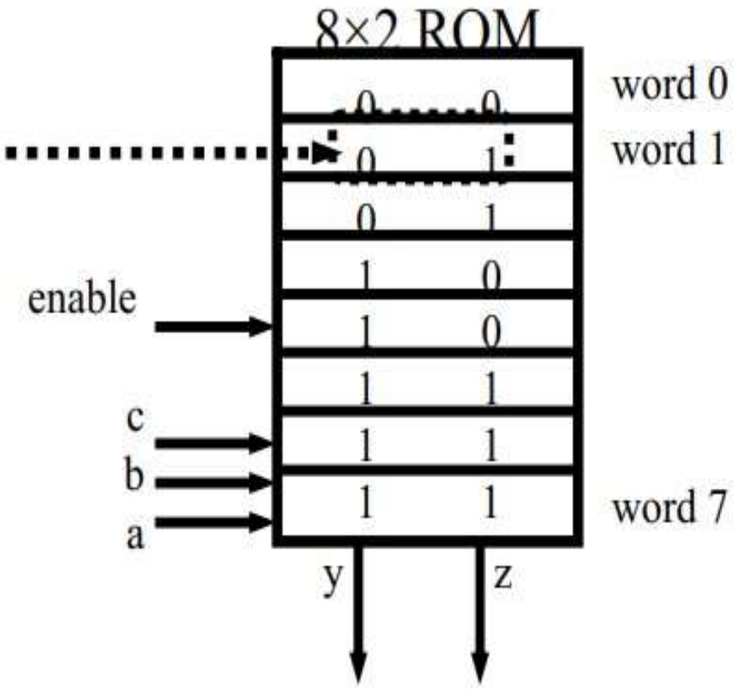
Implementation of Combinatorial Functions

- Any combinational circuit of *n* functions of same *k* variables can be done with 2^k x *n* ROM.
- The inputs of the combinatorial circuit are the address of the ROM locations.
- The output is the word stored at that location.

EMBEDDED MEMORY

Truth table

Inputs (address)			Outputs	
a	b	c	y	z
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	1	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1



Mask-programmed ROM

The connections “programmed” at fabrication.

- They are a set of masks. It can be written only once (in the factory).
- But it stores data for ever.
- Thus it has the highest storage permanence.
- Them bits never change unless damaged.
- These are typically used for final design of high-volume systems.

EMBEDDED MEMORY

OTP ROM: One-time programmable ROM

The Connections “programmed” after manufacture by user.

The user provides file of desired contents of ROM.

The file input to machine called ROM programmer. Each programmable connection is a fuse.

The ROM programmer blows fuses where connections should not exist.

- Very low write ability: typically written only once and requires ROM programmer device
- Very high storage permanence: bits don’t change unless reconnected to programmer and more fuses blown
- Commonly used in final products: cheaper, harder to inadvertently modify

EMBEDDED MEMORY

EPROM: Erasable programmable ROM

This is known as erasable programmable read only memory.

The programmable component is a MOS transistor.

This transistor has a “floating” gate surrounded by an insulator.

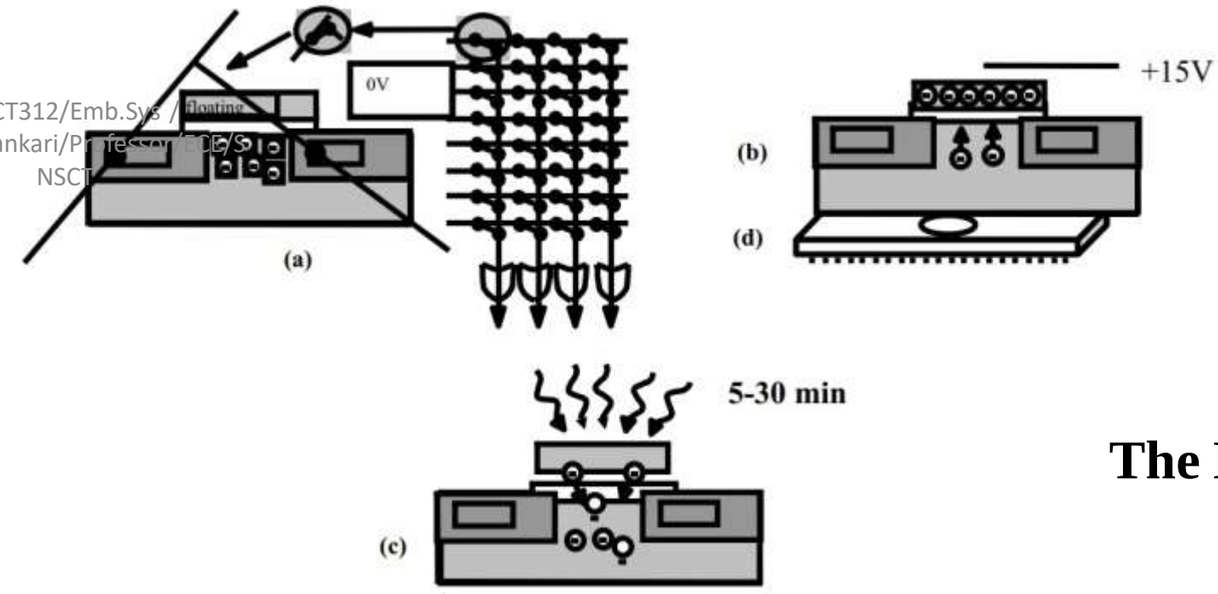
The Negative charges form a channel between source and drain storing a logic 1. The Large positive voltage at gate causes negative charges to move out of channel and get trapped in floating gate storing a logic 0.

The (Erase) Shining UV rays on surface of floating-gate causes negative charges to return to channel from floating gate restoring the logic 1.

EMBEDDED MEMORY

The EPROM has

- Better write ability
  - can be erased and reprogrammed thousands of times
- Reduced storage permanence
  - program lasts about 10 years but is susceptible to radiation and electric noise
- Typically used during design development



The EPROM

EMBEDDED MEMORY

EEPROM

EEPROM is otherwise known as Electrically Erasable and Programmable Read Only Memory. It is erased typically by using higher than normal voltage.It can program and erase individual words unlike the EPROMs where exposure to the UV light erases everything. It has

- Better write ability
  - —can be in-system programmable with built-in circuit to provide higher than normal voltage
    - built-in memory controller commonly used to hide details from memory user
  - —writes very slow due to erasing and programming
    - “busy” pin indicates to processor EEPROM still writing
  - —can be erased and programmed tens of thousands of times
- Similar storage permanence to EPROM (about 10 years)
- Far more convenient than EPROMs, but more expensive

EMBEDDED MEMORY

Flash Memory

It is an extension of EEPROM. It has the same floating gate principle and same write ability and storage permanence. It can be erased at a faster rate i.e. large blocks of memory erased at once, rather than one word at a time. The blocks are typically several thousand bytes large

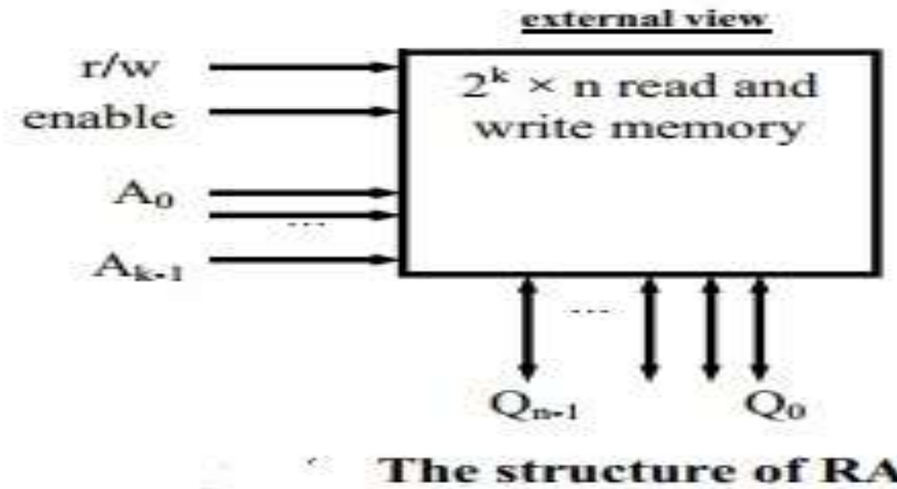
- Writes to single words may be slower
  - Entire block must be read, word updated, then entire block written back
- Used with embedded systems storing large data items in nonvolatile memory
  - e.g., digital cameras, TV set-top boxes, cell phones

EMBEDDED MEMORY

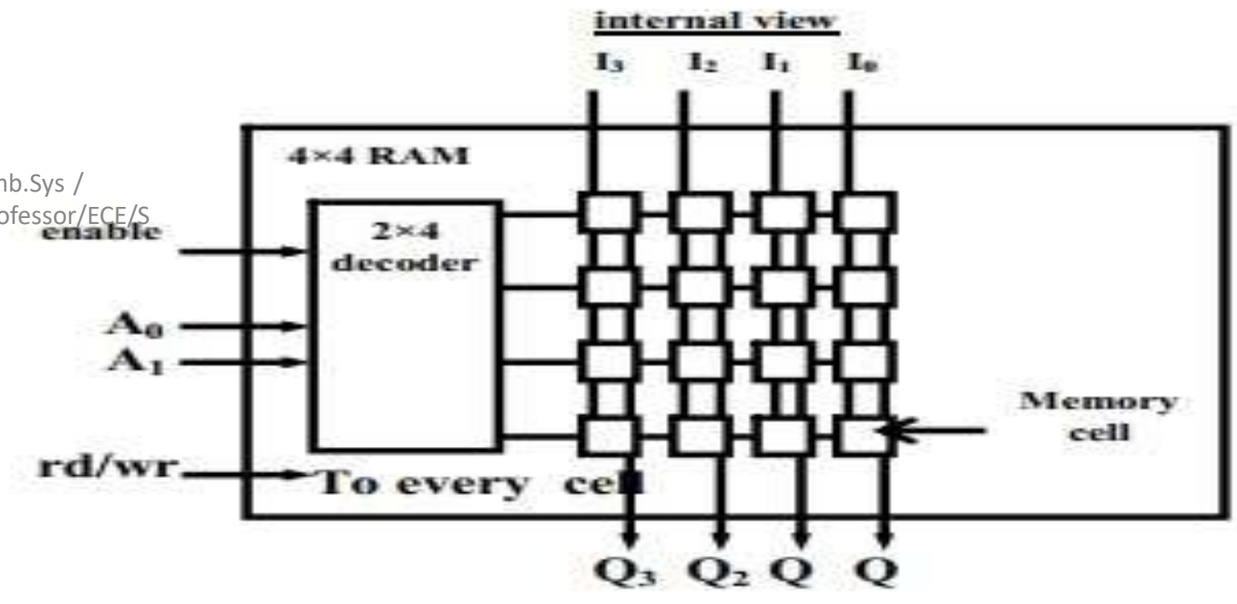
RAM: “Random-access” memory

- Typically volatile memory
  - bits are not held without power supply
- Read and written to easily by embedded system during execution
- Internal structure more complex than ROM
  - a word consists of several memory cells, each storing 1 bit
  - each input and output data line connects to each cell in its column
  - rd/wr connected to every cell
  - when row is enabled by decoder, each cell has logic that stores input data bit when rd/wr indicates write or outputs stored bit when rd/wr indicates read

EMBEDDED MEMORY



The structure of RAM



The RAM decoder and access

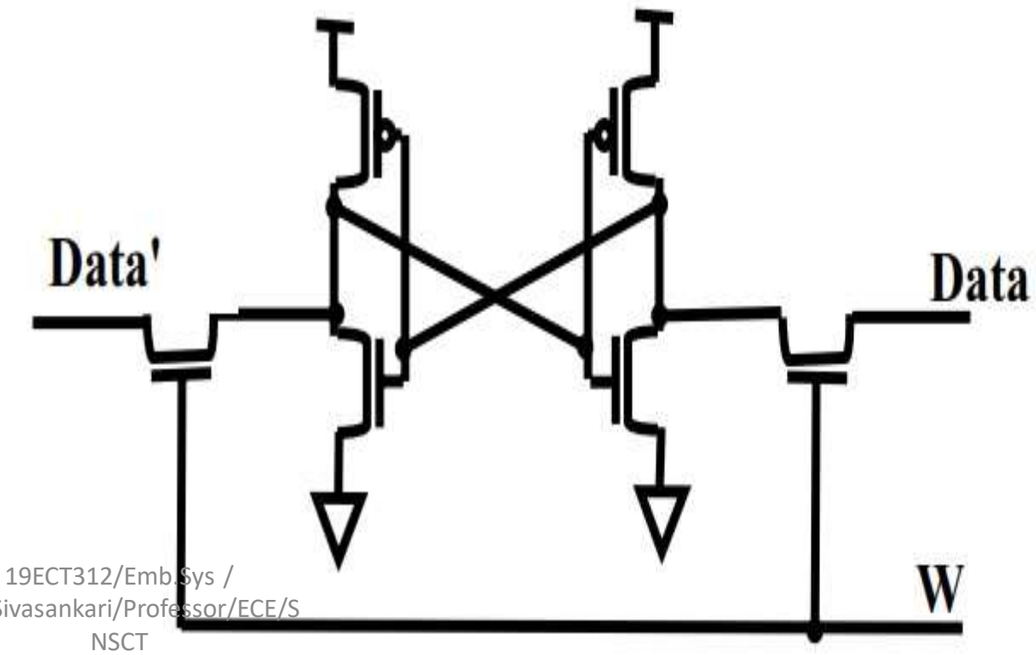
EMBEDDED MEMORY

Basic types of RAM

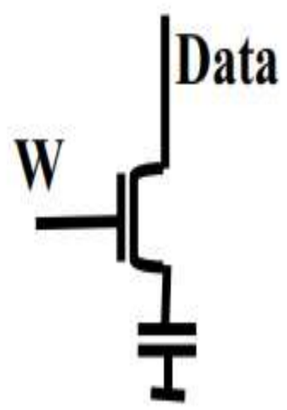
- SRAM: Static RAM
  - Memory cell uses flip-flop to store bit
  - Requires 6 transistors
  - Holds data as long as power supplied
- DRAM: Dynamic RAM
  - Memory cell uses MOS transistor and capacitor to store bit
  - More compact than SRAM
  - “Refresh” required due to capacitor leak
    - word’s cells refreshed when read
  - Typical refresh rate 15.625 microsec.
  - Slower to access than SRAM

EMBEDDED MEMORY

SRAM



DRAM



EMBEDDED MEMORY

Ram variations

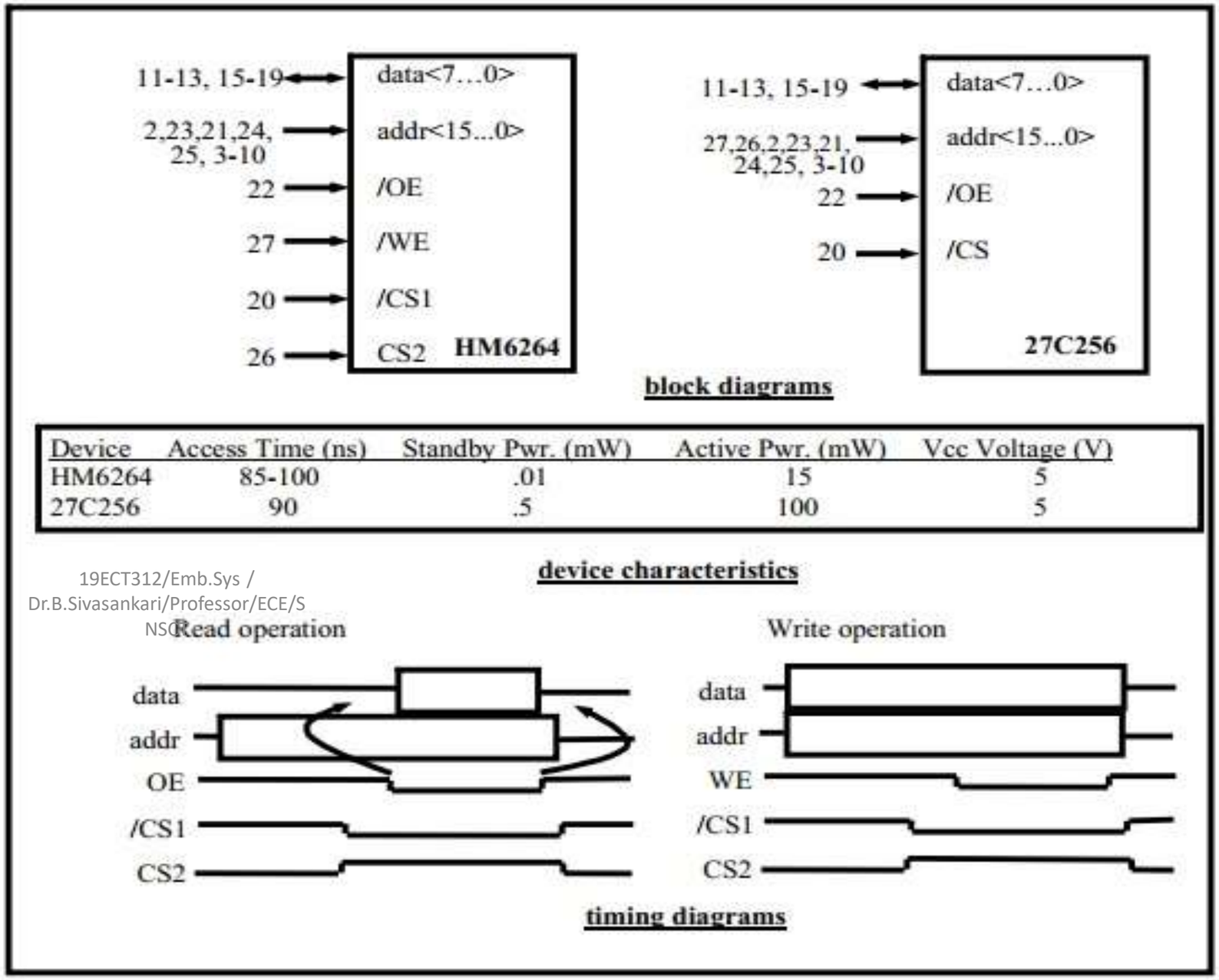
- PSRAM: Pseudo-static RAM
  - —DRAM with built-in memory refresh controller
  - —Popular low-cost high-density alternative to SRAM
- NVRAM: Nonvolatile RAM
  - —Holds data after external power removed
  - —Battery-backed RAM
    - SRAM with own permanently connected battery
    - writes as fast as reads
    - no limit on number of writes unlike nonvolatile ROM-based memory
  - —SRAM with EEPROM or flash stores complete RAM contents on EEPROM or flash before power

EMBEDDED MEMORY

Example: HM6264 & 27C256 RAM/ROM devices

- Low-cost low-capacity memory devices
- Commonly used in 8-bit microcontroller-based embedded systems
- First two numeric digits indicate device type
  - RAM: 62
  - ROM: 27
- Subsequent digits indicate capacity in kilobits

EMBEDDED MEMORY



block diagrams

Device	Access Time (ns)	Standby Pwr. (mW)	Active Pwr. (mW)	Vcc Voltage (V)
HM6264	85-100	.01	15	5
27C256	90	.5	100	5

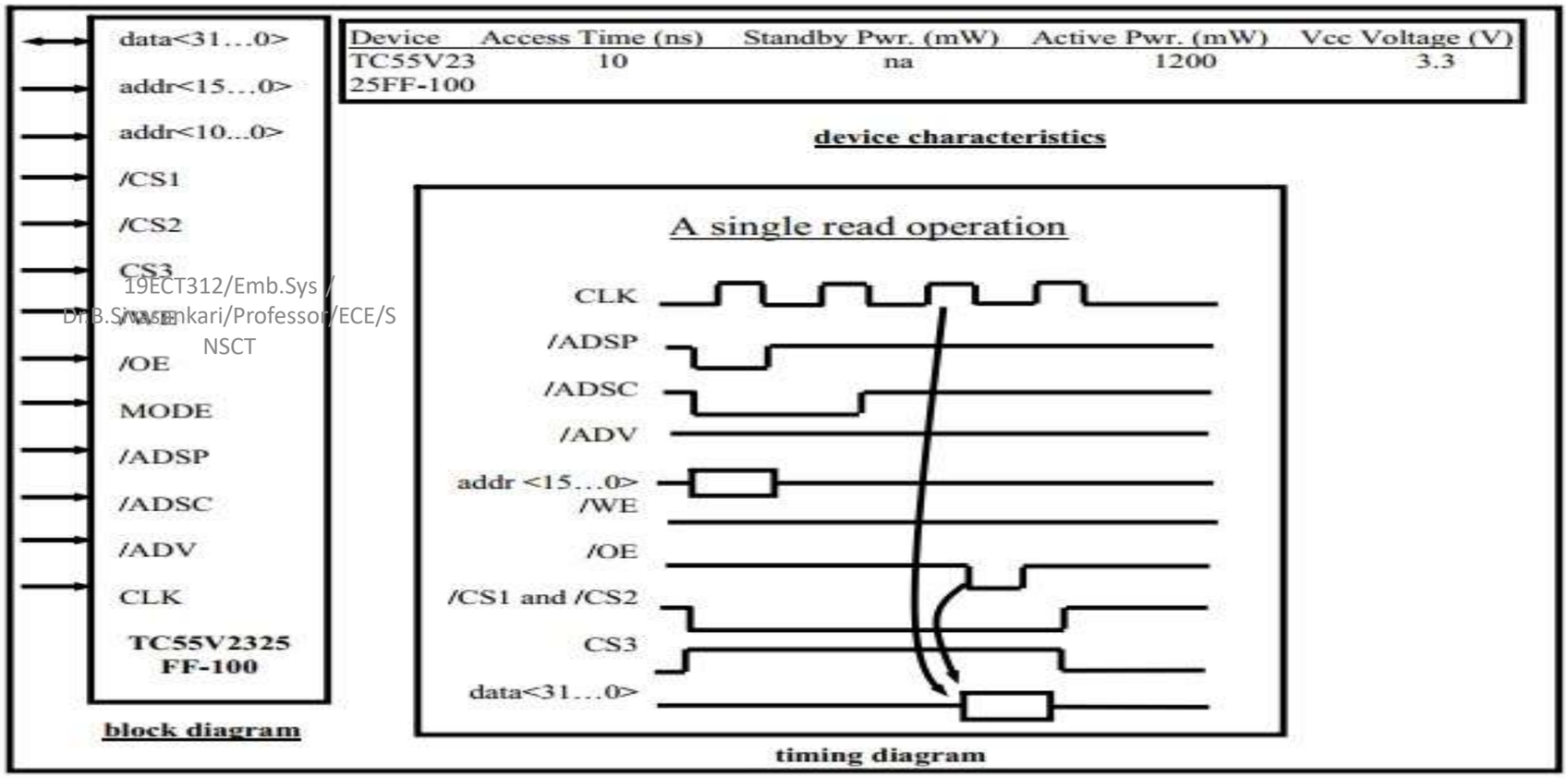
device characteristics

timing diagrams

EMBEDDED MEMORY

Example: TC55V2325FF-100 memory device

- 2-megabit synchronous pipelined burst SRAM memory device
- Designed to be interfaced with 32-bit processors
- Capable of fast sequential reads and writes as well as single byte I/O



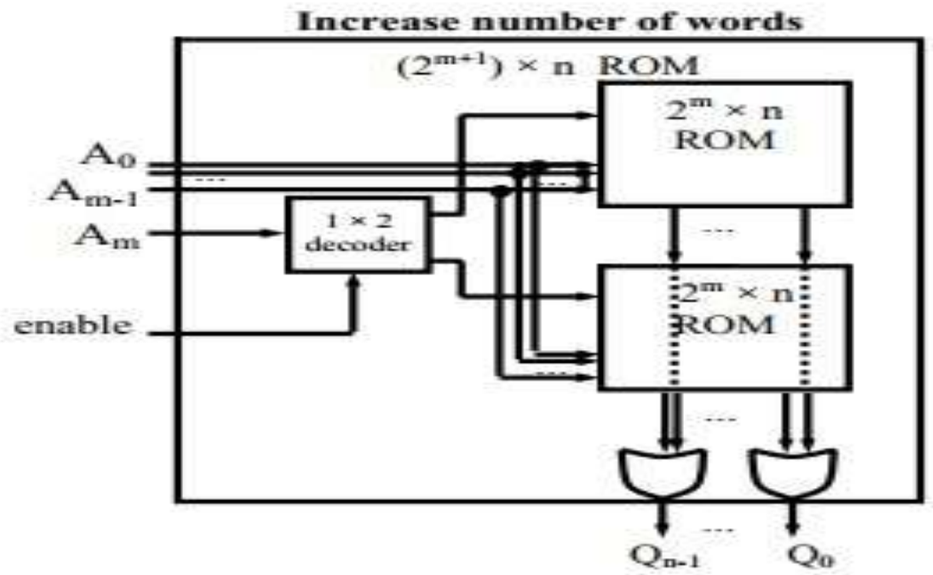
EMBEDDED MEMORY

Composing memory

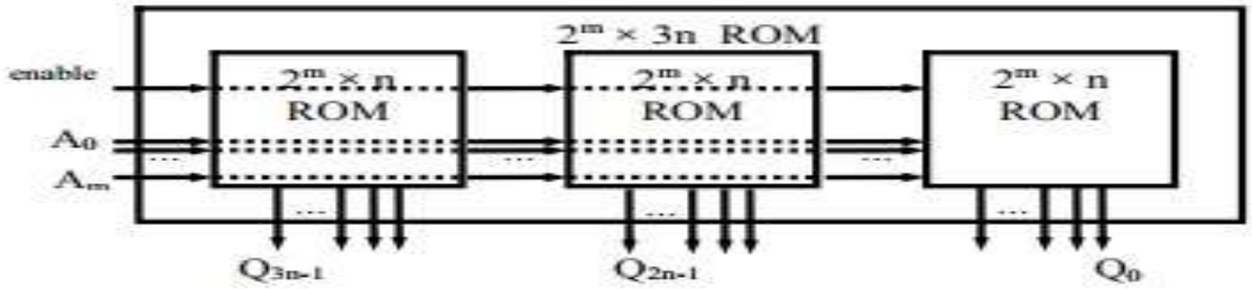
- Memory size needed often differs from size of readily available memories
- When available memory is larger, simply ignore unneeded high-order address bits and higher data lines
- When available memory is smaller, compose several smaller memories into one larger memory
  - Connect side-by-side to increase width of words
  - Connect top to bottom to increase number of words
    - added high-order address line selects smaller memory containing desired word using a decoder
  - Combine techniques to increase number and width of words

EMBEDDED MEMORY

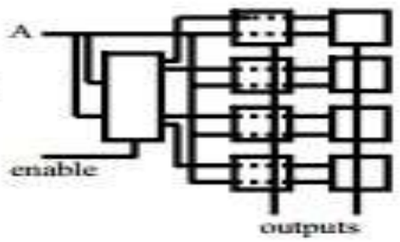
Increase number of words



Increase width of words



Increase number and width of words



Composing Memory

THANK YOU