SNS COLLEGE OF TECHNOLOGY

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB211 – MICROCONTROLLER PROGRAMMING & INTERFACING

II YEAR IV SEM

UNIT II – PIC TIMER, SERIAL PORT AND INTERRUPT

TOPIC 2 – PIC Time Delay and Instruction Pipeline

PIC Instruction Pipeline

> The control unit in all Central Processing Units (CPUs) follows the same

  basic instruction processing sequence:

   fetch the instruction

   decode the instruction

   execute the instruction

> Modern, high-performance CPUs (like MIPS®) use a technique called

  Pipelining

PIC Instruction Pipeline

➢ phases of instruction processing are executed in independent overlapping stages
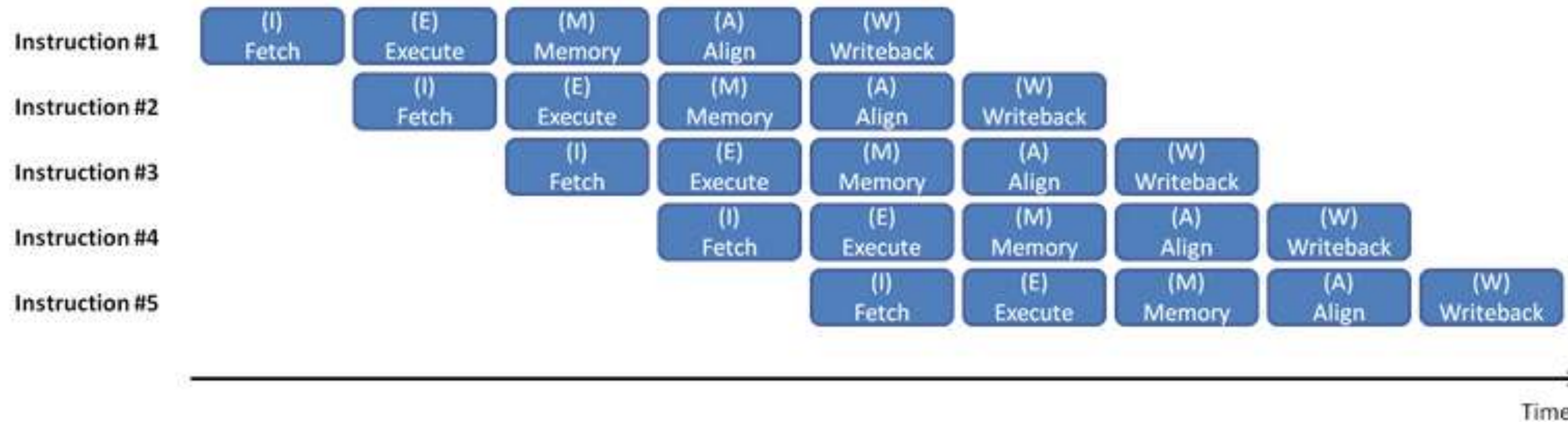

Sequential Instruction Execution
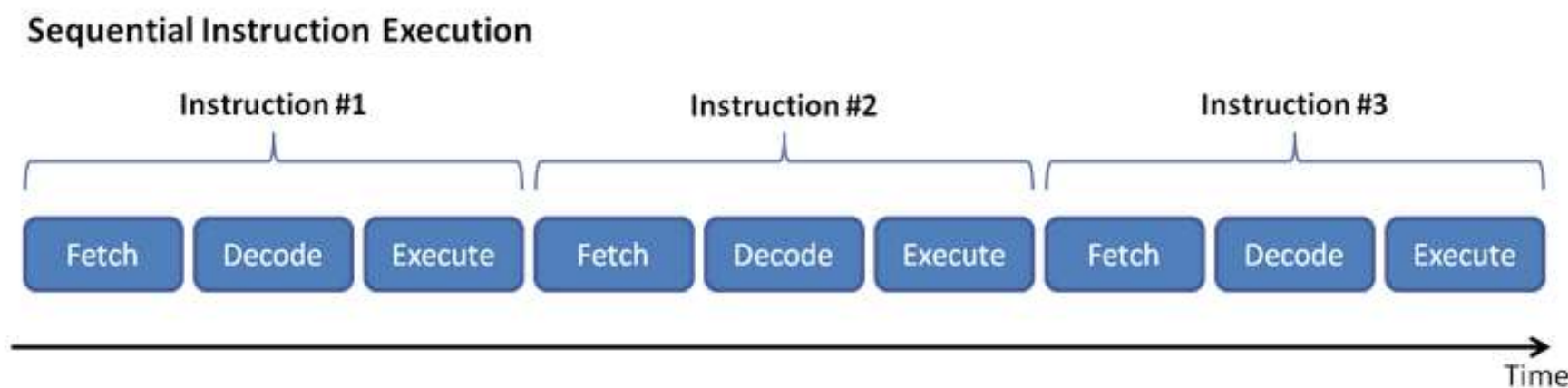
➢ N-stage pipelines therefore have n-instructions at different stages of execution moving through the pipeline, similar to an automotive assembly line.

General Instruction Pipeline

PIC32MZ Pipelined Instruction Execution

PIC Clock & Instruction Cycle

- Clock from the oscillator enters a microcontroller via OSC1 pin where internal circuit of a microcontroller divides the clock into four even clocks Q1, Q2, Q3 and Q4 which do not overlap.

- These four clocks make up one **instruction cycle** (also called machine cycle) during which one instruction is executed.
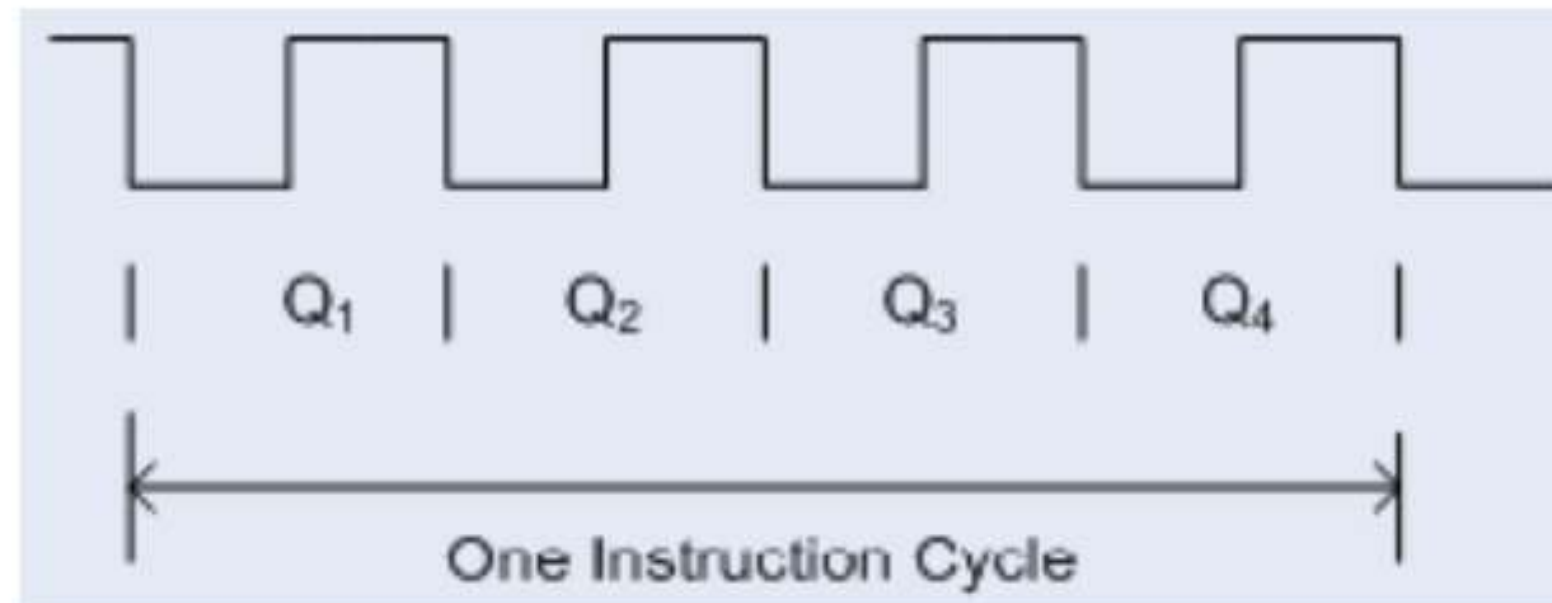
PIC Clock & Instruction Cycle

- Execution of instruction starts by calling an instruction that is next in string.

- Instruction is called from program memory on every Q1 and is written in Instruction Register (IR) on Q4.

- Decoding and execution of instruction are done between the next Q1 and Q4 cycles. The following diagram shows the relationship between instruction cycle and clock of the oscillator (OSC1) as well as that of internal clocks Q1 – Q4.

- Program Counter (PC) holds information about the address of the next instruction.
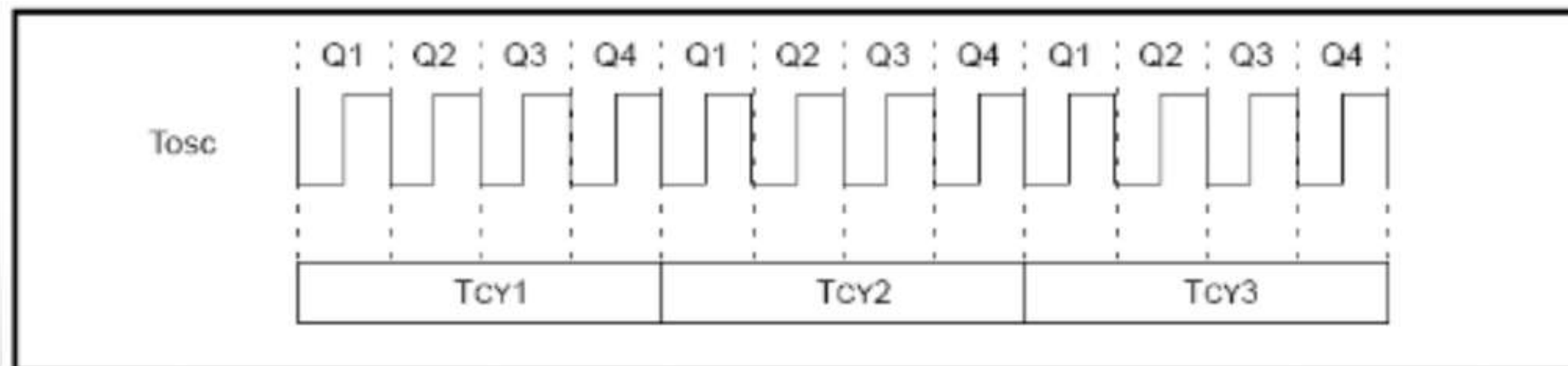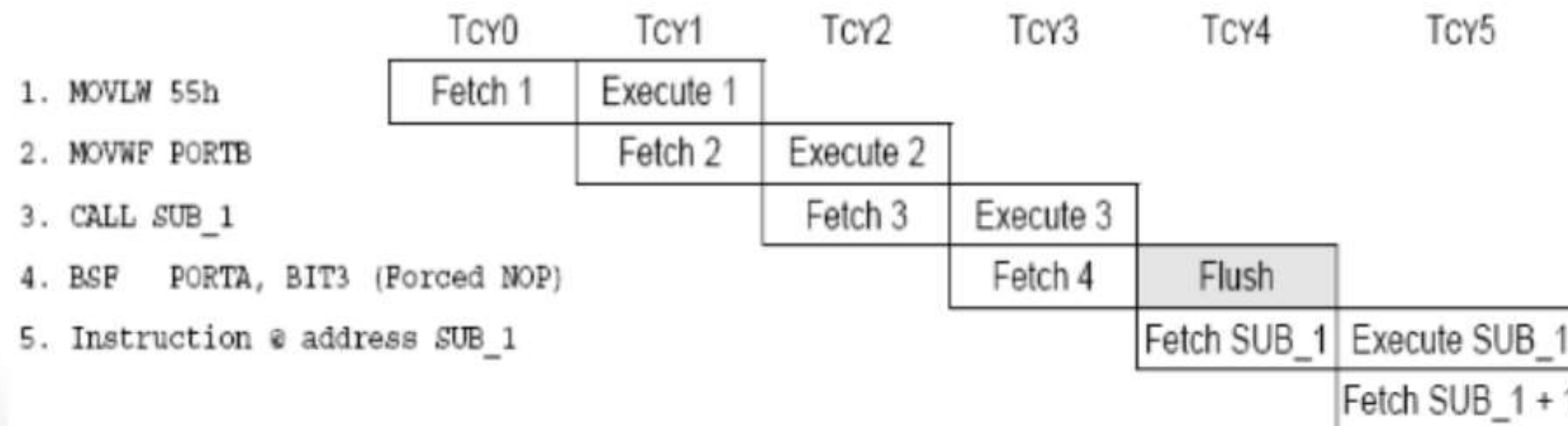
Pipelining in PIC16F877A

- There are 35 single word instructions. A two-stage pipeline overlaps fetch and execution of instructions. As a result, all instructions execute in a single cycle except for program branches. These take two cycles since the fetch instruction is "flushed" from the pipeline while the new instruction is being fetched and then executed.

- A typical picture of the pipeline is shown in Figure 3.

Figure3: Instruction Pipeline Flow

	TCY0	TCY1	TCY2	TCY3	TCY4	TCY5
1. MOVLW 55h	Fetch 1	Execute 1				
2. MOVWF PORTB		Fetch 2	Execute 2			
3. CALL SUB_1			Fetch 3	Execute 3		
4. BSF PORTA, BIT3 (Forced NOP)				Fetch 4	Flush	
5. Instruction @ address SUB_1					Fetch SUB_1	Execute SUB_1
						Fetch SUB_1 + 1

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Thank You