SNS COLLEGE OF TECHNOLOGY

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Coimbatore-35

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MICROPROCESSORS AND MICROCONTROLLERS

II YEAR/ IV SEMESTER

UNIT II – I/O INTERFACING

TOPIC – Programmable Interval Timer

Programmable Interval Timer

- PTI (programmable Interval Timer)
- The 8253 chip was used in the IBM PC/XT, but starting with the IBM PC/AT, the 8254 replaced the 8253.
- 8253 and 8254 have exactly the same pinout.
- 8254 is a superset of the 8253

Programmable Interval Timer

The 8254 programmable interval timer consists of three independent 16-bit programmable counters (**timers**).

Each counter is capable in of counting in binary or BCD with a maximum fre quency of 10MHz.

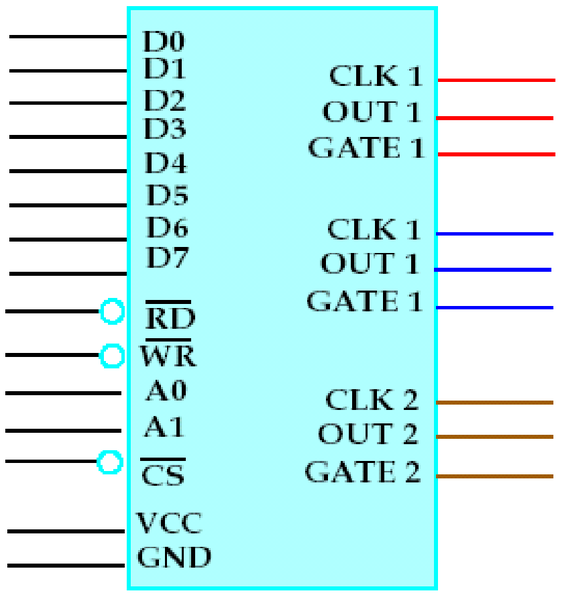
Used for controlling real-time events such as real-time clock, events counter and motor speed and direction control.

Usually decoded at port address 40H-43H and has following functions:

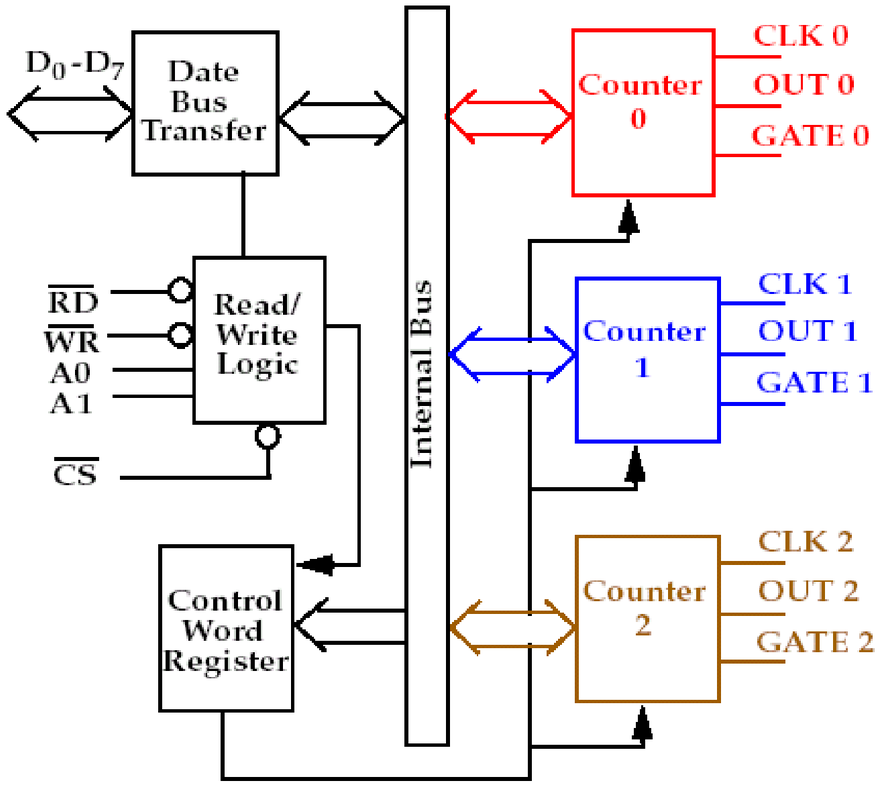
- IGenerate a basic timer interrupt that occurs at approximately 18.2Hz.
- Cause the DRAM memory system to be refreshed
- Providing a timing source to the internal speaker and other devices.

Programmable Interval Timer

Pin-out



Internal structure



Programmable Interval Timer

A0, A1, and CS

- Inside the 8253/54 timer, there are 3 counters.
- Each timer works independently and programmed separately.
- Each counter is assigned an individual port address.
- The control register common to all 3 counters and has its own port.

Table 5-1: Addressing 8253/54 Ports

$\overline{CS}$	A1	A0	Port
0	0	0	Counter 0
0	0	1	Counter 1
0	1	0	Counter 2
0	1	1	Control register
1	x	x	8253/54 is not selected

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Programmable Interval Timer

A_1, A_0 The **address inputs** select one of the four internal registers with the 8254 as follows:

A_1	A_0	Function
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word

CLK The **clock** input is the timing source for each of the internal counters. It is often connected to the PCLK signal from the bus controller.

$\overline{CS}$ **Chip Select** enables the 8254 for programming, and reading and writing to a counter.

G The **gate** input controls the operation of the counter in some modes of operation.

Programmable Interval Timer

CLK

• CLK is the input clock frequency, which can range between 0 and 2 MHz for the 8253.

• For input frequencies higher than 2 MHz, the 8254 must be used.

• The 8254 can go as high as 8 MHz, and 8254-2 can go 10 MHz.

OUT

• Can have square-wave, one-shot, and other square-shape waves for various duty cycles but no sine-wave or saw-tooth shapes.

Gate

• This pin is used to enable or disable the counter.

Programmable Interval Timer

D0-D7

- The D0-D7 data bus of the 8253/54 is a bidirectional bus connected to D0-D7 of the system data bus.
- RD and WR are connected to IOR and IOW control signals of the system bus.

Initialization of the 8253/54

- Each of the three counters of the 8253/54 must be programmed separately.
- The 8253/54 must be initialized before it is used.

Programmable Interval Timer

GND **Ground** connects to the system ground bus.

OUT A **counter output** is where the wave-form generated by the timer is available.

$\overline{RD}$ **Read** causes data to be read from the 8254 and often connects to the I/O read signal.

Vcc **Power** supply pin 5.0V.

$\overline{WR}$ **Write** causes data to be written to the 8254 and often connects to the I/O write signal.

THANK YOU