



SNS COLLEGE OF TECHNOLOGY

An Autonomous Institution
Coimbatore-35



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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MICROPROCESSORS AND MICROCONTROLLERS

II YEAR/ IV SEMESTER

UNIT II – I/O Interfacing

TOPIC – Parallel Communication Interface



8255 ARCHITECTURE



- It is an I/O port chip used for interfacing I/O devices with microprocessor system. It is a device used to implement parallel data transfer between processor and slow peripheral devices like ADC, DAC, keyboard, 7-segment display, LCD etc.
- It is a programmable device.
- It has 24 I/O programmable pins like PA, PB, PC (3-8 pins).
- 8255A has three ports
 - PORT A
 - PORT B
 - PORT C
 - Port A and Port B are 8 bit parallel ports.
 - Port C can be split into two parts, i.e. PORT C lower (PC0-PC3) and PORT C upper (PC7-PC4) by the control word



8255 ARCHITECTURE



These three ports are further divided into two groups,

i.e. Group A includes PORT A and upper PORT C.

Group B includes PORT B and lower PORT C

These two groups can be programmed in three different modes.

Three operating modes :

Mode-0(simple I/O port)

Mode-1(Handshake I/O port)

Mode-2(Bidirectional I/O port)

In this mode, Port A and B is used as two 8-bit ports and Port C as two 4-bit ports.

Each port can be programmed in either input mode or output mode where outputs are latched and inputs are not latched.

Ports do not have interrupt capability.

Ports in mode 0 is used to interfaces LEDs, Hexa keypad and 7 segment LEDS to the processor.



8255 ARCHITECTURE



In this mode, Port A and B is used as 8-bit I/O ports.

They can be configured as either input or output ports.

Each port uses three lines from port C as handshake signals.

Inputs and outputs are latched

MODE 1 :(Input/output with Hand shake)

In this mode, input or output is transferred by hand shaking Signals.

Handshaking signals is used to transfer data between whose data transfer is not same.

The computer send the data to the printer large speed compared to the printer.

When computer send the data according to the printer speed at the time only, printer can accept.

If printer is not ready to accept the data then after sending the data bus , computer uses another handshaking signal to tell printer that valid data is available on the data bus.

Each port uses three lines from port C as handshake signals



§255 ARCHITECTURE



In this mode, Port A can be configured as the bidirectional port and Port B either in Mode 0 or Mode 1.

Port A uses five signals from Port C as handshake signals for data transfer.

The remaining three signals from Port C can be used either as simple I/O or as handshake for port B.

This mode allows bidirectional data transfer over a single 8-bit data bus using handshake signals.

This feature is possible only Group A

Port A is working as 8-bit bidirectional.

PC3-PC7 is used for handshaking purpose.

The data is sent by CPU through this port, when the peripheral request it.

CONTROL WORD FORMATS:

In the INPUT mode, When RESET is High all 24 pins (3-ports) be a input mode.



8255 PIN DIAGRAM

PA3	1		40	PA4
PA2	2		39	PA5
PA1	3		38	PA6
PA0	4		37	PA7
\overline{RD}	5		36	\overline{VWR}
\overline{CS}	6		35	RESET
gnd	7		34	D0
A1	8		33	D1
A0	9		32	D2
PC7	10	8255	31	D3
PC6	11	PPI	30	D4
PC5	12		29	D5
PC4	13		28	D6
PC0	14		27	D7
PC1	15		26	Vcc
PC2	16		25	PB7
PC3	17		24	PB6
PB0	18		23	PB5
PB1	19		22	PB4
PB2	20		21	PB3



8255 ARCHITECTURE



Data bus(D_0 - D_7): These are 8-bit bi-directional buses, connected to 8086 data bus for transferring data.

CS: This is Active Low signal. It stands for Chip Select. A LOW on this input selects the chip and enables the communication between the 8255 and the CPU.

Read: This is Active Low signal, when it is Low the microprocessor reads data from a selected I/O port of 8255A.

Write: This is Active Low signal, when it is Low the microprocessor writes data into a selected I/O port . RESET: This is used to reset the device. That means clear control registers.

PA_0 - PA_7 : It is the 8-bit bi-directional I/O pins used to send the data to peripheral or to receive the data from peripheral.

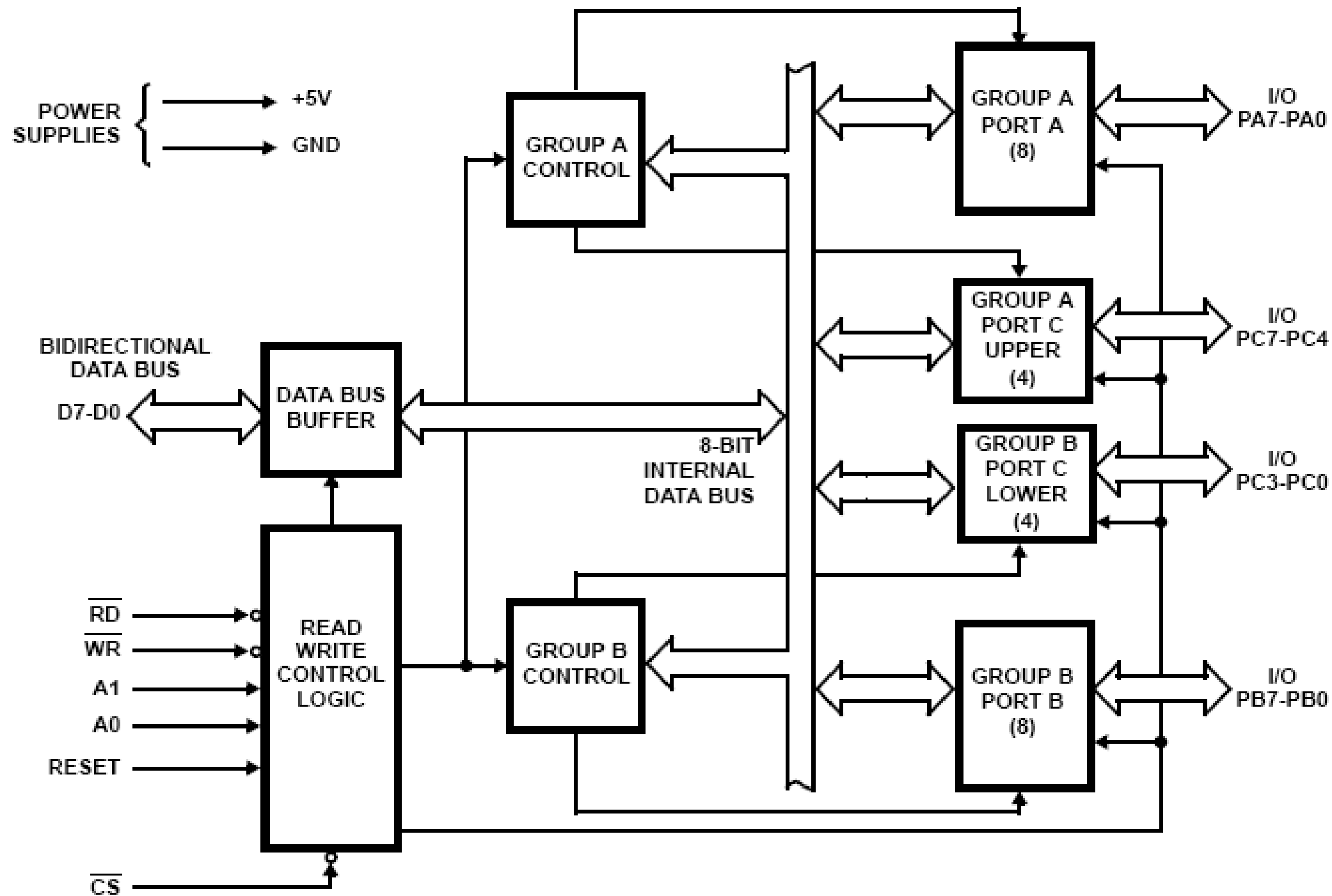
PB_0 - PB_7 : Similar to PA

PC_0 - PC_7 : This is also 8-bit bidirectional I/O pins. These lines are divided into two groups.

1. PC_0 to PC_3 (Lower Groups)
2. PC_4 to PC_7 (Higher groups)



8255 ARCHITECTURE





8255 ARCHITECTURE



It is a 8-bit bidirectional Data bus.

Used to interface between 8255 data bus with system bus.

The internal data bus and Outer pins D_0 - D_7 pins are connected in internally.

The direction of data buffer is decided by Read/Control Logic.

This is getting the input signals from control bus and Address bus

Control signal are RD and WR.

Address signals are A0,A1,and CS.

8255 operation is enabled or disabled by CS.

Group A and B get the Control Signal from CPU and send the command to the individual control blocks.

- Group A send the control signal to port A and Port C (Upper) PC7-PC4.
- Group B send the control signal to port B and Port C (Lower) PC3-PC0.
- PORT A:
- This is a 8-bit buffered I/O latch.
- It can be programmed by mode 0 , mode 1, mode 2 .



8255 ARCHITECTURE



Two control words:

I/O mode set control word(MSW)

Bit set/reset control word(BSR)

MSW is used to specify I/O functions.

BSR is used to set/reset individual pins of Port C.

Both the control words are written in the same control register.

8255 ports are programmed by writing control word in the control word in the control register.

For setting I/O functions and mode of operation the I/O mode set control word is send to control register.

For setting/ resetting pins of port C, the bit set/reset control word is send to control register.



THANK YOU