SNS COLLEGE OF TECHNOLOGY

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Coimbatore-35

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

MICROPROCESSORS AND MICROCONTROLLERS

II YEAR/ IV SEMESTER

UNIT 1 – 8085 AND 8086 ARCHITECTURE

TOPIC – Interrupts

INTERRUPTS

The Interrupt is the method to indicate the microcontroller by sending an interrupt signal. After receiving an interrupt, the microcontroller interrupts whatever it is doing and serves the device. The program associated with the interrupt is called the interrupt service routine (ISR). When an interrupt is invoked, the microcontroller runs the interrupt service routine. For every interrupt, there is a fixed location set aside to hold the addresses of ISRs.

- The following events will cause an interrupt:
- 1. Timer 0 Overflow.
- 2. Timer 1 Overflow.
- 3. Reception/Transmission of Serial Character.
- 4. External Event 0.
- 5. External Event 1

INTERRUPTS

To distinguish between various interrupts and executing different code depending on what interrupt was triggered, 8051may be jumping to a fixed address when a given interrupt occurs as shown in Table.

Interrupt	ROM Location (Hex)	Pin	Flag Clearing
Reset	0000	9	Auto
External hardware interrupt 0 (INT0)	0003	P3.2 (12)	Auto
Timer 0 interrupt (TF0)	000B		Auto
External hardware interrupt 1 (INT1)	0013	P3.3 (13)	Auto
Timer 1 interrupt (TF1)	001B		Auto
Serial COM interrupt (RI and TI)	0023		Programmer clears it.

ENABLING AND DISABLING THE INTERRUPTS

D7							D0
EA	--	ET2	ES	ET1	EX1	ET0	EX0

EA	IE.7	Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit.
--	IE.6	Not implemented, reserved for future use.*
ET2	IE.5	Enables or disables Timer 2 overflow or capture interrupt (8052 only).
ES	IE.4	Enables or disables the serial port interrupt.
ET1	IE.3	Enables or disables Timer 1 overflow interrupt.
EX1	IE.2	Enables or disables external interrupt 1.
ET0	IE.1	Enables or disables Timer 0 overflow interrupt.
EX0	IE.0	Enables or disables external interrupt 0.

*User software should not write 1s to reserved bits. These bits may be used in future flash microcontrollers to invoke new features.

PROGRAMMING EXTERNAL HARDWARE INTERRUPTS

The 8051 has two external hardware interrupts PIN 12 (P3.2) and Pin 13 (P3.3), designated as INT0 and INT1.

Upon activation of these pins, the 8051 finishes the execution of current instruction whatever it is executing and jumps to the vector table to perform the interrupt service routine.

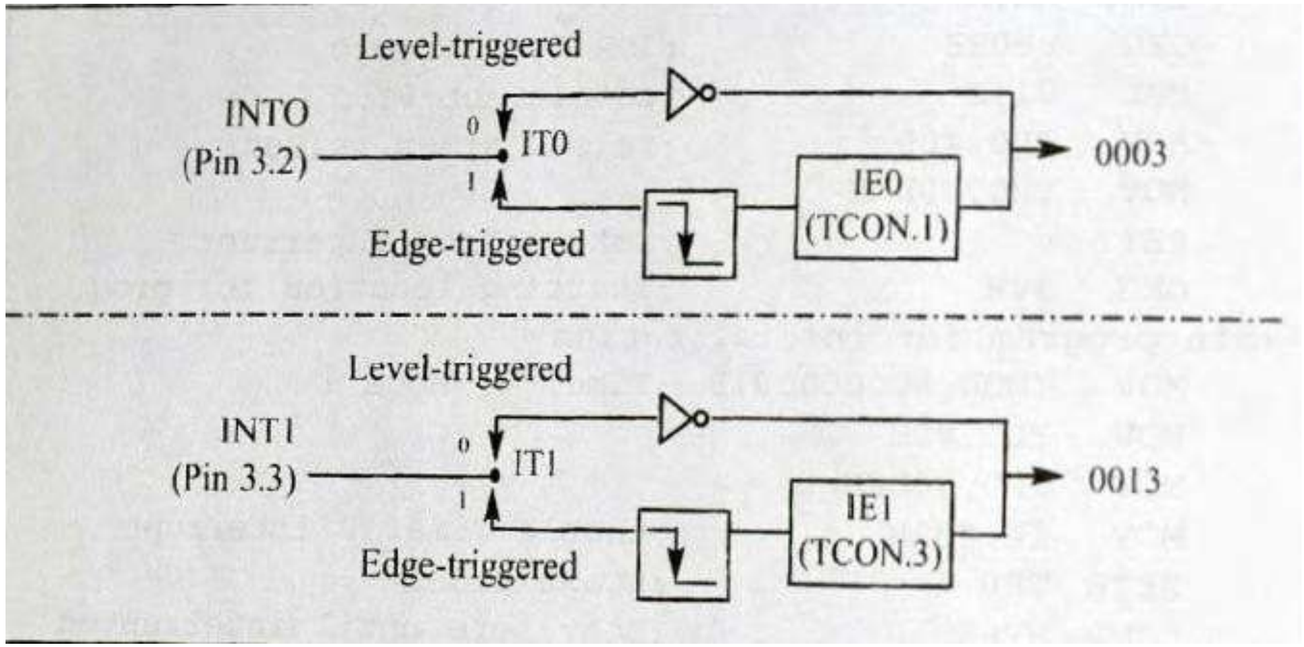
TYPES OF INTERRUPT

Level-Triggered Interrupt

Edge -Triggered Interrupt

LEVEL TRIGGERED INTERRUPTS

In this mode, INT0 and INT1 are normally high and if the low level signal is applied to them, it triggers the Interrupt. Then the microcontroller stops and jumps to the interrupt vector table to service that interrupt.



EDGE TRIGGERED INTERRUPTS

The low-level signal at the INT pin must be removed before the execution of the last instruction of the ISR, RETI.
Otherwise, another interrupt will be generated. This is called a level-triggered or level-activated.

EDGE -TRIGGERED INTERRUPT

Upon reset 8051 makes INT0 and INT1 low l Level-Triggered Interrupt. To make them Edge -Triggered Interrupt, we must program the bits of the TCON Register.
The TCON register holds among other bits and IT0 and IT1 flags bit the determine level- or edge triggered mode. IT0 and IT1 are bits D0 (TCON.0) and D2(TCON.2) of the TCON Register respectively.

SERIAL COMMUNICATION INTERRUPTS

TI (transfer interrupt) is raised when the stop bit is transferred indicating that the SBUF register is ready to transfer the next byte.
RI (received interrupt) is raised when the stop bit is received indicating that the received byte needs to be picked up before it is lost (overrun) by new incoming serial data.
In the 8051 there is only one interrupt set aside for serial communication ,used for both sending and receiving data.
If the interrupt bit in the IE register (IE.4) is enabled, when RI or TI is raised the 8051 gets interrupted and jumps to memory location 0023H to execute the ISR.
In that ISR we must examine the TI and RI flags to see which one caused the interrupt and respond accordingly.

THANK YOU