SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECT312 – EMBEDDED SYSTEM DESIGN

III YEAR/ VI SEMESTER

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UNIT 1 – **INTRODUCTION TO EMBEDDED SYSTEMS**

TOPIC 2 –1.6 – CISC ARCHITECTURE

CISC ARCHITECTURE

What is CISC….?

A complex instruction set computer (CISC, pronounced like "*sisk*") is a microprocessor instruction set architecture (ISA) in which each instruction can execute several low-level operations, such as a load from memory, an arithmetic operation, and a memory store, all in a single instruction.

CISC ARCHITECTURE

Main Idea of CISC

- Hardware is always faster than software, therefore one should make a powerful instruction set, which provides programmers with assembly instructions to do a lot with short programs.
- So the primary goal of the CISC is to complete a task in few lines of assembly instruction as possible.

CISC ARCHITECTURE

- Memory in those days was expensive
  - ✓ bigger program->more storage->more money

Hence needed to *reduce the number of instructions per program*

- Number of instructions are reduced by having *multiple operations* within a single instruction
- Multiple operations lead to many different kinds of instructions that access memory
  - ✓ In turn making instruction length variable and fetch-decode execute time unpredictable – making it more complex
  - ✓ Thus hardware handles the complexity

CISC ARCHITECTURE

CISC philosophy

➢ Use microcode

- Used a simplified microcode instruction set to control the data path logic.

This type of implementation is known as a **microprogrammed implementation.**

➢ Build rich instruction sets

•Consequences of using a micro programmed design is that designers could build more functionality into each instruction.

➢ Build high-level instruction sets

•The logical next step was to build instruction sets which map directly from high-level languages

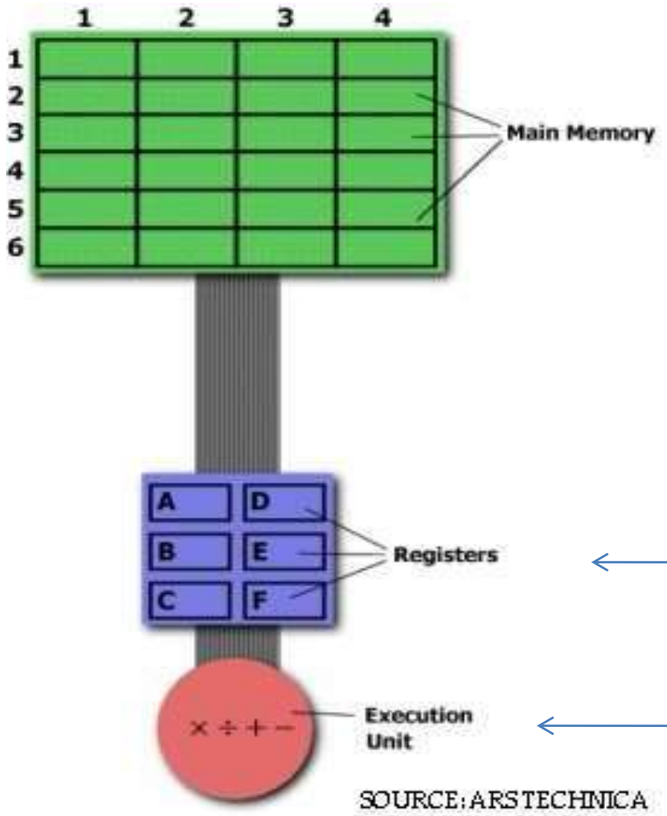
CISC ARCHITECTURE

Characteristics of a CISC design

- Register to register, register to memory, and memory to register commands.
- Uses Multiple addressing modes .
- Variable length instructions where the length often varies according to the addressing mode
- Instructions which require multiple clock cycles to execute.

CISC ARCHITECTURE

CISC Vs. RISC



Main memory

Memory (1,1) .. (6,4) = 24 locations

General purpose registers

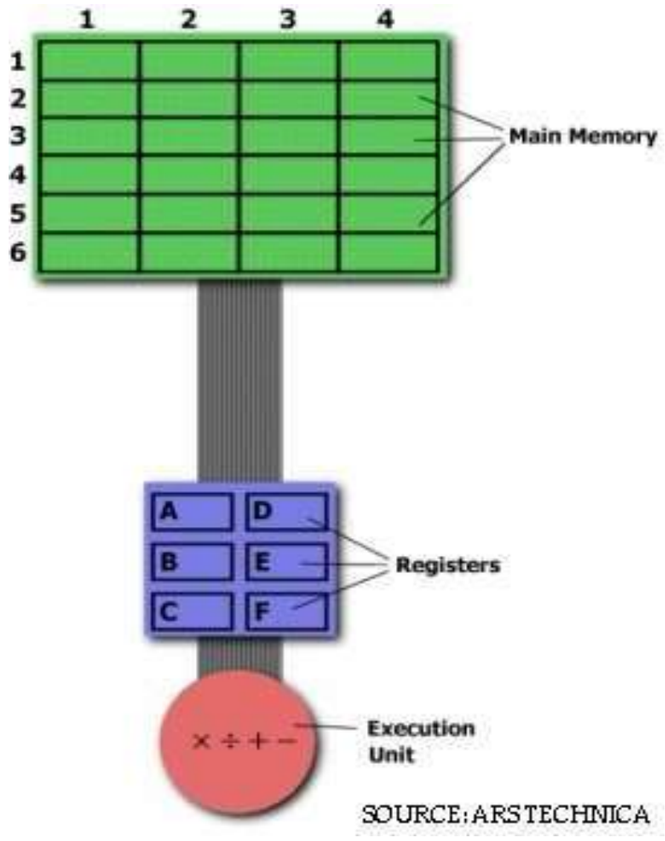
Registers: A,B,C,D,E,F

Arithmetic Logical Unit

Execution unit : arithmetic (+ -* ÷)

CISC ARCHITECTURE

Consider the operation of Multiplication



- Let's say we want to find the product of two numbers - one stored in location 2:3 and another stored in location 5:2 - and then store the product back in the location 2:3.
- i.e.,

M(2,3)<- M(5,2)*M(2,3)

CISC ARCHITECTURE

CISC Approach

For this particular task, a CISC

- processor would come prepared with a specific instruction (we'll call it "MULT").

MULT A,B

When executed, this instruction

- loads the two values into separate registers,
- multiplies the operands in the execution unit, and then
- stores the product in the appropriate register.

entire task of multiplying two numbers can be completed with one instruction

- MULT is what is known as a "complex instruction."
- It operates directly on the computer's memory banks and does not require the programmer to explicitly call any loading or storing functions.
- It closely resembles a command in a higher level language, identical to the C statement "a = a * b."

CISC ARCHITECTURE

RISC Approach

- RISC processors only use simple instructions that can be executed within one clock cycle.
- The "MULT" command described above could be divided into three separate commands:

LOAD A, 2:3

LOAD B, 5:2

PROD A, B ("PROD,"finds the product of two operands)

STORE 2:3, A ("STORE,“ moves data from a register to the memory banks)

CISC ARCHITECTURE

CISC

- Primary goal is to complete a task in as few lines of assembly as possible
- Emphasis on hardware
- Includes multi-clock complex instructions
  - Memory-to-memory: "LOAD" and "STORE" incorporated in instructions
- Difficult to apply pipelining.
- Small code sizes, high cycles per second

RISC

- Primary goal is to speedup individual instruction
- Emphasis on software
- Single-clock, reduced instruction only
- Register to register: "LOAD" and "STORE" are independent instructions
- Easy to apply pipelining.
- Low cycles per second, large code sizes

CISC ARCHITECTURE

The Performance Equation

- The following equation is commonly used for expressing a computer's performance ability:

$$\frac{\text{time}}{\text{program}} = \frac{\text{time}}{\text{cycle}} \times \frac{\text{cycles}}{\text{instruction}} \times \frac{\text{instructions}}{\text{program}}$$

cisc

Risc

The CISC approach attempts to minimize the number of instructions per program, sacrificing the number of cycles per instruction.

RISC does the opposite, reducing the cycles per instruction at the cost of the number of instructions per program.

CISC ARCHITECTURE

Which one is better...?

- There is still considerable controversy among experts about which architecture is better.

Some say that RISC is cheaper and faster and therefore the architecture of the future.

Others note that by making the hardware simpler, RISC puts a greater burden on the software.

Software needs to become more complex. Software developers need to write more lines for the same tasks.

CISC ARCHITECTURE

No Big Difference Now!

- RISC and CISC architectures are becoming more and more alike.
- Many of today's RISC chips support just as many instructions as yesterday's CISC chips. The PowerPC 601, for example, supports *more* instructions than the Pentium. Yet the 601 is considered a RISC chip, while the Pentium is definitely CISC.
- Further more today's CISC chips use many techniques formerly associated with RISC chips
- So simply said: RISC and CISC are growing to each other

CISC ARCHITECTURE

Recent Developments & Future Scope

EPIC :

- The biggest threat for CISC and RISC might not be each other, but a new technology called EPIC. **Explicitly Parallel Instruction Computing.**
- EPIC can do many instruction executions in parallel to one another.
- EPIC is a created by Intel and is in a way a combination **of both CISC and RISC.**
    - This will in theory allow the processing of **Windows-based a**s well as **UNIX-based** applications by the same CPU.
- Intel is working on it under code-name ***Merced*.**
- Microsoft is already developing their Win64 standard for it. Like the name says, Merced will be a 64-bit chip.

CISC ARCHITECTURE

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