



DMA Controller is a hardware device that allows I/O devices to directly access memory with less participation of the processor. DMA controller needs the same old circuits of an interface to communicate with the CPU and Input/Output devices.

#### *What is a DMA Controller?*

Direct Memory Access uses hardware for accessing the memory, that hardware is called a DMA Controller. It has the work of transferring the data between Input Output devices and main memory with very less interaction with the processor. The direct Memory Access Controller is a control unit, which has the work of transferring data.

#### *DMA Controller Diagram in Computer Architecture*

DMA Controller is a type of control unit that works as an interface for the data bus and the I/O Devices. As mentioned, DMA Controller has the work of transferring the data without the intervention of the processors, processors can control the data transfer. DMA Controller also contains an address unit, which generates the address and selects an I/O device for the transfer of data. Here we are showing the block diagram of the DMA Controller.

<https://media.geeksforgeeks.org/wp-content/uploads/20230509110159/DMA-Controller-660.webp>

#### *Block Diagram of DMA Controller*

#### *Types of Direct Memory Access (DMA)*

There are four popular types of DMA.

- Single-Ended DMA
- Dual-Ended DMA
- Arbitrated-Ended DMA
- Interleaved DMA

**Single-Ended DMA:** Single-Ended DMA Controllers operate by reading and writing from a single memory address. They are the simplest DMA.

**Dual-Ended DMA:** Dual-Ended DMA controllers can read and write from two memory addresses. Dual-ended DMA is more advanced than single-ended DMA.

**Arbitrated-Ended DMA:** Arbitrated-Ended DMA works by reading and writing to several memory addresses. It is more advanced than Dual-Ended DMA.

**Interleaved DMA:** Interleaved DMA are those DMA that read from one memory address and write from another memory address.

#### *Working of DMA Controller*

The DMA controller registers have three registers as follows.

- **Address register** – It contains the address to specify the desired location in memory.
- **Word count register** – It contains the number of words to be transferred.
- **Control register** – It specifies the transfer mode.

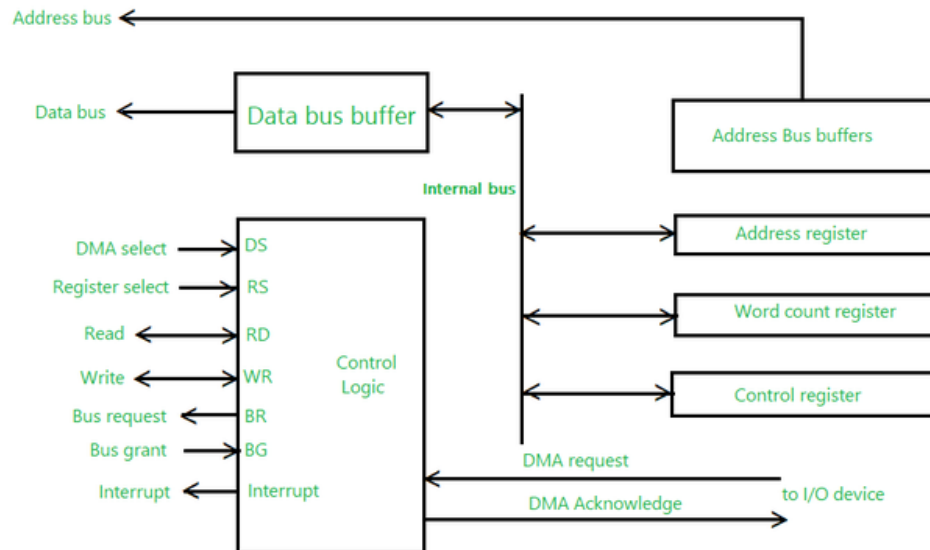
**Note:** All registers in the DMA appear to the CPU as I/O interface registers. Therefore, the CPU can both read and write into the DMA registers under program control via the data bus.

The figure below shows the block diagram of the DMA controller. The unit communicates with the CPU through the data bus and control lines. Through the use of the address bus and allowing the



DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

DMA and RS register to select inputs, the register within the DMA is chosen by the CPU. RD and WR are two-way inputs. When BG (bus grant) input is 0, the CPU can communicate with DMA registers. When BG (bus grant) input is 1, the CPU has relinquished the buses and DMA can communicate directly with the memory.



Working Diagram of DMA Controller

**Explanation:** The CPU initializes the DMA by sending the given information through the [data bus](#).

- The starting address of the memory block where the data is available (to read) or where data are to be stored (to write).
- It also sends word count which is the number of words in the memory block to be read or written.
- Control to define the mode of transfer such as read or write.
- A control to begin the DMA transfer

**Modes of Data Transfer in DMA**

There are 3 [modes of data transfer](#) in DMA that are described below.

- **Burst Mode:** In Burst Mode, buses are handed over to the CPU by the DMA if the whole data is completely transferred, not before that.
- **Cycle Stealing Mode:** In Cycle Stealing Mode, buses are handed over to the CPU by the DMA after the transfer of each byte. Continuous request for bus control is generated by this Data Transfer Mode. It works more easily for higher-priority tasks.
- **Transparent Mode:** Transparent Mode in DMA does not require any bus in the transfer of the data as it works when the CPU is executing the transaction.

**8237 DMA Controller**

[8237 DMA Controller](#) is a type of DMA Controller which has a flexible number of channels but generally works on 4 Input-Output channels. In these present channels, the channel has to be given the highest priority to be decided by the Priority Encoder. Each channel in the 8237 DMA Controller has to be programmed separately.



SNS COLLEGE OF TECHNOLOGY, COIMBATORE –35  
(An Autonomous Institution)



DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

**8257 DMA Controller**

8257 DMA Controller is a type of DMA Controller, that when a single Intel 8212 I/O device is paired with it, becomes 4 channel DMA Controller. In 8257 DMA Controller, the highest priority channel is acknowledged. It contains two 16-bit registers, one is DMA Address Register and the other one is Terminal Count Register.

**Advantages of DMA Controller**

- Data Memory Access speeds up memory operations and data transfer.
- CPU is not involved while transferring data.
- DMA requires very few clock cycles while transferring data.
- DMA distributes workload very appropriately.
- DMA helps the CPU in decreasing its load.

**Disadvantages of DMA Controller**

- Direct Memory Access is a costly operation because of additional operations.
- DMA suffers from [Cache-Coherence Problems](#).
- DMA Controller increases the overall cost of the system.
- DMA Controller increases the complexity of the software.