Reg.No:


SNS College of Technology, Coimbatore-35.
(Autonomous)
B.E/B.Tech- Internal Assessment -I

B Academic Year 2023-2024(ODD)

Third Semester
Computer Science and Engineering

## 19ITT202 Computer Organization and Architecture

 [Common to CSE \& IT]Time: 1.5 Hours
Maximum Marks: 50
Answer All Questions

PART - A (5x $2=10$ Marks)

1. List out the components of functional units of Computer.
2. Consider the $\mathrm{C} \leftarrow[\mathrm{A}]+[\mathrm{B}]$ operation to be performed, write the sequence of instructions to be executed to perform the operation without destroying the former contents of location A and B , with respect to one, two \& three address instruction.

Define Bus and label different types of buses used.
If computer A runs a program in 10 seconds and computer B runs the same program in 15 seconds. How much faster is A than B.

Find 1's and 2's Complement of 1100

## PART - B (13+13+14=40 Marks)

6. (a) Summarize the functional units of computer by extending the 13 CO1 Und basic operational concepts.
(or)
(b) Illustrate the execution of straight-line sequencing \& 13 CO1 App branching instruction. Construct \& compare the sequence of instruction to be performed for adding n numbers in both sequencing \& branching instruction.
7. (a) Interpret different addressing modes and experiment all modes by assuming the addition operation of N numbers to be performed and saved in SUM.

## (or)

(b) Identify the concept of addition and subtraction of signed $13 \quad \mathrm{CO} 2$ Ana numbers and examine the usage of each level in a problem.
8. (a) Registers R1 and R2 of a computer contain the decimal values $14 \quad \mathrm{CO} 1 \quad \mathrm{App}$ 1200 and 4600. In each of the following instructions determine the Addressing mode used in the instruction and find the effective address of the memory operand?
a) Load $20(\mathrm{R} 1), \mathrm{R} 5$
b) Move \#3000,R5
c) Store R5,30(R1,R2)
d) Add -(R2),R5
e) Subtract (R1)+,R5
(or)
(b) Design and inspect the operation of Full Adder by 14 CO2 Und constructing full adder using 2 half adders.

