

# SNS COLLEGE OF TECHNOLOGY



## (An Autonomous Institution)

#### **COIMBATORE-35**

#### **DEPARTMENT OF COMPUTER SCIENE AND ENGINEERING**

### **COMPUTER ORGANIZATION AND ARCHITECTURE**

#### **Multiple Choice Questions with Answers**

1. What would be the minterm expansion of the following:

$$f(P, Q, R) = PQ + QR' + PR'$$

a. 
$$m0 + m1 + m3 + m5$$

b. 
$$m2 + m4 + m6 + m7$$

c. 
$$m2 + m3 + m4 + m5$$

$$d. m0 + m1 + m6 + m7$$

**Answer:** (b) m2 + m4 + m6 + m7

**2.** What is the hexadecimal representation of 6578?

a. D71

b. 32F

c. 1AF

d. D78

Answer: (c) 1AF

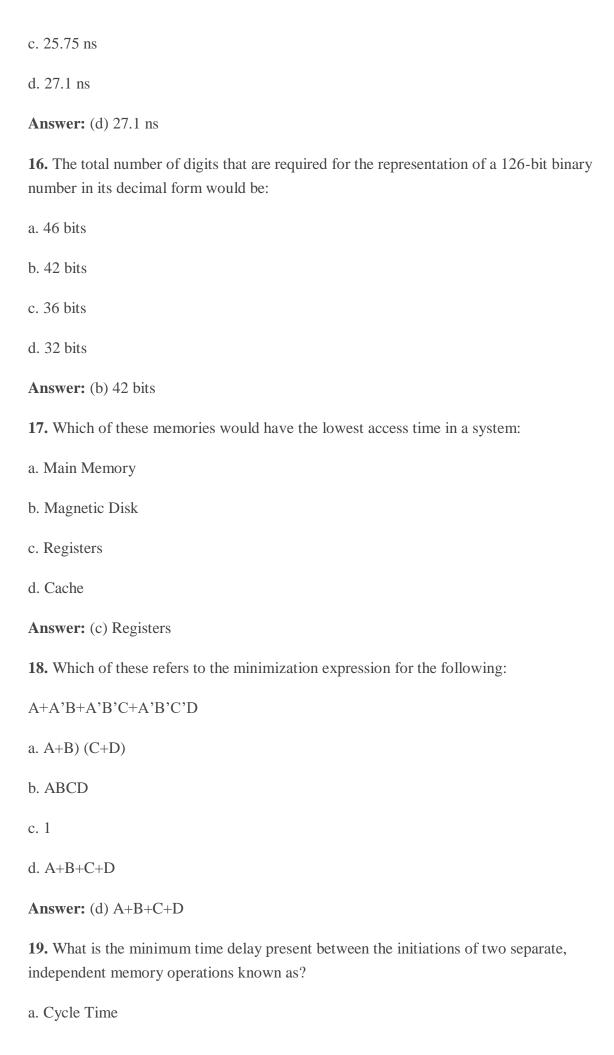
**3.** Let us consider an array multiplier used for the multiplication of two n bit numbers. In case every gate in the circuit faces a unit delay, then the total delay of this multiplier would be:

- a.  $\Theta(n)$
- b.  $\Theta(1)$
- c. Θ(n^2)
- d.  $\Theta(\log n)$

Answer: (a) $\Theta(n)$
<b>4.</b> What would be the total prime implicants of the following function:
$f(w, x, y, z) = \Sigma(0, 2, 4, 5, 6, 10)$
a. 5
b. 4
c. 3
d. 2
<b>Answer:</b> (c) 3
<b>5.</b> How many pulses do we need if we want to change the contents of any given 8-bit up counter from the bit 10101100 to bit 00100111 (the rightmost bit here is the LSB)?
a. 123
b. 124
c. 133
d. 134
<b>Answer:</b> (a) 123
<b>6.</b> When we add a two's complement, 4-bit, binary numbers 1101 and 0100, it would result in:
a. 1001 and no overflow
b. 0001 and an overflow
c. 1001 and an overflow
d. 0001 and no overflow
Answer: (d) 0001 and no overflow
7. If we want to put an 8085 microprocessor in a wait state, then we have:
a. to raise the-HOLD input
b. to raise the READY input
c. to lower the HOLD input

d. to lower the READY input
<b>Answer:</b> (d) to lower the READY input
<b>8.</b> What would be the 2's complement representation (in hexadecimal) of (-539)10?
a. 9E7
b. DE5
c. DBC
d. ABE
Answer: (b) DE5
<b>9.</b> What would be the 2's complement representation of the -15 decimal value?
a. 10001
b. 1111111
c. 1001
d. 1111
<b>Answer:</b> (d) 1111
<b>10.</b> If in a base-x type of number system, 73x is equivalent to that of 54y in a base-y type of number system, then the possible values of both- x and y would be:
a. 10, 12
b. 8, 16
c. 8, 11
d. 9, 13
<b>Answer:</b> (c) 8, 11
11. In the Principle of locality, there is a justification of the use of:
a. DMA
b. Cache memory
c. Threads

d. Interrupts
Answer: (b) Cache memory
12. Which of these is NOT involved in the case of a memory write operation?
a. Databus
b. MDR
c. MAR
d. PC
Answer: (d) PC
13. Which of these is required when we want to establish the communication links between a CPU and its peripherals?
a. Memory data register
b. Memory address register
c. Instruction register
d. Index register
Answer: (a) Memory data register
<b>14.</b> A given 2 level memory consists of a 30 ns average access time. If the cache, as well as the memory access time here, is 20 ns and 150 ns, respectively, what would be the hit ratio?
a. 99%
b. 70%
c. 93%
d. 80%
<b>Answer:</b> (c) 93%
<b>15.</b> If we double the cache line length and it reduces the miss rate to 3%, then by how much will the average memory access time be reduced?
a. 4.85 ns
b. 22.2 ns



b. Latency Time
c. Access Time
d. Transfer Rate

Answer: (a) Cycle time

20. Which of these addressing modes is the most suitable for some high-level language statements?
a. Indexed
b. Auto-decrement
c. Auto-increment
d. Displacement

Answer: (b) Auto-decrement
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