UNIT I TRANSISTOR BIASING CIRCUITS

Part - A

1. **Why CE configuration is widely used in amplifier circuits?**
   - The CE configuration is the only configuration which provides both voltage gain as well as current gain greater than unity. In case of CB configuration current gain is less than unity and in case of CC configuration voltage gain is less than unity. The power gain of the CE amplifier is much greater the other two (CB &CC) configurations.
   - In a common emitter circuit, the ratio of output resistance to input resistance is small, may range 10Ω to 100 Ω. Hence coupling between various transistor stages becomes efficient.

2. **Define dc biasing.**

   In order to operate transistor in the desired region we have to apply external dc voltages of correct polarity and magnitude to the two junctions of the transistor. This is nothing but the biasing of the transistor. Since the dc voltages are used to bias the transistor, biasing is known as dc biasing of the transistor.

3. **What is meant by quiescent point?**

   When we bias a transistor we establish a certain current and voltage conditions for the transistor. These conditions are known as operating conditions or dc operating point or quiescent point.

4. **Why biasing is necessary in BJT amplifiers?**
   - We have to apply external dc biasing of correct polarity and magnitude to the two junctions of the transistor, to operate it in the desired region.
   - The dc biasing supplies the power to the transistor circuit to get the output signal power greater than input signal power.

5. **Why do you fix the operating point in the middle of the load line?**

   When transistor is used as an amplifier, the Q point should be selected at the center of the dc load line to prevent any possible distortion in the amplified output signal.

6. **What is meant by bias stability?**

   While designing the biasing circuit, care should be taken so that the operating point will not shift into an undesirable region. Designing the biasing circuit to stabilize the Q-point is known as bias stability.

7. **What are the requirements of a biasing circuit?**
   - The transistor should be operated in the middle of the active region or operating region should be fixed at the center of the active region.
   - The circuit design should provide a degree of temperature stability.

- The operating point should be made independent of the transistor parameters.

8. What is thermal runaway?

The increase in the collector current increases the power dissipated at the collector junction. This in turn further increases the temperature of the junction and hence increases collector current. The process is cumulative. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called thermal runaway of the transistor.

9. Define stability factor. What is its ideal value?

Stability factor indicates degree of change in operating point due to variation in temperature. Ideally, it should be zero to keep the operating point stable.

10. What is d.c load line?

The d.c load line is defined as a line on the output characteristics of the transistor which gives the value of Ic & Vce corresponding to zero signal condition.

11. Name the two techniques used in the stability of the q point and explain.

1. Stabilization techniques: This refers to the use of resistive biasing circuit which allows IB to vary so as to keep IC relatively constant with variations in Ico, β, and VBE.

2. Compensation techniques: This refers to the use of temperature sensitive devices such as transistors, thermistors and diodes. It provides compensating voltages &currents to maintain operating point constant.

12. Give the expression for stability factor.

$S= (1+ \beta)/ [(1- \beta (\partial I_B/ \partial I_C)]$

13. List out the different types of biasing.

- Fixed bias
- Voltage divider or self bias
- Collector feedback bias

14. What are the advantages of fixed bias circuit?

- This is a simple circuit which uses very few components.
- The operating point can be fixed anywhere in the active region of the characteristics by simply changing the value of R_B. Thus, it provides maximum flexibility in the design.

15. What are the limitations of fixed bias circuit?

- This circuit does not provide any check on the collector current which increases with rise in temperature, i.e. thermal stability is not provided by this circuit. So operating point is not maintained.

- Since IC= β I_B and I_B is already fixed; IC depends on β which changes unit to unit and shifts the operating point. Thus stabilization of operating point is very poor in the fixed bias circuit.

16. What is the use of JFET as a voltage variable resistor?

The region before pinch off voltage, drain characteristics is linear. In this region the FET is useful as a voltage controlled resistor, i.e., the drain to source resistance is controlled by the bias voltage. The operation of FET in this region is useful in most linear applications of FET. In such an application the FET is also referred to as a voltage variable resistor.

17. What is thermal resistance and temperature compensation?

The Θ, which is constant of proportionality, is referred to as thermal resistance.

$\Theta = (T_J - T_A)/P_D$

Where, P_D is power dissipated, T_j and T_A are Junction temperature and ambient temperature respectively.

Temperature compensation is the method to keep V_{BE} & I_{CO} as constant during temperature changes.

18. State the advantages of self bias over other types of biasing?

It has the smallest value of S among the three biasing circuits. This shows that the stability is highest for the self bias circuit.

- It is possible to avoid the loss of signal gain by connecting an emitter bypass capacitor across R_E.
- RE introduces negative feedback for compensating the change in I_C.

19. Define reverse saturation current (Ico).

When emitter is open circuited, the base and collector act as a reverse biased diode, and the collector current Ic equals the reverse saturation current (Ico).

20. What are the various BJT configurations?

- Common Base configuration.
- Common Emitter configuration.
- Common Collector configuration.

21. Give the term for Reverse leakage current in Common Emitter configuration.

$I_{CEO} = (\beta_{dc} I_B + 1) I_{CBO}$.

22. Write any one application of FET as a voltage divider resistor?

` The voltage variable resistor property of FET can be used to vary the voltage gain of a multistage amplifier A as the signal level increased. This action is called automatic gain control.

23. Give the relation between S and S''.

$S'' = I_C/\beta\ (S/\ (1+\beta\ ))$

24. What are the various Compensation Techniques?

- Diode Compensation
- Thermistor Compensation
- Sensistor Compensation

25. What are the various reasons for increase in Collector – Base Junction temperature?

a. Due to rise in ambient Temperature.
b. Due to self heating

26. What is the advantage of using emitter resistance in the context of biasing?

If the collector current increases due to the change in temperature or change in ß, the emitter current I_E also increases and the voltage drop across **emitter resistance** R_E increases, reducing the voltage difference between base and emitter.

Due to reduction in V_{BE}, I_B and hence I_C also reduces. Therefore we can say that negative feedback exists in the circuit. The reduction in I_C compensates for the original change in I_C.

27. Why thermal runaway is not occurring in FET?

In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET.

28. Define the various stability factors.

Since there are three variables which are temperature dependent, we can define three stability factors as below:

i. $S = \partial I_C / \partial I_{CO;\ VBE,\ \beta\ const}$
ii. $S = \partial I_C / \partial V_{BE\ ;\ ICO,\ \beta\ const}$
iii. $S = \partial I_C / \partial\ ß\ ;\ ;\ ICO,\ VBE\ const$

Part – B

1) i) Draw the circuit diagram of voltage divider bias circuit using CE configuration and explain how it stabilizes the operating point. Derive the stability factor of it.(10)
ii) Explain bias compensation using sensistors. (6) **Nov/dec 2005**

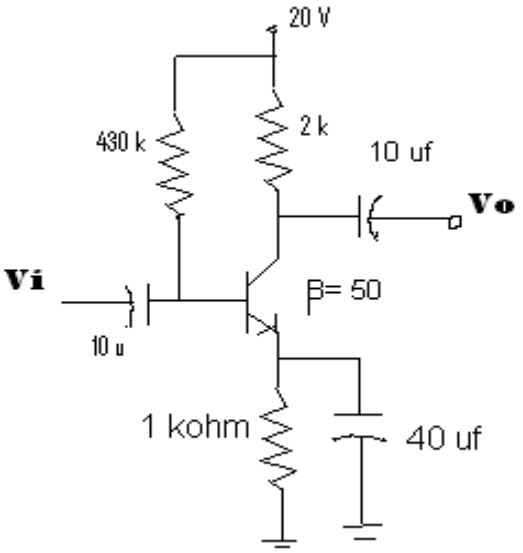
2) i) What is the need for stabilization? Explain.(8) **Nov/dec 2008**
ii) Explain how a field effect transistor can be biased.(8)

3) i) List out the advantages and various properties of FETs.(10)
ii) Draw the biasing circuit for MOSFET using a common source configuration and explain.(6) **Nov/dec 2008**

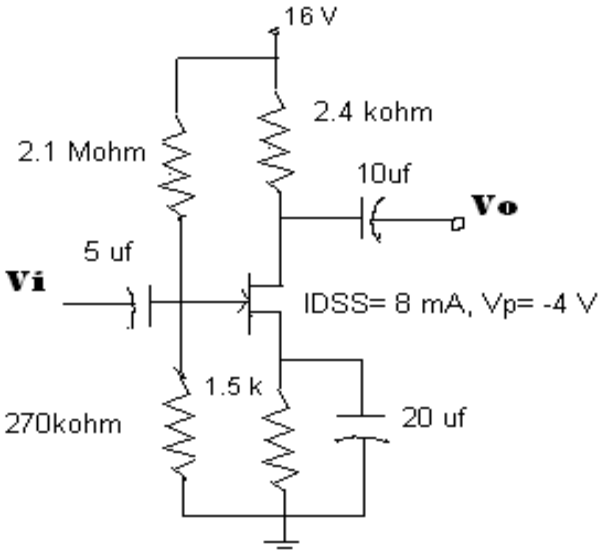
4) i) In fixed bias compensation method a silicon transistor with β=100 is used. V_{CC} = 6V, R_C= 3 kΩ, R_B = 530 kΩ. Draw the dc load line and determine the operating point. What is the stability factor? (8)
ii) Draw a circuit which uses a diode to compensate for changes in Ico. Explain how stabilization is achieved in the circuit. (8) **Nov/dec 2010**

5) i) Calculate the values of R_1 and R_C in the voltage divider bias circuit so that Q point is at V_{CE} =6V and I_C= 2 mA. Assume transistor parameter as α=0.985, I_{CBO}= 4 μA and V_{BE}= 0.2 V.
ii) Determine the stability factor for a CB amplifier circuit. **Nov/dec 2010**

6) For the emitter bias network of figure determine I_B, I_C, V_{CE}, V_C, V_E, V_B, and V_{BC}. (16) **May/jun 2009**



7) Determine I_{DQ}, V_{GSQ}, V_D, V_S, V_{DS}, and V_{DG} for the network of fig. **May/jun 2009**



8) i) Illustrate how dc and ac load lines are plotted and explain their significance. (8)
ii) Describe the effect on Q point due to variation in β and temperature. (8) **Apr/may 2011**

9) Draw the circuit of a CE amplifier with self bias and obtain the expression for stability factor of the circuit. Explain how the circuit is an improvement over the other bising circuits.(16)

10) Discuss about diode and thermistor compensation techniques.

11) Draw the collector to base bias circuit. Why it is called so? Derive an expression for its stability factor

12) Discuss the different types of biasing circuits in FET.

13) What is the need for biasing BJT? Explain the different types of biasing circuits. **Nov/dec 2006** (16)

14) i) What is dc load line? How will you select the operation point? Explain it using CE amplifier characteristics as an example.(8)
ii) Explain the voltage divider bias circuit for n-channel JFET give its dc analysis.(8)

15) i) Derive the expressions for the various stability factors. (12)
ii) Draw the source self bias and voltage divider bias circuit for FET. (4)

16) Define three stability factors. Derive and explain the condition to avoid thermal runaway **Apr/may 2011**

17) i) Draw and explain base bias with collector feedback circuit. Derive an expression for stability (6)
ii) With neat diagram, explain the working of thermistor and sensistor compensation circuit. (6)

UNIT II BJT AND FET AMPLIFIERS

Part – A

1. What is the use of the coupling capacitor?

It is used to block the dc signal to the transistor amplifier. It allows ac & blocks the dc.

2. What is the necessary of the bypass capacitor?

An emitter bypass capacitor C_E is connected in parallel with the emitter resistance, R_E to provide a low reactance path to the amplified ac signal. If it is not inserted, the amplified ac signal passing through R_E will cause a voltage drop across it. This will reduce the output voltage, reducing the gain of the amplifier.

3. Define the four h-parameters.

(i) $h_{11} = V_i / I_i \quad |_{V0=0}$ Input resistance with output short-circuited. In oms.

(ii) $h_{12} = V_i / V_o \quad |_{Ii=0}$ Fraction of output voltage at input with input open circuited.

(iii) $h_{21} = I_o / I_i \quad |_{V0=0}$ Forward current transfer ratio or current gain with output short circuited.

(iv) $h_{22} = I_o / V_o \quad |_{Ii=0}$ Output admittance with input open circuited, in mhos.

4. Write the benefits of h-parameters?

- Real numbers at audio frequencies.
- Easy to measure.
- Can be obtained from the transistor static characteristic curves.
- Convenient to use in circuit analysis and design.

5. What is meant by impedance matching?

It means that making the input impedance is equal to the output impedance by providing a matching transformer to transfer the maximum power between input and output.

6. What are the advantages of transformer coupled amplifiers.

- It provides excellent impedance matching, thus voltage and power gains are improved.
- Higher voltage gain
- DC biasing of individual stages will remain unchanged even after the cascading.

7. What are the features of differential amplifiers?

- High differential voltage gain
- Low common mode gain
- High CMRR
- Large bandwidth

- Low output impedance

8. What do you mean by cascode connection?

The cascade amplifier stage consists of a common emitter amplifier stage in series with the common base amplifier stage. It is one approach to solve the low impedance problem of a common base circuit.

9. What is the overall current gain for a cascode connection?

Overall current gain

(Ais)= $Io/I_s = I_o/I_{c2} * I_{c2}/I_{e2} * I_{e2}/I_{c1} * I_{c1}/I_{b1} * I_{b1}/I_s$

10. What are the advantages of direct coupled amplifiers?

- It does not use any frequency dependent coupling.
- It can amplify low frequency signals down to zero frequency.
- Its cost is very low.

11. What do you mean by multistage amplifier?

When the amplification of a single stage amplifier is not sufficient or when the input or output impedance is not of the correct magnitude for a particular application two or more amplifier stages are connected in cascade. Such amplifier with two or more stages is known multistage amplifier.

12. What are the different methods of coupling?

For the coupling different types of coupling elements can be employed.

- RC coupling
- Transformer coupling
- Direct coupling

13. What is meant by cascaded amplifier?

In cascaded amplifier, the stages are connected such that output of the first stage is connected to the input of the second stage.

14. What are the features of cascode amplifier?

The cascade amplifier gives the high input impedance of a common emitter amplifier as well as the good voltage gain and high frequency performance of a common base circuit.

15. What is meant by bootstrapping?

Bootstrapping is the technique named from the fact that if one end of resistor changes in voltage, the other also moves through the same change in voltage, it acts as if R is pulling itself up by its bootstraps.

16. Mention two advantages which are specific to Darlington connection.

1. It provides high input impedance.
2. Improves current gain.

17. What are the advantages of cascade amplifier?

- Cascade amplifier has a very high bandwidth thus it can be used to amplify the TV signals.
- High voltage gain
- The current gain and power gain of this configuration is very large.
- Flexibility of operation

18. Define CMRR.

It is defined as the ratio of the differential mode voltage gain to the common mode voltage gain.

CMRR= $|A_d / A_c|$

19. What is the need for constant current source for differential amplifier.

The necessity for constant current source for differential amplifier is to increase the CMRR without changing the quiescent current.

20. What is a differential amplifier?

An amplifier which amplifies the difference between the two input signals is called the differential amplifier.

21. What are the different configurations of differential amplifier?

- Dual input, balanced output.
- Dual input, unbalanced output
- Single input, balanced output
- Single input, unbalanced output.

22. State miller's theorem.

If Z is the impedance connected between two nodes, node1 and node 2, it can be replaced by two separate impedances Z1 and Z2; where Z1 is connected between node 1 and ground and Z2 is connected between node 2 and ground.

23. Why Re is replaced by a constant current bias in a differential amplifier?

The emitter supply VEE used for biasing purpose must become larger as Re is increased in order to maintain the quiescent current at its proper value. If the operating currents of the transistors are allowed to decrease, this will lead to higher hie values and will tend to decrease CMRR. To overcome this practical limitations Re is replaced by a constant current bias.

24. Write the equation from which the small signal low frequency equivalent circuit of JFET is formed.

$\Delta Id = g_m \Delta V_{GS}$

The change in drain current due to change in gate to source voltage can be determined using the transconductance factor gm.

Part - B

1) Draw the small signal equivalent circuit of a CS n-channel JFET. Analyze the circuit and obtain its input, output impedance and voltage gain. (16) **Apr/may 2011**

2) i) Draw the circuit diagram of an emitter coupled differential amplifier and explain its working. (8)

ii) Explain and derive the expression for the differential mode gain, common mode gain and CMRR. (8) **Apr/may 2011**

3) i) with mathematical substantiation draw the basic circuit of darlington pair and explain. (11) **nov/ dec 2008**

ii) List out the advantages of differential amplifier. (5)

4) i) Explain briefly the circuit operation of differential amplifier. (8) **nov/ dec 2008**

ii) Derive the expressions for CMRR for a small signal model with a common mode input voltage (8)

5) For the CE amplifier, V_{CC} =12 V, R_L= 4.7 kΩ, Re= 1 kΩ, R_1=15 kΩ, R_2= 2.2 kΩ, Rs= 600 kΩ. The transistor has h parameters of h_{fe} = 400 , h_{ie} = 10 kΩ. Assume Ce=50μF with no series resistance. Calculate **Nov/dec 2010**

i) Mid frequency voltage gain Vo/Vs
ii) Mid frequency voltage gain Vo/Vi
iii) fo and fp. If fp>>fo what does this mean?
iv) f1 for Vo/Vs
v) f1 for Vo/Vi (16)

6) Describe the DC analysis and AC analysis of an emitter coupled pair. (16)

7) i) Obtain an expression for current gain of CE amplifier with bypassed emitter resistor making use of exact hybrid model. (10) **nov/dec 2005**

ii) Derive input and output impedance of FET amplifier with the help of small signal model. (6)

8) i) What are the significance of cascode connection with the help of its equivalent circuit , derive Ai, Av, Ri, Ro. (10)

ii) Explain the method of measuring CMRR (6)

9) Derive the expression for the differential and average voltage gain of a dual input dual output differential amplifier and explain the modification done to improve CMRR. **apr/may 2011**

10) Derive the expression for voltage gain, current gain, power gain, input and output impedances for CE BJT amplifier using h parameter analysis.

11) i) Give the guidelines for the analysis of transistor circuit for its small signal behavior. Explain with an example. (8) **nov/dec 2006**

ii) Define CMRR. Explain the methods to improve CMRR. (8)

12) i) With small signal equivalent circuit of emitter follower derive its input impedance, Av, and output impedance. (10)

ii) Employ bootstrapping technique in the emitter follower, derive its input impedance. (6)

13) Derive the expression for the voltage gain of

i) Common emitter amplifier

ii) Common drain amplifier configurations under small signal low frequency conditions. (16) **DEC 2004**

FREQUENCY RESPONSE OF AMPLIFIERS

Part - A

1. What is the relationship between bandwidth and rise time?

We can relate the bandwidth and rise time as follows,

$$BW = 0.35/t_r$$

2. What is the significance of octaves and decades?

The octaves and decades are the measures of change in frequency. A ten times change in frequency is called a decade. An octave corresponds to a doubling or halving of the frequency.

3. Write a note on frequency response curve.

Over the range of frequencies, an amplifier should ideally provide the same amplification for all frequencies. The degree to which this is done is usually indicated by a curve known as frequency response curve of the amplifier. This curve is plot of the voltage gain of an amplifier against the frequency of the signal.

4. Write a note on effects of coupling capacitor.

At medium and high frequencies, the factor f makes Xc very small, so that coupling capacitors behave as short circuits. At low frequencies, Xc increases. This increase in X_C drops the signal voltage across the capacitor and reduces the circuit gain. As signal frequencies decrease, the capacitor reactance increase and circuit gain continues to fall, reducing the output voltage.

5. Write a note on effects of bypass capacitor.

At lower frequencies, the bypass capacitor C_E is not a short. So, the emitter is not at ac ground. X_C in parallel with R_E creates an impedance. The signal voltage drops across this impedance reducing the circuit gain.

6. What is mean by 3 dB frequencies and 3 dB bandwidth?

Voltage gain at f1 and f2 is less than 3 dB of the maximum voltage gain. Due to this, these frequencies are called 3 dB frequencies.

At f1 and f2 power gain drops by 3 dB. For all frequencies within the bandwidth, amplifier power gain is at least half of the maximum power gain. So this bandwidth is referred to as 3 dB bandwidth.

7. Define lower and upper cut-off frequencies for an amplifier.

Lower cut-off frequency:

The frequency (on lower side) at which the voltage gain of the amplifier is exactly 70.7% of the maximum gain is known as lower cut off frequency.

Upper cut-off frequency:

The frequency (on the higher side) at which the voltage gain of the amplifier is exactly 70.7% of the maximum gain is known as upper cut off frequency.

8. Define ά cut off frequency.

It is the frequency at which the transistor's short circuit CB current gain drops by 3db or 1/√2 times from its value at low frequency.

9. Define β cut off frequency.

It is the frequency at which the transistor's short circuit CE current gain drops by 3db or 1/√2 times from its value at low frequency.

10. What are the high frequency effects?

At high frequencies, the coupling and bypass capacitors act as short circuit and do not affect the amplifier frequency response. However at high frequencies, the reactance of junction capacitances is low. They provide shunting effect as they are in parallel with junctions. This reduces the circuit gain and hence the output voltage.

11. For an amplifier, midband gain = 100 and lower cutoff frequency is 1Khz. Find the gain of an amplifier at frequency = 20 Hz.

$A = A_{mid} / \sqrt{(1+(f_1 / f)^2}$

$A= 100 / \sqrt{(1+(1000/20)^2)}$

$=2$

12. If the rise time of a BJT is 35 nano seconds, what is the bandwidth that can be obtained using this BJT?

$$t_r = 0.35/ f_2 = 0.35/BW$$

$$BW = 0.35/ t_r = 10 \text{ Mhz}$$

13. What does the rise time indicate? How it is related to upper 3 dB frequency?

The rise time tr is an indication of how fast the amplifier can respond to a discontinuity in the input voltage. Upper 3 dB frequency can be represented in terms of rise time as

$$f_H = 0.35/t_r$$

14. Define f_T in a high frequency transistor.

It is the frequency at which short circuit CE current gain becomes unity.

15. Define sag and give its relation to lower cutoff frequency.

The amplifiers low frequency RC networks consist of coupling and bypass capacitors make amplifiers output to decrease with large time constant. The output voltage has sag or tilt associated with it.

Sag can be related to lower cutoff frequency as,

$P= (\Pi f_L / f)*100$

16. Define the term bandwidth.

The term bandwidth is defined as the difference between upper and lower cutoff frequencies.

BW= f2- f1

17. Define gain bandwidth product and unity gain frequency.

One of the important characteristic of an amplifier is that the product of its voltage gain and bandwidth is always constant when the roll-off is -20 dB/decade. This product is called as gain-bandwidth product.

The frequency at which the amplifier gain is equal to 1 is called as unity gain frequency.

Part - B

1) i) Draw the hybrid Π- equivalent of BJT and discuss about the high frequency analysis of BJT (8) **Nov/dec 2010**

ii) Write the expressions for frequency response of multistage amplifiers (8)

2) may/june 2009 Explain high frequency analysis of FET with necessary circuit diagrams.(16)

3) i) Derive the expression for common emitter short circuit current gain with resistive load using hybrid Π model (8) **nov/dec 2010**

ii) Write short notes on high frequency response of FET amplifier (4)

4) Derive the expression for the CE short circuit current gain of transistor at high frequency. (16)

5) i) What are the effects of coupling and bypass capacitors on the bandwidth of amplifiers? (8)

ii) Derive the equation for gm which gives their elation between gm, Ic and temperature. (8)

6) Draw the hybrid ∏ - common emitter transistor model and derive the values of the various components in terms of the h parameters. (16)

7) i) Draw the high frequency hybrid ∏ model for a transistor in the CE configuration and explain the significance of each component. (12)

ii) Define alpha cutoff frequency and beta cutoff frequency (4)

8) Discuss about the low frequency response and the high frequency of an amplifier. (16)

9) Discuss the high frequency equivalent circuit of FET and hence derive gain bandwidth product for anyone configuration. **May/june 2012**

10) i) Give the relationship between rise time and upper cutoff frequency (4)

ii) Give the relationship between bandwidth and rise time. (4)

iii) What do you understand by frequency response of an amplifier? How is it plotted? (8)