UNIT- I

Biasing of Discrete BJT and MOSFET

Transistors

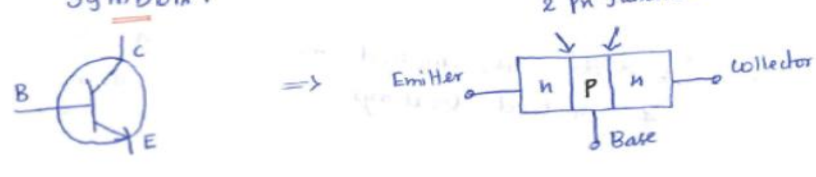
- Unipolar Junction Transistor (UJT) ⇓ The current conduction is only due to one type of carriers ie majority carriers.
- Bipolar Junction Transistor (BJT) ⇓ The current conduction in bipolar transistor is due to both minority and majority carriers.

Bipolar Junction Transistor (BJT)

Construction :

* It's a 3 terminal device → Emitter (E), Base (B) & collector (C)
* Two Basic types
  - npn ⇓ 2 layers of n-type material sandwitching a Thin p-type layer is called npn Transistor
  - pnp ⇒ 2 layer of p-type material sandwitching a Thin n-type layer is called pnp Transistor.
* The Emitter terminal is heavily doped while the base & collector are lightly doped.
* The Thickness of the base layer is ~ 0.06% of that of the emitter (or) collector layer.

Symbols :



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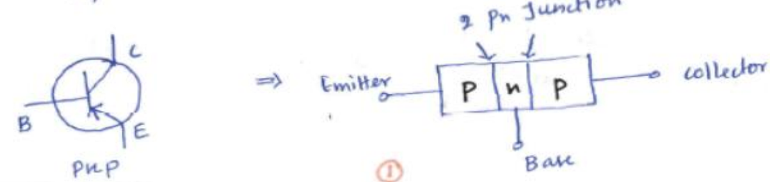

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Operations:

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* The arrow at each Terminals points in the direction of conventional current.

* The current flow out of the E Terminal is referred as Emitter current, which is denoted as I_E.

* the current flow into the B terminal is referred as Base current, which is denoted as I_B & collector terminal current is denoted as I_c.

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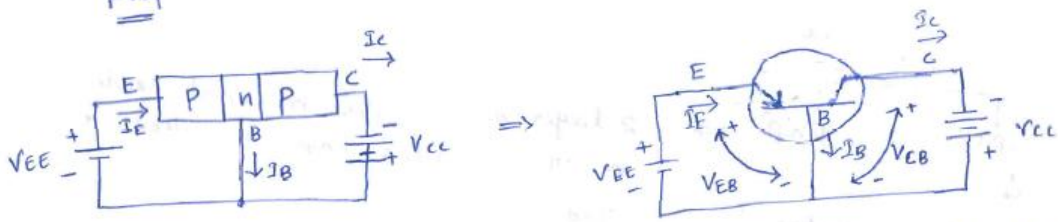


* The current flow into the E Terminal is referred as Emitter current which is denoted as I_E.

* The current flow out of the B & C terminals are referred as base & collector currents, which are denoted as I_B & I_c.

For current flow through the BJT in 2 PN junctions (2 diodes back to back) must be properly biased.

One Junction is forward bias while the other is Reverse Bias.

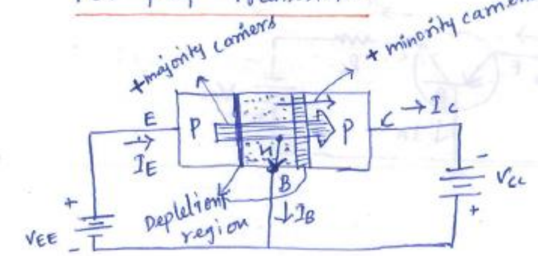
1. Forward Bias

   When the p side is applied +ve and n side is applied -ve in a Junction & applied voltage is greater than a threshold 0.65 V for Si

2. Reverse Bias

   When the p side is applied -ve and n side is applied +ve in a Junction & applied voltage is between 0 to a breakdown voltage.

For PNP Transistor



* The Emitter-Base Junction is forward biased while the collector-Base Junction is Reverse biased.
* The majority carriers will flow from E to B across forward bias Junction.

* Because the Base layer is very thin & has a high resistance. most of these carriers will diffuse across the reverse bias junction into the collector in the same direction of the minority charges & only tiny amount of current will flow out of the Base Terminal.

* Typically collector currents are of the order of mA While Base currents are μA.

* Applying Kirchhoff's current law:

$$I_E = I_C + I_B$$

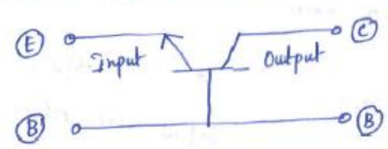
* The collector current is comprised of 2 components → majority & minority carriers.
* The minority current component is called leakage current, I_{CO} (I_C with Emitter terminal open).
* So the collector current is

$$I_C = I_{C\,majority} + I_{CO\,minority}$$

Transistor Configurations:

1. Common Base (CB) configuration
2. Common Emitter (CE) configuration
3. Common Collector (CC) configuration

1. Common Base configuration



* The Base terminal is common to both i/p & o/p.
* The i/p is applied b/w the Emitter & the base & o/p is taken from collector & Base.

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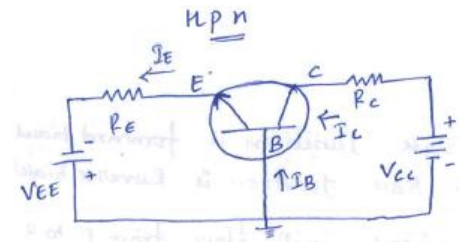

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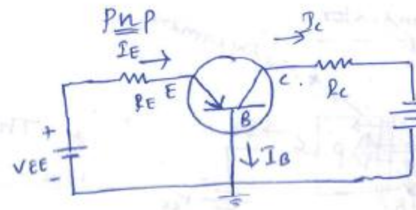
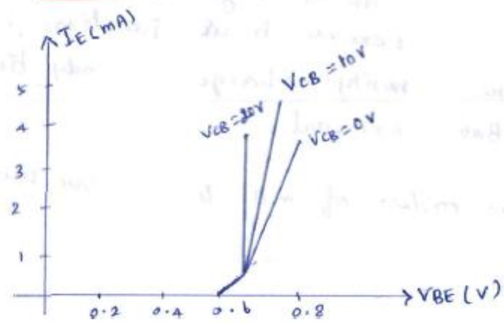


Consider npn

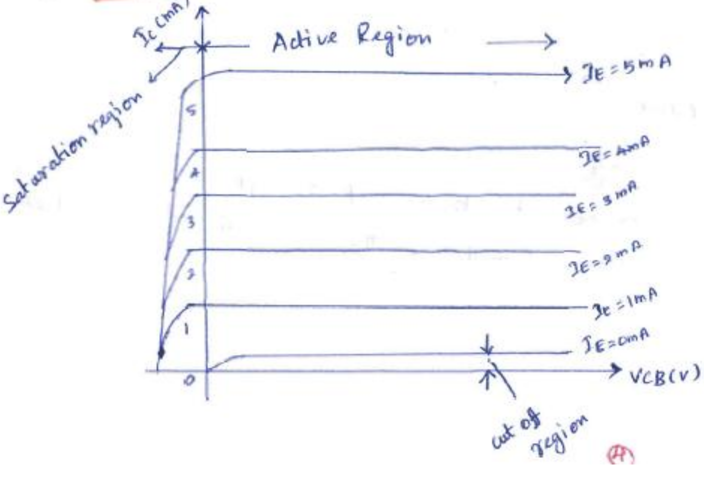
1. Input Characteristics



* It shows the relation b/w input current I_E & input voltage V_{BE} for different value of output voltage V_{CB}.
* It resembles the characteristics of forward bias diode.

* I_E increases as V_{BE} increases for a fixed value of V_{CB}.
* As V_{CB} increases, the width of the depletion layer in the Base increases.
* Hence, the width of the Base available for conduction decreases.
* The reduction in the width of the Base due to increase in Reverse bias is known as Early Effect.
* Due to Early effect, the chance of recombination of electrons with holes in the Base decreases.
* As V_{CB} further increases, at one stage the depletion region completely occupies the Base at which the collector-Base junction breaks down.
* This phenomenon is known as punch-through.

2. Output Characteristics



* It shows the relationship b/w the o/p voltage V_{CB} & o/p current I_C for different values of input current I_E.

(4)

i) Cut-off Region

* Both the junctions are reverse biased.
* When the emitter-base junction is reverse biased, the current due to majority carrier ie I_E is zero.
* When the collector-base junction is reverse biased, the current due to minority carriers flows from the collector to the base is represented as I_{CBO}.

ii) Active Region

* The Emitter-base Junction is forward biased & the collector-base junction is reverse biased.
* Once the V_{CB} reaches a value large enough to ensure a large portion of electrons enter the collector, I_C remains constant as shown by horizontal lines.
* As I_E increases, I_C increases.

iii) Saturation Region

* Both junctions are forward biased.
* When V_{CB} is -ve, the collector-base junction is actually forward biased
* Thus, graphs are drawn on the -ve side of V_{CB}.

Current Amplification factor (α)

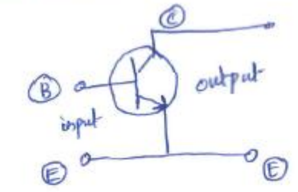
* It's the ratio of change in collector current to the change in Emitter current at constant collector-base voltage V_{CB}.

$$\alpha_{AC} = \frac{\Delta I_C}{\Delta I_E} \Bigg|_{V_{CB} = \text{constant}}$$

* If only DC values are considered

$$\alpha_{DC} = \frac{I_C}{I_E}$$

2. Common-Emitter configuration



* Input is applied b/w base & Emitter and output is taken b/w collector & the emitter.

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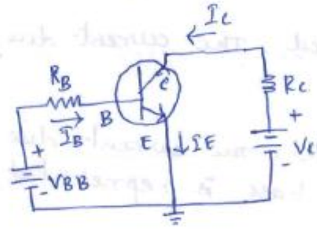

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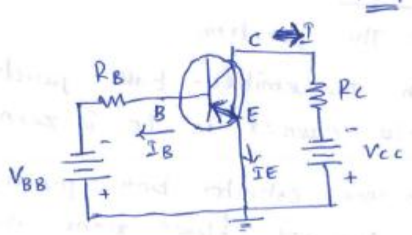
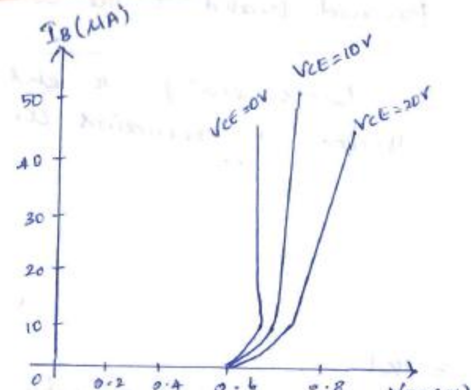


Consider npn

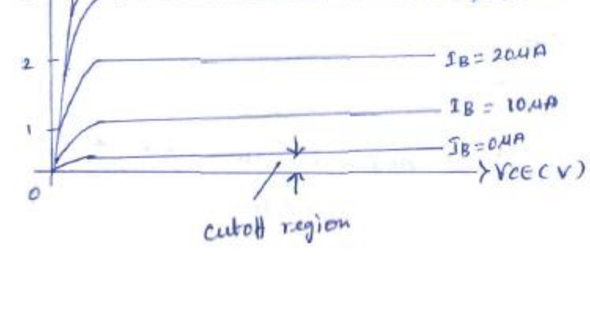
1. Input characteristics



* It shows the relationship b/w the i/p current I_B & i/p voltage V_{BE} for different values of o/p voltage V_{CE}.
* It resembles the characteristics of forward bias diode.
* I/p current I_B increases as i/p voltage V_{BE} increases for fixed value of V_{CE}.

* As V_{CE} increases, the depletion region in the collector base increases which decreases the width of the base available for conduction.
* Hence I_B decreases due to early Effect & the graph shifts towards the x-axis.

2. Output characteristics



* It shows the relation b/w o/p current I_C & o/p voltage V_{CE} for different values of i/p current I_B.

i) Cut-off Region

* Both the junctions are reverse biased.
* When the emitter-base junction is reverse biased, the current due to majority carriers ie I_B is zero.
* When the collector-base junction is reverse biased. The current due to minority carriers flows from the collector to emitter which is represented as I_{CEO}.

ii) Active Region

* The Emitter-base junction is forward biased & the collector-base junctio is reverse biased.
* As I_B is maintained constant, current I_C increases as reverse-bias voltage V_{CE} increases.

iii) Saturation Region

* Both junctions are forward biased.
* When V_{CE} is reduced to a small value such as 0.2 V, the collector base junction is actually forward biased.
* In this region, there is a large change in I_C with small change in V_{CE}

Current Amplification factor (β)

* It's defined as the change in collector current to the change in base current as constant collector-Emitter voltage V_{CE}.

$$\beta_{AC} = \frac{\Delta I_C}{\Delta I_B} \Big|_{V_{CE} = \text{constant}}$$

* If only DC values are considered

$$\beta_{DC} = \frac{I_C}{I_B}$$

Relation between α and β

$$I_E = I_C + I_B \quad — (1)$$

Also, $$\beta_{DC} = \frac{I_C}{I_B} \quad — (2)$$

From (1) $$I_B = I_E - I_C \quad — (3)$$

sub (3) in (2) $$\beta_{DC} = \frac{I_C}{I_E - I_C} \quad — (4)$$

* Divide eqn (4) by I_E both Numerator & Denominator

$$\text{(4)} \Rightarrow \beta_{DC} = \frac{I_C / I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}} = \frac{I_C / I_E}{1 - \frac{I_C}{I_E}} \quad \text{— (5)}$$

W.K.T $\alpha_{DC} = \frac{I_C}{I_E}$

Sub α_{DC} in eqn (5)

$$\text{(5)} \Rightarrow \beta_{DC} = \frac{\alpha_{DC}}{1 - \alpha_{DC}}$$

* If subscript DC is ignored

$$\beta = \frac{\alpha}{1-\alpha}$$

Collector Current (I_C):

* Apply KCL to the transistor

$$I_E = I_B + I_C \quad \text{— (A)}$$

* The collector current has 2 components

$$I_C = I_{C\,majority} + I_{C\,minority}$$

$$I_C = \alpha I_E + I_{CO} \quad \text{— (B)}$$

* For general purpose Transistors → I_C is measured in mA & I_{CO} is measured in μA (or) nA.

sub eq (A) in (B)

$$I_C = \alpha(I_B + I_C) + I_{CO}$$

$$= \alpha I_B + \alpha I_C + I_{CO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CO}$$

$$I_C = \frac{\alpha}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CO}$$

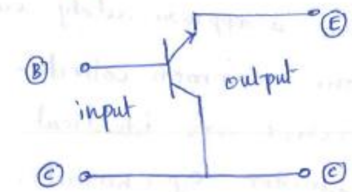
$$\because \beta = \frac{\alpha}{1-\alpha}$$

$$= \beta I_B + \frac{1}{1-\alpha} I_{CO}$$

sub $\frac{1}{1-\alpha} = (\beta+1)$ so we get

$$I_C = \beta I_B + (\beta+1) I_{CO}$$

3. Common- Collector Configuration



* The i/p is applied b/w base & collector & o/p is taken b/w Emitter & collector.

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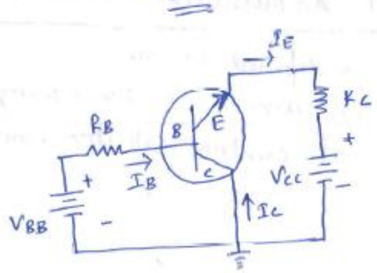

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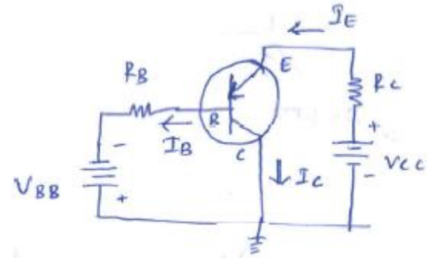
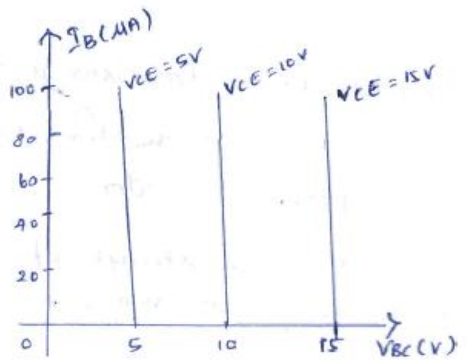


consider npn

1) Input characteristics

* It shows the relation b/w i/p current I_B & i/p voltage V_{BC} for different values of o/p voltage V_{CE}.
* The i/p voltage V_{BC} is largely determined by the o/p voltage V_{CE}.



* The i/p current I_B decreases to 0 as i/p voltage V_{CB} increases slightly for fixed values of V_{CE}.

$$V_{CE} = V_{BE} + V_{BC}$$

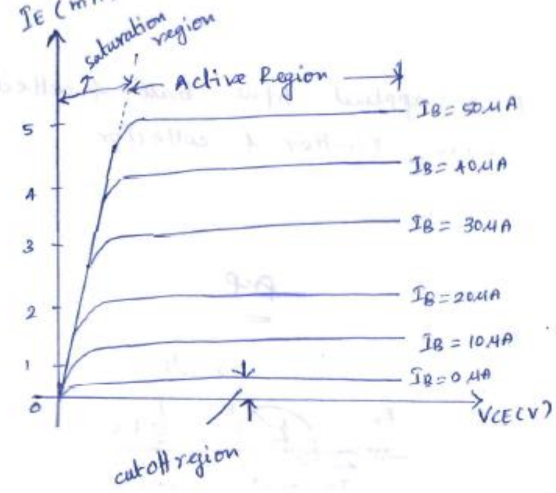
$$V_{BE} = V_{CE} - V_{BC}$$

* When V_{BC} is increased by keeping V_{CE} constant, V_{BE} decreases whic decreases I_B.

* ∴ If the value of V_{BE} is allowed to increase to a point where it's near to the value of V_{CE}, the value of V_{BE} approaches 0 & no base current will flow.

2) Output characteristics.

* It shows the relation b/w o/p current I_E & o/p voltage V_{CE} for different values of i/p current I_B.



* Since I_C is approximately equal to I_E, the common collector characteristics are identical to the common emitter o/p characteristics.

Current Amplification factor (γ)

* It's defined as the ratio of change in Emitter current to the change in base current at constant collector-emitter voltage V_{CE}.

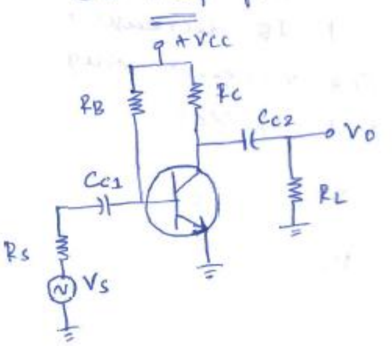
$$\gamma_{AC} = \frac{\Delta I_E}{\Delta I_B} \Big| V_{CE} = \text{constant}$$

* If only DC values are considered

$$\gamma_{DC} = \frac{I_E}{I_B}$$

Load Line Analysis

CE Amplifier



* The basic function of a transistor is to do amplification.
* The weak signal is given to the transistor & amplified output is obtained from the collector.
* The process of raising the strength of weak signal without any change in its general shape is known as Amplification.
* A Transistor must be properly biased to operate as an amplifier.

* In CE amplifier the Capacitor C_{C1} is a DC blocking capacitor & couples AC input signal to the base of the Transistor.
* The capacitor C_{C2} is used to couple AC output of the amplifier to load R_L

DC Analysis:

For DC, $f = 0$

$$X_C = \frac{1}{2\pi f_C} = \frac{1}{0} = \infty$$

* The DC equivalent circuit is obtained by replacing all capacitors by open circuit.

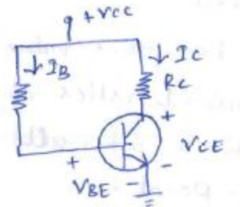


Fig: DC Equivalent circuit

Load Line :

* Applying KVL to the collector - Emitter circuit

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CC} - V_{CE} = I_C R_C$$

$$I_C = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C} \quad \text{——} \; ①$$

* The eqn ① represent the DC load line with slope is $-\frac{1}{R_C}$ & 'y' intercept of $\frac{V_{CC}}{R_C}$.

* When $I_C = 0$ ie the transistor is in cutoff region

$$① \Rightarrow \quad 0 = -\frac{1}{R_C} V_{CE} + \frac{V_{CC}}{R_C}$$

$$\frac{V_{CE}}{R_C} = \frac{V_{CC}}{R_C}$$

$$V_{CE} = V_{CC}$$

* When $V_{CE} = 0$ ie the transistor is in saturation region

$$① \Rightarrow \quad I_C = -\frac{1}{R_C}(0) + \frac{V_{CC}}{R_C}$$

$$I_C = \frac{V_{CC}}{R_C}$$

* The two endpoints are $(V_{CC}, 0)$ & $(0, \frac{V_{CC}}{R_C})$.

* A line passing through these points is called DC load line as the slope of this line depends on the DC load R_C.

Quiescent point

* Applying KVL to the base - Emitter circuit

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B R_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

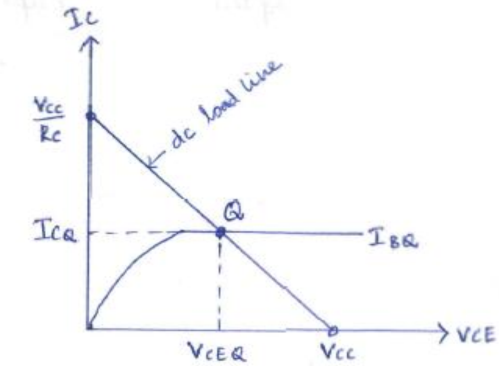


Fig: Load line and Q point

* This equation gives the value of base current.
* For this value of base current, o/p characteristics of the amplifier is plotted which intersects the Dc load line at Q-point.
* Hence, Q point indicates quiescent (inactive, still) value of collector-Emitter voltage V_{CE} & collector current I_C.

Need for Biasing

* The Transistor can be operated in 3 regions: cutoff, active & saturation by applying proper biasing conditions

Region of operation	Emitter-Base Junction	collector-Base Junction
cut off	Reverse biased	Reverse biased
Active	forward biased	Reverse biased
Saturation	forward biased	Forward biased

* In order to operate Transistor in the desired region we have to apply external dc voltage of correct polarity & magnitude to the 2 junctions of the Transistor. This is called biasing of the Transistor.

* Dc biasing is used to establish proper values of I_C & V_{CE} called the Dc operating point (or) quiescent point (or) Q point.

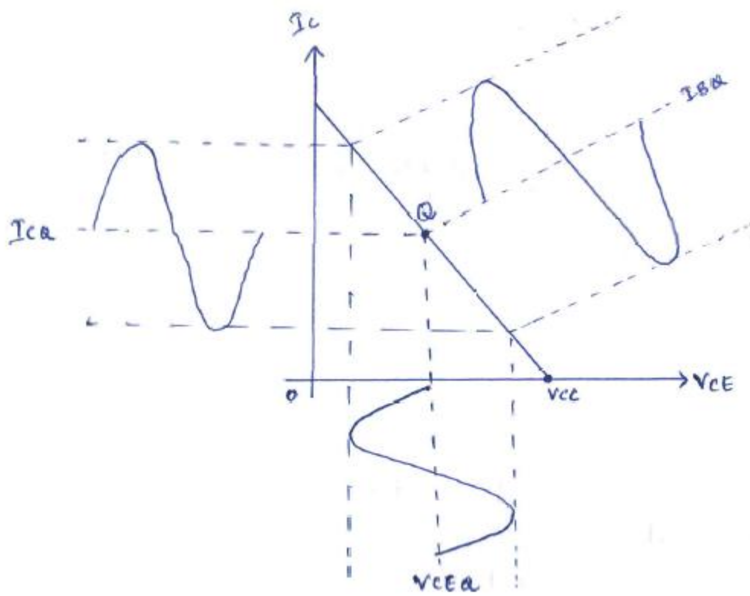
* The value of I_C & V_{CE} is expressed interms of operating point (or) Q point.
* For faithful amplification, Q point must be selected properly.
* The fulfilment of the below condition is known as transistor biasing
    1. proper zero signal collector current I_C
    2. proper base-emitter voltage V_{BE}
    3. proper collector-emitter voltage V_{CE}

Selection of operating point:

* While fixing the Q-point it has to be seen that the o/p of the amplifier is a proper sinusoidal waveform for sinusoidal input without distortion.

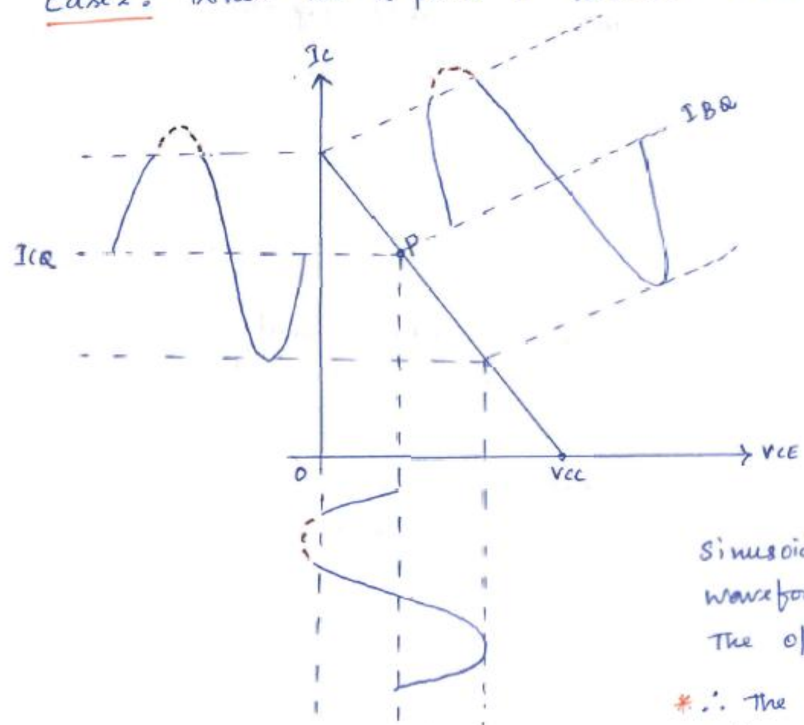
* If an amplifier is not biased properly, it can go into saturation (or) cutoff when an i/p signal is applied.
* By fixing the Q-point at different positions, we can observe the variation in I_C & V_{CE} corresponding to a given variation of I_B.

Case 1: When the Q point is located in the middle of the DC load line (or) center of the Active region



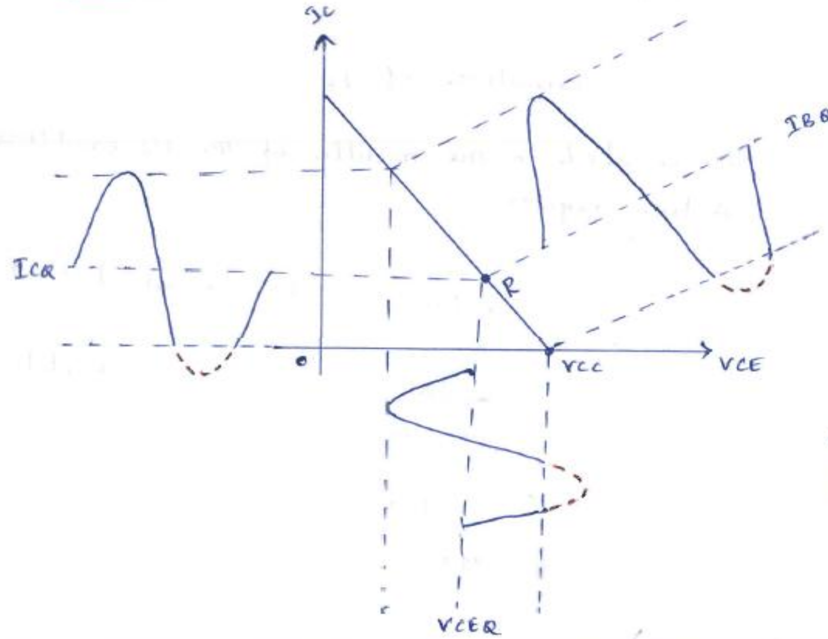
* The Q point is fixed at point Q.
* The o/p signal is sinusoidal waveform without any distortion
* Thus the point Q is the best operating point.

Case 2: When the Q point is located near the saturation region.



* The Q point is fixed at point P.
* The point P is very near to saturation region.
* The collector current I_C is clipped only at the positive half cycle.
* Eventhough the I_B varies sinusoidally, I_C is not a sinusoidal waveform i.e distortion is present at the o/p.
* ∴ The point P is not a suitable operating point.

Case 3: When the Q-point is located near the cut-off region



* The Q point is fixed at point R.
* The point R is very near to the cut off region.
* The I_c is clipped at the negative half cycle.
* So point R is also not a suitable Q point (or) operating point.

Variation of Q-point (or) Factors Affecting stability of Q-point

* The biasing circuit should be designed to fix the operating point (or Q-point at the centre of the active region.
* But only fixing of the operating point is not sufficent.
* While designing the biasing circuit, care should be taken so that the Q-point will not shift into an undesirable region (ie cutoff or saturati
* Designing the bias circuit to stabilize the Q-point is taken as bias stability.

Temperature

1) I_{CO}

* The flow of current in the circuit produces heat at the junctions.
* This heat increases the temperature at the junctions.
* We know that the minority carriers are temperature dependent
* They increase with Temperature.
* The increase in the minority carriers increases the leakage curre I_{CEO}.

$$\because \; I_{CEO} = (1+\beta) I_{CBO}$$

* I_{CBO} doubles for every $10°C$ rise in temperature.

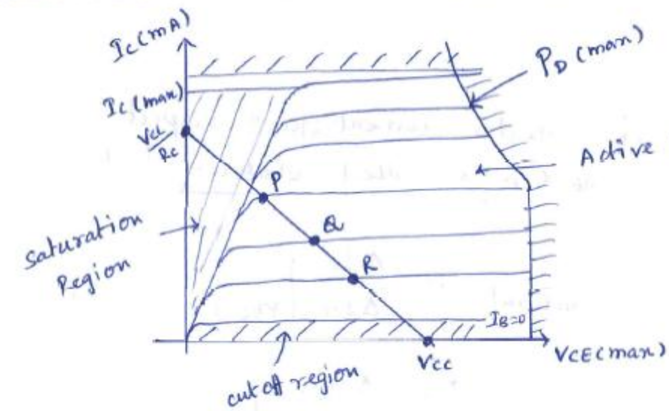
* Increase in I_{CEO} in turn Increase in the collector current.

$$\therefore I_C = \beta I_B + I_{CEO}$$

* The increase in I_C further raises the temperature at the collector junction & the same cycle repeats.
* The excessive increase in I_C shifts the Q-point into the saturation region, changing the operating condition set by biasing circuit.
* The power dissipation at collector base junction is

$$P_D = V_C I_C$$

* The increase in the I_C increases the power dissipated at the collector junction.
* This in turn further increase the temperature of the junction & hence increase the I_C.
* The power is cumulative.
* The excess heat produced at the collector base junction may even burn & destroy the transistor.
* This situation is called Thermal runaway of the transistor.
* For any Transistor the maximum power dissipation is always a fixed value.
* This known as <u>maximum power dissipation</u> rating of a Transistor.



* The hyperbola give the maximum power dissipation for Transistor
* If this limit is crossed the device will fail.

2) V_{BE}

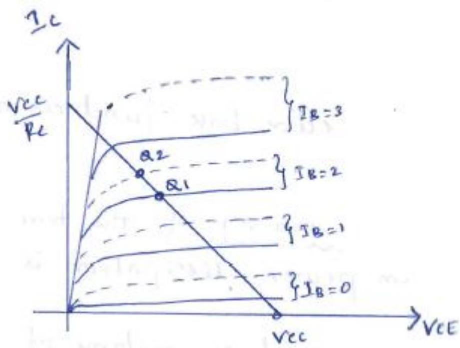
* V_{BE} changes with temperature at the rate of 2.5 mV/°C
* I_B depends upon V_{BE}
* I_B depends on V_{BE} & I_C depends on I_B. I_C depends on V_{BE}.
* $\therefore I_C$ changes with temperature due to changes in V_{BE}
* The change in I_C changes the Q-point.

3) β_{dc}

* It's also temperature dependent.
* As β_{dc} varies, I_c also varies, since $I_c = \beta I_B$
* The change in I_c change the Q-point.

Transistor current gain $h_{FE} | \beta$

* There are changes in the Transistor parameters among different units of the same type, same number.
* If we take 2 transistor units of same type & use them in the circuit, there is change in the β value in actual practice.
* The biasing circuit is designed according to the required β value.
* But due to change in β from unit to unit, the Q-point may shift.



* This fig: shows the CE o/p characteristics for 2 Transistor of the same type.
* The dashed characteristics are for a Transistor whose β is much larger than that of the Transistor represent by solid curves.

Stability Factors

S:

* The rate of change of collector current (I_c) with respect to collector leakage current (I_{co}) at constant V_{BE} & β is called stability factor.

$$S = \frac{\partial I_c}{\partial I_{co}} \Big|_{V_{BE} \,\&\, \beta \text{ constant}} = \frac{\Delta I_c}{\Delta I_{co}} \Big|_{V_{BE} \,\&\, \beta \text{ constant}}$$

$$= \frac{\Delta I_{c_2} - \Delta I_{c_1}}{\Delta I_{co_2} - \Delta I_{co_1}} \Big|_{V_{BE} \,\&\, \beta \text{ constant}}$$

S':

* The rate of change of collector current (I_c) with respect to V_{BE} at constant I_{co} & β is called stability factor S'.

$$S' = \frac{\partial I_c}{\partial V_{BE}} \Big|_{I_{co} \,\&\, \beta \text{ constant}} = \frac{\Delta I_c}{\Delta V_{BE}} \Big|_{I_{co} \,\&\, \beta \text{ constant}} = \frac{\Delta I_{c_2} - \Delta I_{c_1}}{\Delta V_{BE_2} - \Delta V_{BE_1}} \Big|_{I_{co} \,\&\, \beta \text{ constant}}$$