Disadvantages

1. Thermal stability is not provided by this circuit. so the operating point is not maintained.

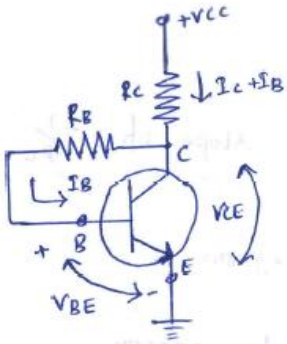
$$I_C = \beta I_B + I_{CEO}$$

2. Since $I_C = \beta I_B$ & I_B is already fixed; I_C depends on β which changes unit to unit & shifts the operating point.

The stabilization of operating point is very poor in the fixed bias circuit. Because of this reason the fixed bias circuit need some modifications.

In the modified circuit, R_B is connected b/w collector & base. Hence the circuit is called collector to base bias circuit.

2. Collector to Base Bias / Biasing with Feedback Resistor



* It's an improvement over the fixed bias method
* The resistor is connected b/w the base & the collector of the transistor. Hence the circuit is called collector to base bias circuit.
* Thus I_B flows through R_B & $(I_C + I_B)$ flows through the R_C.

Dc Analysis

* For Dc $f = 0$

$$X_C = \frac{1}{2\pi f C} = \frac{1}{0} = \infty$$

Collector Current I_C

* Apply KVL to the base - Emitter circuit

$$V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - (\beta + 1) I_B R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} - I_B((\beta+1)R_C + R_B) - V_{BE} = 0$$

$$V_{CC} - V_{BE} = I_B((\beta+1)R_C + R_B)$$

$$\boxed{I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta+1)R_C}}$$

* If there is a change in β due to piece to piece variation b/w Transistors, then I_C tends to increase. As the result voltage drop across R_C increases.
* The supply voltage V_{CC} is constant, due to increase in $I_C R_C$, V_{CE} decreases. Due to reduction in V_{CE}, I_B decreases. This I_B reduction is lead to increase I_C.

W.K.T $I_B = \frac{I_c}{\beta} \Rightarrow I_c = \beta I_B$

$$I_c = \beta \left[\frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_c} \right]$$

Collector Emitter Voltage V_{CE}

* Apply KVL to the collector - Emitter circuit

$$V_{cc} - (I_B + I_c) R_c - V_{CE} = 0$$

$$V_{CE} = V_{cc} - (I_B + I_c) R_c$$

Load Line Analysis

* Apply KVL to the collector - Emitter circuit

$$V_{cc} - (I_B + I_c) R_c - V_{CE} = 0$$

* Assume $I_B + I_c \simeq I_c$

$$V_{cc} - I_c R_c - V_{CE} = 0$$

$$I_c = -\frac{1}{R_c} V_{CE} + \frac{V_{cc}}{R_c}$$

* The equation represents a DC load line with slope of $-\frac{1}{R_c}$ & y-intercept $\frac{V_{cc}}{R_c}$.

* When $I_c = 0$ i.e Transistor is in cut-off region

$$V_{CE} = V_{cc}$$

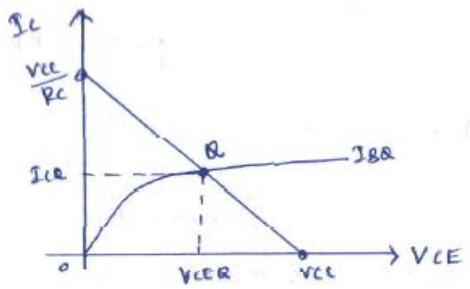
* When $V_{CE} = 0$ i.e Transistor is in saturation region

$$I_c = \frac{V_{cc}}{R_c}$$

* Thus the 2 end points are $(V_{cc}, 0)$ & $(0, \frac{V_{cc}}{R_c})$. by joining the 2 end points DC load line is drawn.

* From Base - Emitter circuit

$$I_B = \frac{V_{cc} - V_{BE}}{R_B + (\beta+1) R_c}$$



The saturation current for the circuit is $I_{c\,sat} = \frac{V_{cc}}{R_c}$

Stability Factors

S :

* Apply KVL to the base - Emitter junction

$$V_{CC} = I_C R_C + I_B (R_C + R_B) + V_{BE}$$

* When I_B changes by ∂I_B & I_C changes by ∂I_C There is no effect on V_{CC} & V_{BE}

* So the equation becomes

$$0 = \partial I_C R_C + \partial I_B (R_C + R_B) + 0$$

$$\partial I_B (R_C + R_B) = -\partial I_C R_C$$

$$\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_C + R_B} \quad -(1)$$

* substitute (1) in S

$$S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{1+\beta}{1-\beta\left(\frac{-R_C}{R_C+R_B}\right)}$$

$$S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$$

* The collector - Base bias circuit is having Lesser stability factor than fixed bias circuit.

* Hence the circuit provides better stability than fixed bias circuit

S' :

$$S' = \frac{-\beta}{R_B + (1+\beta)R_C}$$

S'' :

$$S'' = \frac{I_C}{\beta}\left(\frac{S}{1+\beta}\right)$$