PARALLEL COMMUNICATION INTERFACE

8255 (PROGRAMMABLE PERIPHERAL INTERFACE)

The 8255 is a widely used, programmable parallel I/O device. It can be programmed to transfer data under data under various conditions, from simple I/O to interrupt I/O. It is an important general purpose I/O device that can be used with almost any microprocessor.

The 8255 has 24 I/O pins that can be grouped primarily into two 8 bit parallel ports: A and B, with the remaining 8 bits as Port C. The 8 bits of port C can be used as individual bits or be grouped into two 4 bitports: CUpper (CU) and CLower (CL). The functions of these ports are defined by writing a control word in the control register.

8255 can be used in two modes: Bit set/Reset (BSR) mode and I/O mode.

- The BSR mode is used to set or reset the bits in port C.
- The I/O mode is further divided into 3 modes:
  - **mode 0**- all ports function as simple I/O ports
  - **mode 1** - a handshake mode whereby Port A and/or Port B use bits from Port Cas handshake signals
  - **mode 2**- Port A can be set up for bidirectional data transfer using handshakesignals from Port C, and Port B can be set up either in mode 0 or mode 1

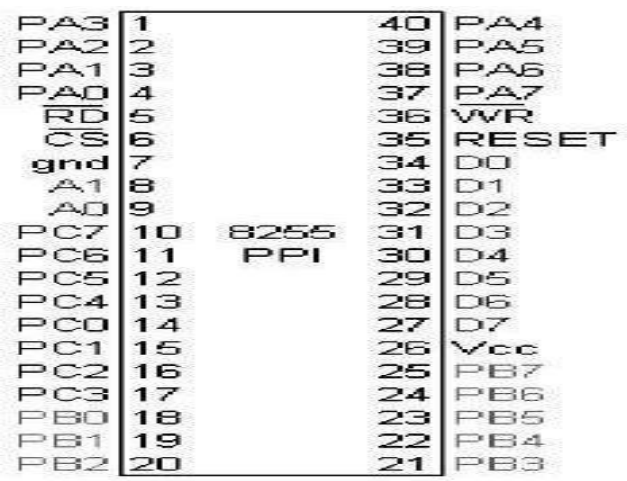

Figure 3.2.1 Pin Configuration of 8255

The signal description of 8255 is briefly presented as follows:

PA7-PA0: These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the control word register.

PC7-PC4: Upper nibble of port C lines. They may act as either output latches or input buffers lines. This port also can be used for generation of handshake lines in mode 1 or mode 2.

PC3-PC0: These are the lower port C lines, other details are the same as PC7-PC4 lines.

PB0-PB7: These are the eight port B lines which are used as latched output lines or buffered input linesin the same way as port A.

RD: This is the input line driven by the microprocessor and should be low to indicate read operation to8255.

WR: This is an input line driven by the microprocessor. A low on this line indicates write operation.

CS: This is a chip select line. If this line goes low, it enables the 8255 to respond to RD and WR signals, otherwise RD and WR signal are neglected.

A1-A0: These are the address input lines and are driven by the microprocessor. These lines A1-A0 with RD, WR and CS from the following operations for 8255. In case of 8086 systems, if the 8255 is to be interfaced with lower order data bus, the A0 and A1 pins of 8255 are connected with A1 and A2 respectively.

D0-D7: These are the data bus lines those carry data or control word to/from the microprocessor.

RESET: A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.

8255 BLOCK DIAGRAM:

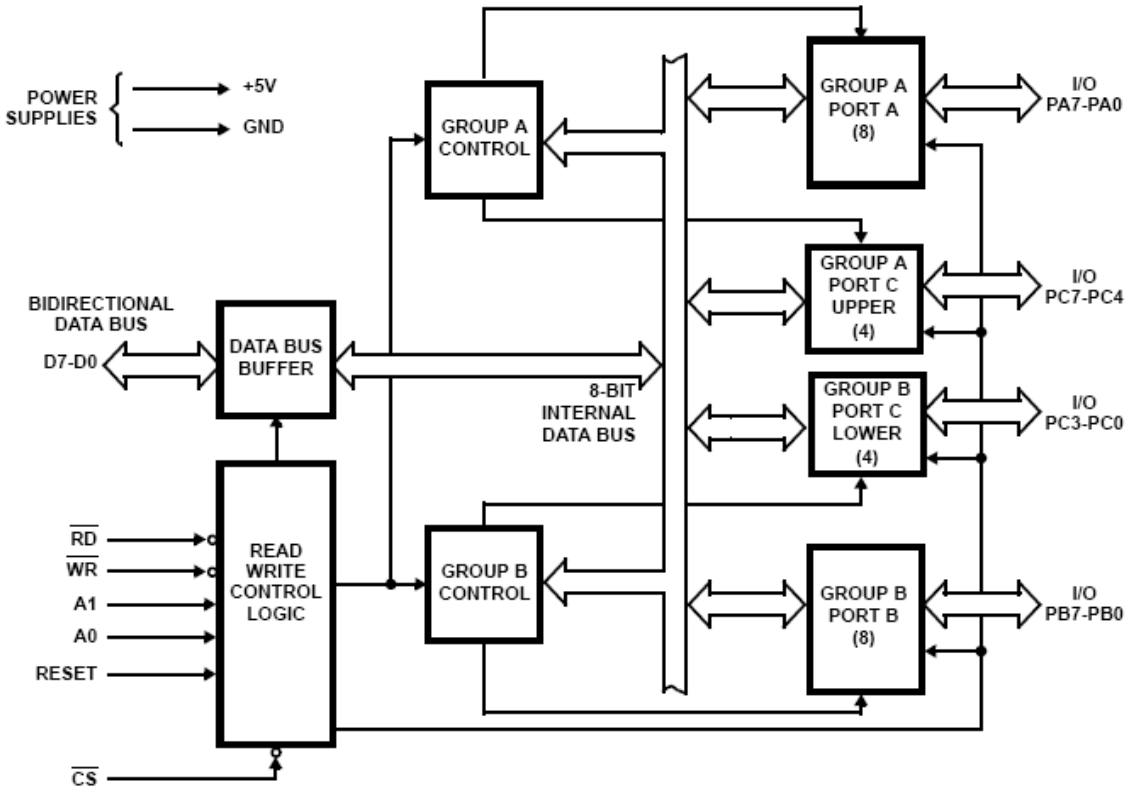

Figure 3.2.2 Block Diagram of 8255

Data Bus Buffer-This three-state bi-directional 8-bit buffer is used to interface the 8255 to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions bythe CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.**A0 and A1** Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word register as shown in **Table 3.2.1.**They are normally connected to the least significant bits of the address bus (A0 and A1)

CS	A1	A0	Selection
0	0	0	Port A
0	0	1	Port B
0	1	0	Port C
0	1	1	Control Register
1	x	x	8255 is not selected

Table 3.2.1 Port / Control Register Selection

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control logic, receives "controlwords" from the internal data bus and issues the proper commands to its associated ports.

Ports A, B, and C

The 8255 contains three 8-bit ports (A, B, and C). All can be configured to a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255.

Port A One 8-bit data output latch/buffer and one 8-bit data input latch. Both "pull-up" and "pull-down" bus-hold devices are present on Port A.

Port B One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input).

This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal output and status signal inputs in conjunction with ports A and B.

OPERATION MODES OF 8255:

The bit pattern loaded in control word register specifies an I/O functionfor each port and the mode ofoperation in which the ports are to be used.

There are two different control word formats which specify two basic modes:

- BSR (Bit set reset)mode
- I/O mode

The two basic modes are selected by *D*7 bit of control register. When *D*7=1 it is an I/O mode and when

*D*7=0; it is a BSR mode.

BSR MODE-

- The BSR mode is a port C bit set/reset mode.
- The individual bit of port C can be set or reset by writing control word in thecontrol register.
- The control word format of BSR mode is as shown in the Figure 3.2.3 below:

.

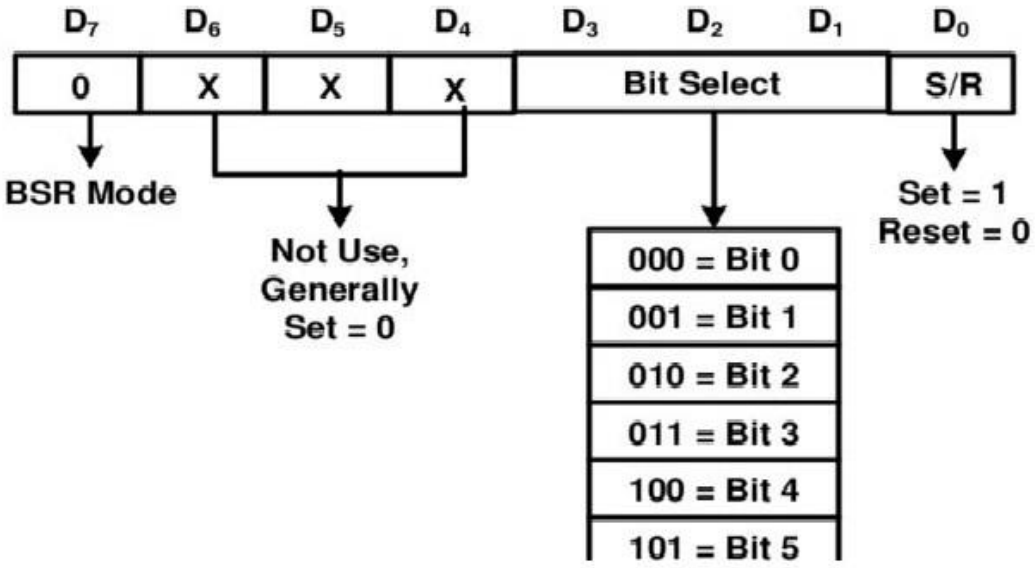

Figure 3.2.3 Control word for BSR Mode

- The pin of port C is selected using bit select bits [b b b] and set or reset is decided by bit S/$\overline{R}$.
- The BSR mode affects only one bit of port C at a time. The bit set using BSR mode remains set unless and until you change the bit. So to set any bit of port C, bit pattern is loaded in control register.

- If a BSR mode is selected it will not affect I/O mode.

I/O MODES

There are three I/O modes of operation:

- Mode 0- Basic I/O
- Mode 1- Strobed I/O
- Mode 2- Bi-directional I/O

The I/O modes are programmed using control register.The control word format of I/O modes is as shown in the Figure 3.2.4 below:

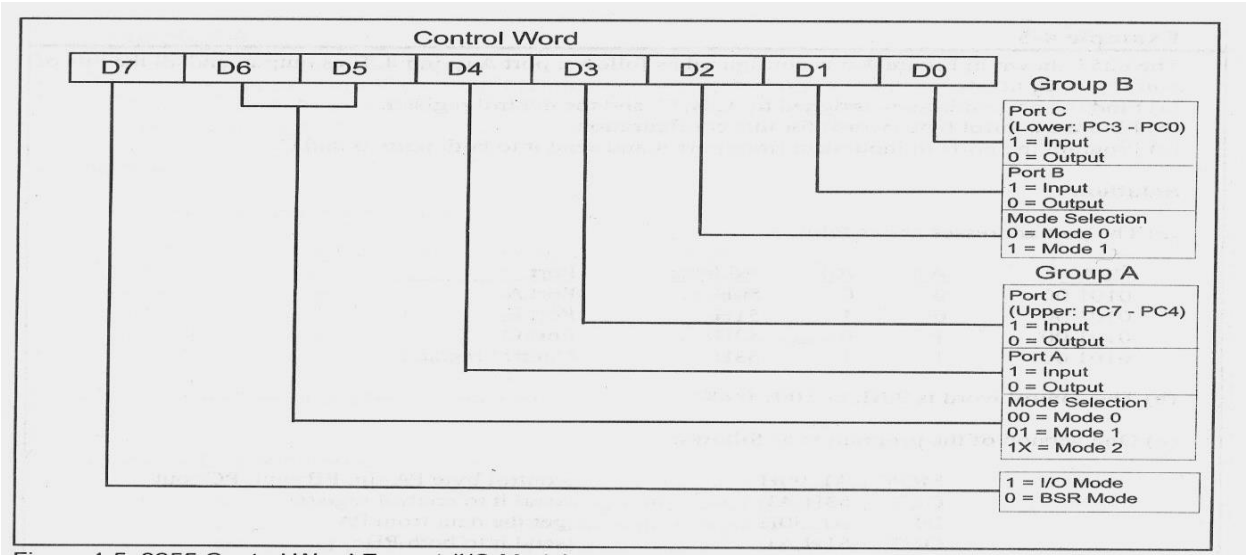

Figure 3.2.4 Control word for I/O Mode

Function of each bit is as follows:

1. *D*7– When the bit *D*7 = 1 then I/O mode is selected, if *D*7=0 then BSR mode is selected. The function of bits *D*0 to *D*6 is independent on mode (I/O mode or BSR mode).
2. *D*6 and *D*5-In I/O mode the bits D6 and D5 specifies the different I/O modes for group A i.e.Mode 0, Mode 1 and Mode 2 for port A and port Cupper.
3. *D*2 – In I/O mode the bit *D*2 specifies the different I/O modes for group B i.e. Mode 0 and Mode 1 for port B and port C lower.

All the 3 modes i.e. Mode 0, Mode 1 and Mode 2 are only for group A ports, but for group B only 2 modes i.e. Mode 0 and Mode 1 are provided. When 8255 is reset, it will clear control word register contents and all the ports are set to input mode. The ports of 8255 can be programmed for other modes by sending appropriate bit pattern to control register.

Mode 0: Simple Input or Output

In this mode, Port A and Port B are used as two simple 8-bit I/O ports and Port C as two4-bit I/O ports. Each port (or half-port, in case of Port C) can be programmed to function as simply an input port or an output port. The input/output features in mode 0 are: Outputs are latched, Inputs are not latched. Ports do not have handshake or interrupt capability.

Mode 1: Input or Output with handshake

In mode 1, handshake signals are exchanged between the microprocessor and peripherals prior to data transfer. The ports (A and B) function as 8-bit I/O ports. They can be configured either as input or output ports. Each port (Port A and Port B) uses 3 lines from port C as handshake signals. The remaining two lines of port C can be used for simple I/O functions. Input and output data are latched and Interrupt logicis supported.

Mode 1: Input control signals

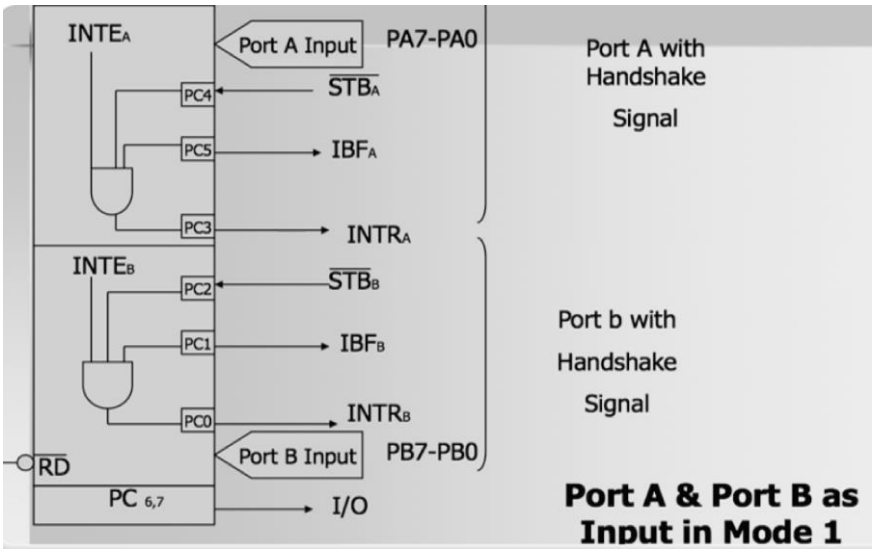

Figure 3.2.5 Input Control Signals

STB (**Strobe Input**): This signal (active low) is generated by a peripheral device that it has transmitted abyte of data. The 8255, in response to, generates IBF and INTR.

IBF (**Input buffer full):** This signal is an acknowledgement by the 8255 to indicate that the input latchhas received the data byte. This is reset when the microprocessor reads the data.

INTR (Interrupt Request): This is an output signal that may be used to interrupt the microprocessor.This signal is generated if , IBF and INTE are allat logic 1.

INTE (Interrupt Enable): This is an internal flip-flop to a port and needs to be set to generate the INTR signal. The two flip-flops INTEA and INTEB are set /reset using the BSR mode. The INTEA is enabled or disabled through PC4, and INTEB is enabled or disabled through PC2.

Figure 3.2.6 shows thr Mode 1 strobed Input Data Transfer.

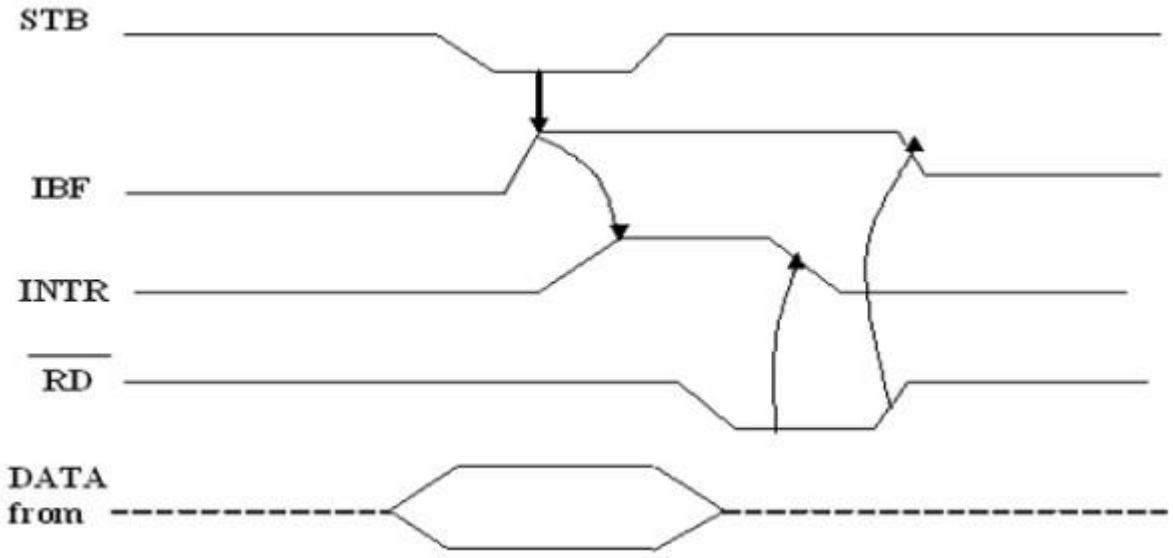

Figure 3.2.6 Mode 1 strobed Input Data Transfer

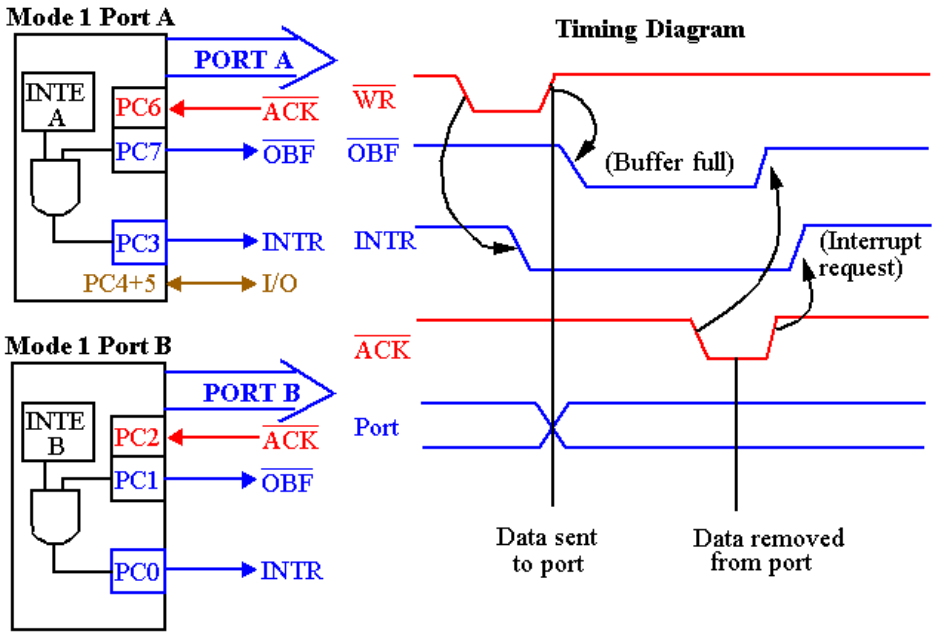

Figure 3.2.7 Output control signals

OUTPUT CONTROL SIGNAL DEFINITION:

OBF (Output Buffer Full): This is an output signal that goes low when the microprocessor writes data into the output latch of the 8255. This signal indicates to an output peripheral that new data is ready to be read. It goes high again after the 8255 receives a signal from the peripheral.

ACK (Acknowledge): This is an input signal from a peripheral that must output a low when the peripheral receives the data from the 8255 ports.

INTR (Interrupt Request): This is an output signal, and it is set by the rising edge of the signal. This signal can be used to interrupt the microprocessor to request the next data byte for output. The INTR is setand INTE are all one andreset by the rising edge of RD signal. INTEA & INTEB is controlled by bit set/reset of PC6 & PC2 respectively.

Mode 2: Bidirectional Data Transfer

This mode is used primarily in applications such as data transfer between the two computers or floppy disk controller interface. Port A can be configured as the bidirectional port and Port B either in mode 0 or mode 1. Port A uses five signals from Port C as handshake signals for data transfer. The remaining three lines from Port C can be used either as simple I/O or as handshake signals for Port B.