EXTERNAL MEMORY INTERFACE

EXTERNAL ROM (PROGRAM MEMORY) INTERFACING

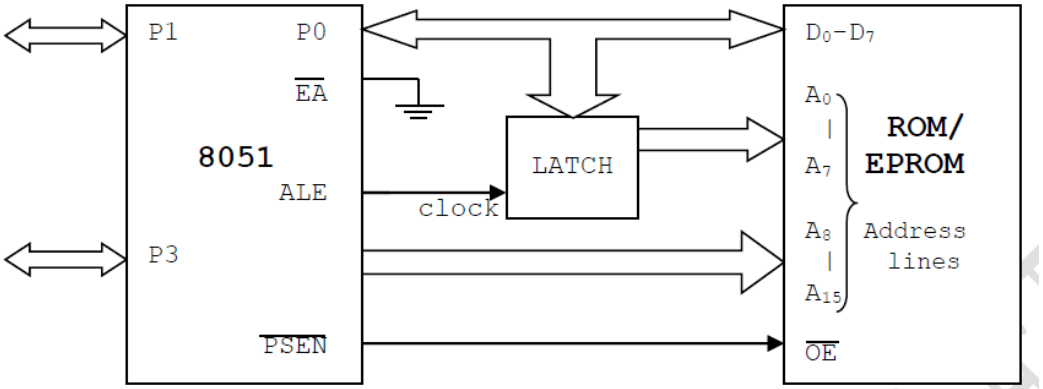

Figure 5.6.1 Interfacing of ROM/EPROM to 8051

Figure 5.6.1 shows how to access or interface ROM to 8051.

- Port 0 is used as multiplexed data & address lines. It gives lower order (A7-A0)
- 8bit address in initial T cycle & higher order (A8-A15) used as data bus.
- 8 bit address is latched using external latch & ALE signal from 8051.
- Port 2 provides higher order (A15-A8) 8 bit address.
- PSEN is used to activate the output enable signal of external ROM/EPROM.

EXTERNAL RAM (DATA MEMORY) INTERFACING

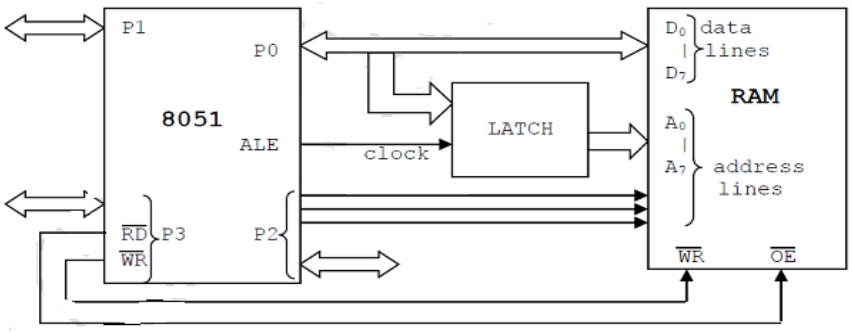

Figure 5.6.2 Interfacing of RAM to 8051

Figure 5.6.2 shows how to connect or interface external RAM (data memory) to 8051.

- Port 0 is used as multiplexed data & address lines.
- Address lines are decoded using external latch & ALE signal from 8051 to provide lower order (A7-A0) address lines.
- Port 2 gives higher order address lines.
- RD & WR signals from 8051 selects the memory read & memory write operations respectively.

Note:RD & WR signals: generally P3.6 & P3.7 pins of port 3 are used to generate memory read and memory write signals. Remaining pins of port 3 i.e. P3.0-P3.5 can be used for other functions.

Solved Examples:

Example 1: Design a μController system using 8051 to Interface the external RAM of size 16k x 8.

Solution: Given, Memory size: 16k

Which means, we require 2^n=16k: n address lines

- Here n=14: A0 to A13 address lines are required.
- A14 and A15 are connected through OR gate to CS pin of external RAM.
- When A14 and A15 both are low (logic '0'), external data memory (RAM) is selected.

Address Decoding (Memory Map) For 16k X 8 Ram

Address	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Hex Addr
Start	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000H
End	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFFH

Figure 5.6.3 shows interfacing of 16k x 8 RAM to 8051.

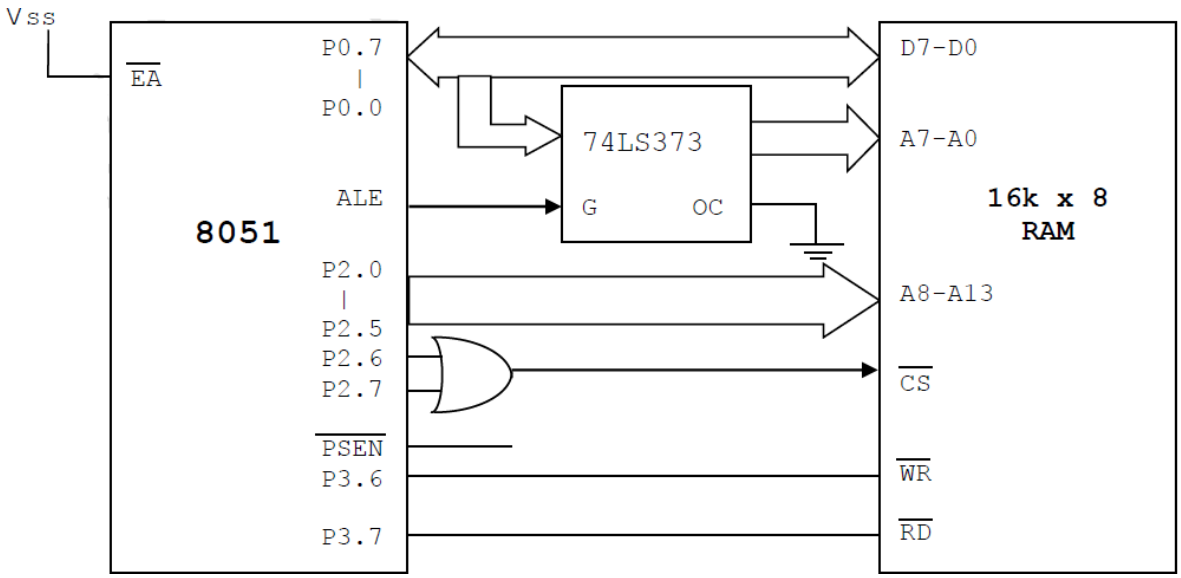

Figure 5.6.3 16Kx8 Memory (RAM) Interfacing with 8051

Example 2: Design a μController system using 8051 to interface the external ROM of size 4k x 8.

Solution: Given, Memory size: 4k

i.e we require 2^n=4k :: n address lines

- Here n=12 :: A0 to A11 address lines are required.
- Remaining lines A0, A0, A0, A0 & PSEN are connected though OR gate to CS & RD of external ROM.
- When A0 to A0 are low (logic '0'), only then external ROM is selected.

Address Decoding (Memory Map)for 4k x 8 RAM

Address	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Hex Addr
Start	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000 H
End	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0FFF H

Figure 5.6.4 shows interfacing of 4k x 8 ROM to 8051

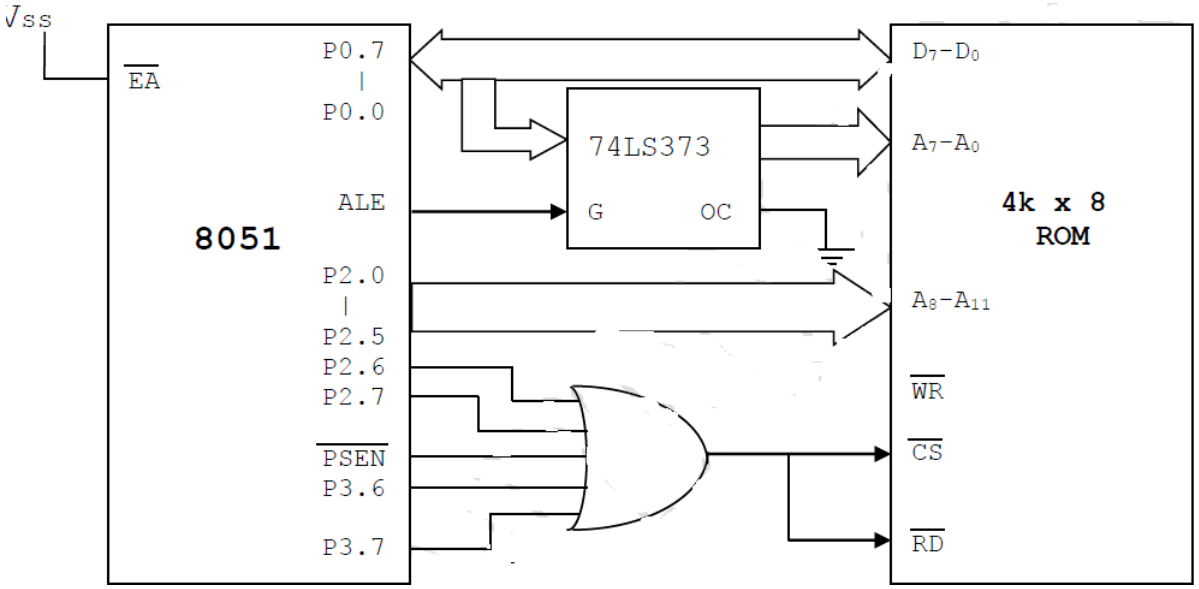

Figure 5.6.4 4Kx8 Memory (ROM) Interfacing with 8051

Example 3: Design a µController system using 8051, 16k bytes of ROM & 32k bytes of RAM. Interface the memory such that starting address for ROM is 0000H & RAM is 8000H.

Solution:

Given, Memory size- ROM : 16k

i.e we require 2^n=16k :: n address lines

Here n=14 :: A0 to A13 address lines are required.

A14,A15,PSEN ORed CS *when low – ROM is selected*

Memory size- RAM :32k

i.e we require 2^n=32k :: n address lines

Here n=15 :: A0 to A15 address lines are required.

A15 inverted(NOT Gate) CS when high- RAM is selected.

For RAM selection

- PSEN is used as chip select pin ROM.
- RD is used as read control signal pin..
- WR is used as write control signal pin.

Address Decoding (Memory Map) for 16k x 8 ROM.

Address	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Hex Addr
Start	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000 H
End	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	3FFF H

Address Decoding (Memory Map) for 32k x 8 RAM.

Address	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	Hex Addr
Start	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	8000 H
End	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	FFFF H

Figure 5.6.5 shows the interfacing of 16Kx8 Memory (ROM) and 32Kx8 RAM with 8051

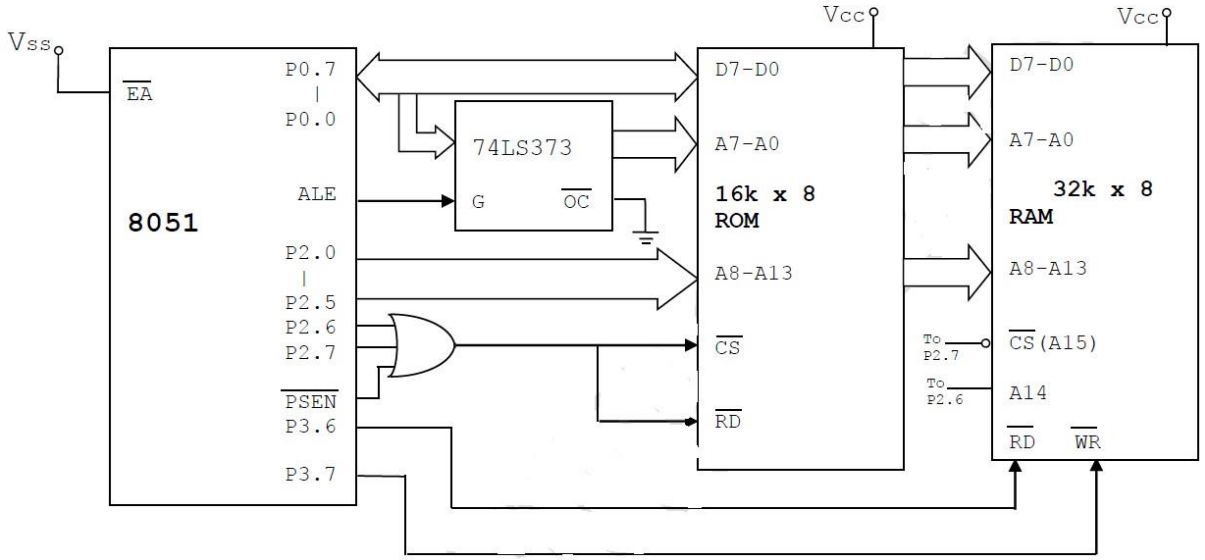

Figure 5.6.5 16Kx8 Memory (ROM) and 32Kx8 RAM Interfacing with 8051