SNS COLLEGE OF TECHNOLOGY

(AN AUTONOMOUS INSTITUTION)

COIMBATORE-35

19ECB211 - MICROCONTROLLER PROGRAMMING AND INTERFACING

UNIT V

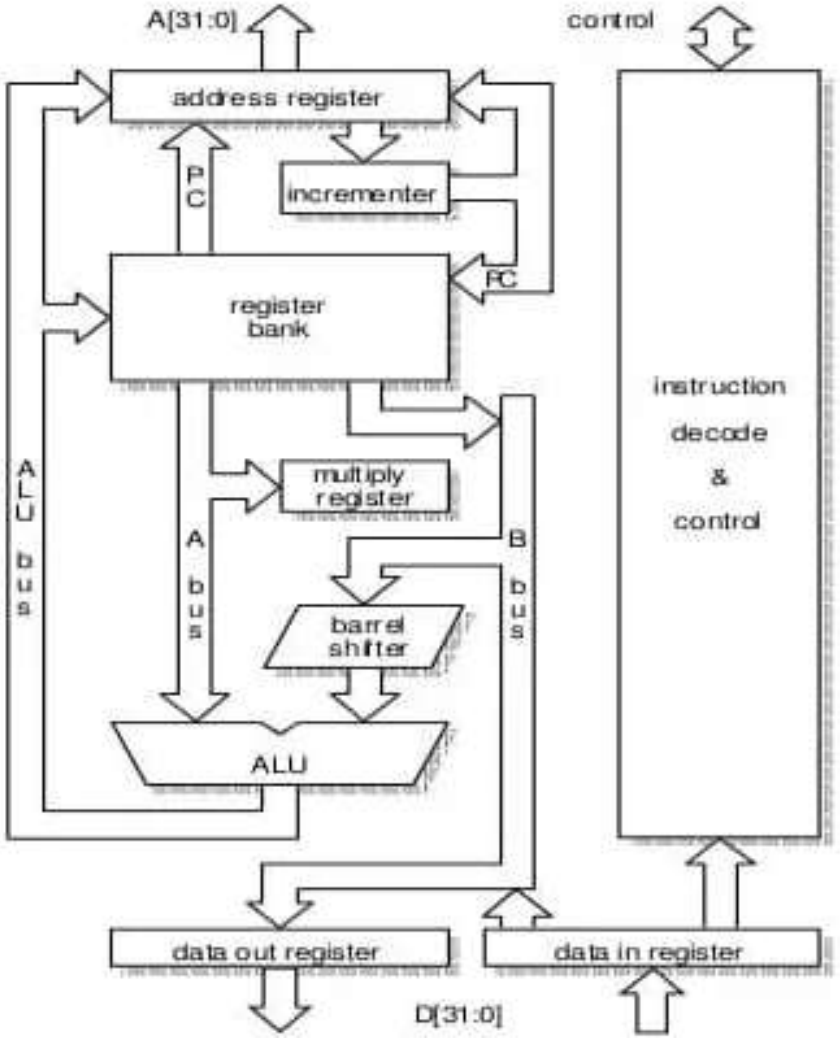
ADVANCED MICROCONTROLLERS

ARM MICROCONTROLLER - Architeture

INTRODUCTION

- The ARM stands for Advanced RISC Machine and basically it is available as a 32-bit RISC microcontroller.
- It was first introduced by the Acron Computer's Organization in 1987. Like other microcontrollers, the ARM is also a family of microcontroller architecture and this patent has been brought by different microcontroller chip designers and they are manufacturing micro-controllers such as ST Microelectronics, Motorola, NXP, etc.
- Basically the ARM comes with the different versions as each version has its own merit and demerit.
- The ARM processor family maintains his own design from 1987 when they have started their ARM microcontroller basics design.

The ARM Architecture



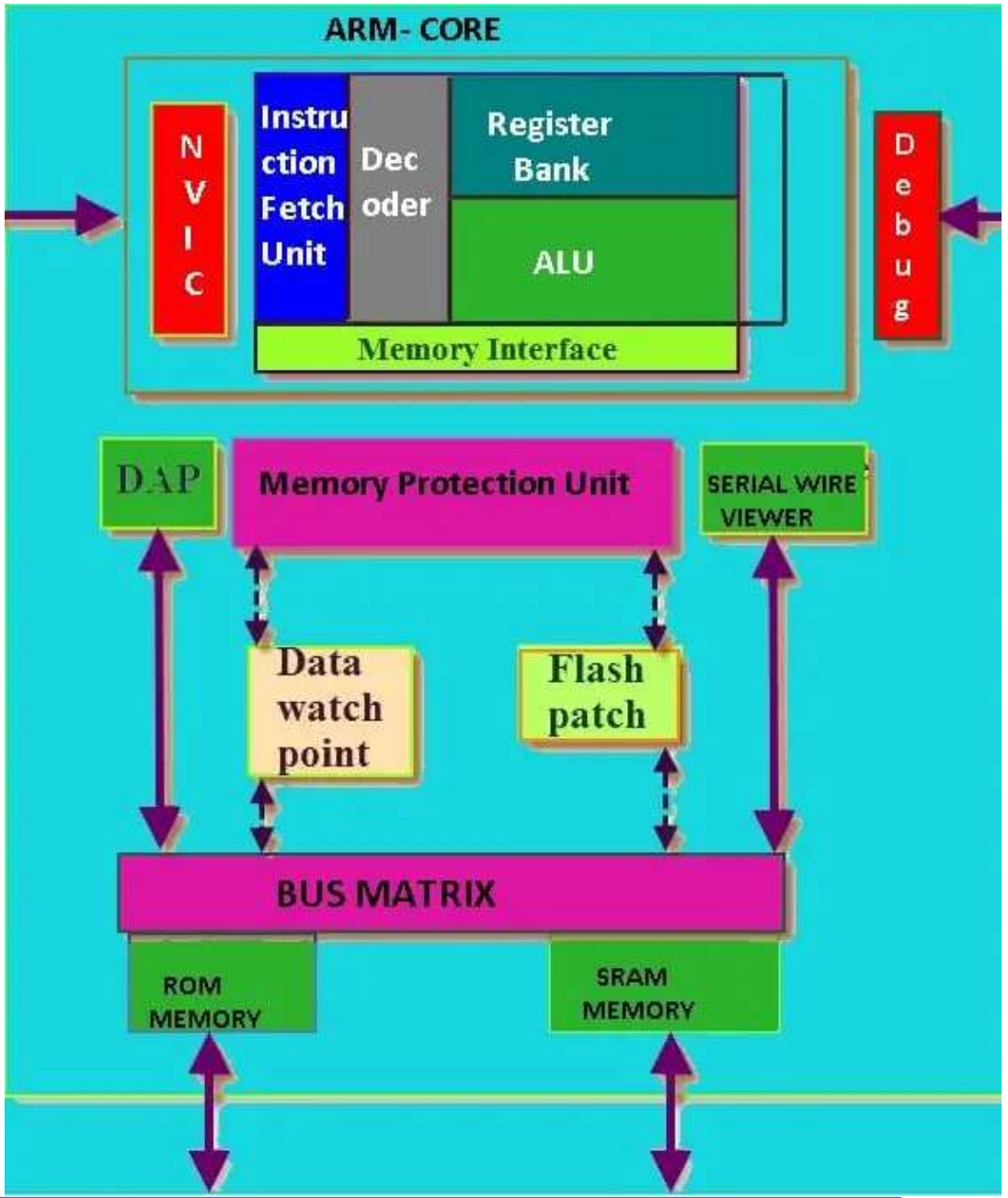
The ARM is having different variants available in the commercial market, but the ARM Cortex family which developed by the ARMv7 architecture.

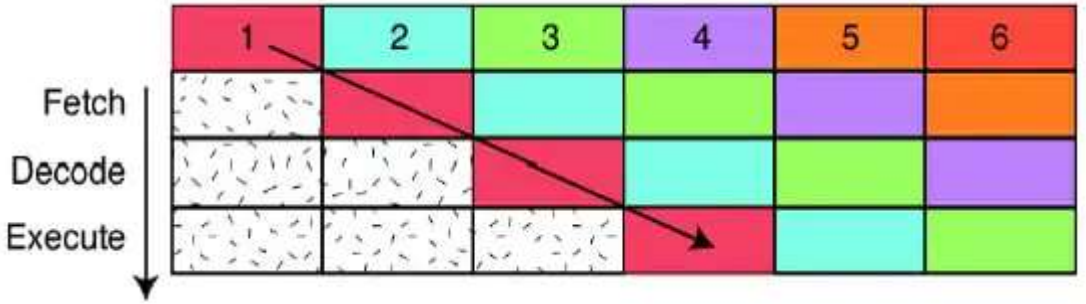
This is again divided into 3 subfamilies as:

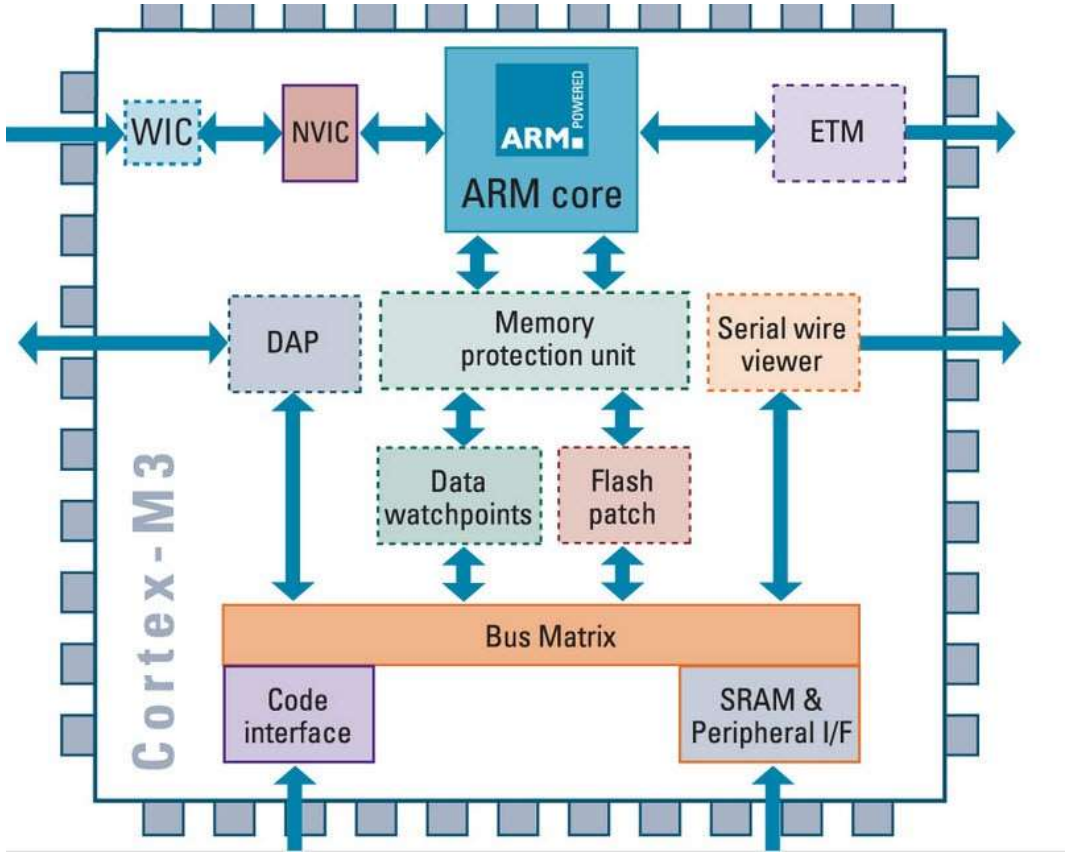
- ARM-Cortex Ax-series.
- ARM-Cortex Rx-series.
- ARM-Cortex Mx-series.

ARM Cortex-M3 MCU Architecture

- The Cortex-M3 processor is a high performance low-cost 32-bit processor. The ARM is a “Harvard Architecture” based processor that offer’s the separate Data and instruction line for communicating with RAM, ROM, etc.
- This is having consists 3-stage pipeline to fetch, decode, and execute the instructions sequentially.
- The Cortex series processors are the cost-sensitive device which is used to reduce the processor area and has extensive NVIC interrupt handling, and system debugs capability.
- The Cortex-M3 ARM processors are implemented by the **THUMB** instruction sets based on **THUMB-2** technology. Therefore, it ensures high code density and reduces the program memory requirement. The Cortex-M3 instruction set provides excellent performance due to modern 32-bit architecture. The ARM processor core-m3 is closely integrated to Nested Vector Interrupt Controller (NVIC) to provide a good interrupt performance.


ARM- CORE
NVIC
Instruction Fetch Unit
Decoder
Register Bank
ALU
Debug
Memory Interface
DAP
Memory Protection Unit
SERIAL WIRE VIEWER
Data watch point
Flash patch
BUS MATRIX
ROM MEMORY
SRAM MEMORY


1
2
3
4
5
6
Fetch
Decode
Execute



The ARM Architecture

- Arithmetic Logic Unit
- Booth multiplier
- Barrel shifter
- Control unit
- Register file

Arithmetic Logic Unit (ALU)

The ALU has two 32-bits inputs. The primary comes from the register file, whereas the other comes from the shifter. Status registers flags modified by the ALU outputs. The V-bit output goes to the V flag as well as the Count goes to the C flag. Whereas the foremost significant bit really represents the S flag, the ALU output operation is done by NORed to get the Z flag. The ALU has a 4-bit function bus that permits up to 16 opcode to be implemented.

Booth Multiplier Factor

The multiplier factor has 3 32-bit inputs and the inputs return from the register file. The multiplier output is barely 32-Least Significant Bits of the merchandise. The entity representation of the multiplier factor is shown in the above block diagram. The multiplication starts whenever the beginning 04 input goes active. Fin of the output goes high when finishing.

Booth Algorithm

Booth algorithm is a noteworthy multiplication algorithmic rule for 2's complement numbers. This treats positive and negative numbers uniformly. Moreover, the runs of 0's or 1's within the multiplier factor are skipped over without any addition or subtraction being performed, thereby creating possible quicker multiplication. The figure shows the simulation results for the multiplier test bench. It's clear that the multiplication finishes only in16 clock cycle.

Barrel Shifter

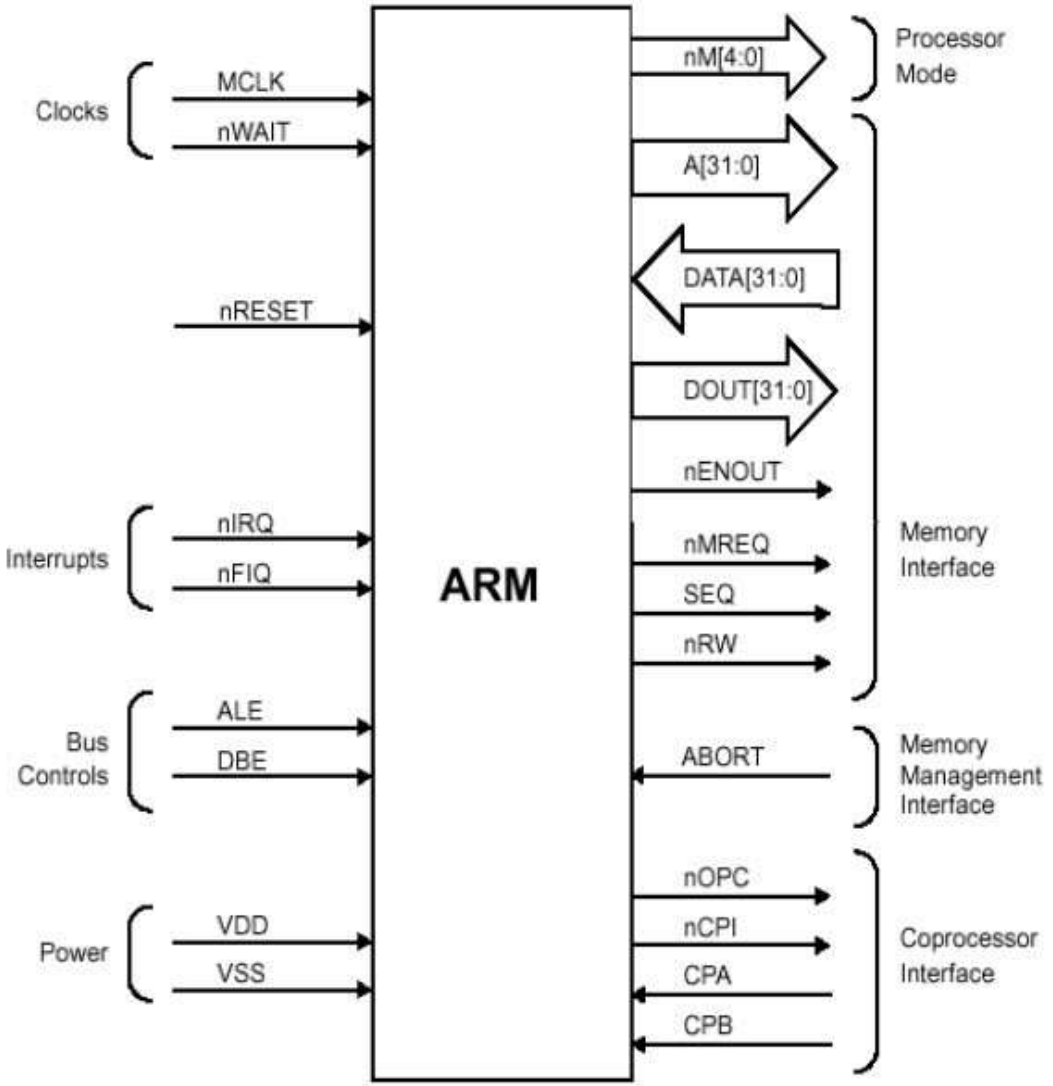
The barrel shifter features a 32-bit input to be shifted. This input is coming back from the register file or it might be immediate data. The shifter has different control inputs coming back from the instruction register. The Shift field within the instruction controls the operation of the barrel shifter. This field indicates the kind of shift to be performed (logical left or right, arithmetic right or rotate right). The quantity by which the register ought to be shifted is contained in an immediate field within the instruction or it might be the lower 6 bits of a register within the register file.

The shift_val input bus is 6-bits, permitting up to 32 bit shift. The shifttype indicates the needed shift sort of 00, 01, 10, 11 are corresponding to shift left, shift right, an arithmetic shift right and rotate right, respectively. The barrel shifter is especially created with multiplexers.

Control Unit

For any microprocessor, control unit is the heart of the whole process and it is responsible for the system operation,so the control unit design is the most important part within the whole design. The control unit is sometimes a pure combinational circuit design. Here, the control unit is implemented by easy state machine. The processor timing is additionally included within the control unit. Signals from the control unit are connected to each component within the processor to supervise its operation.

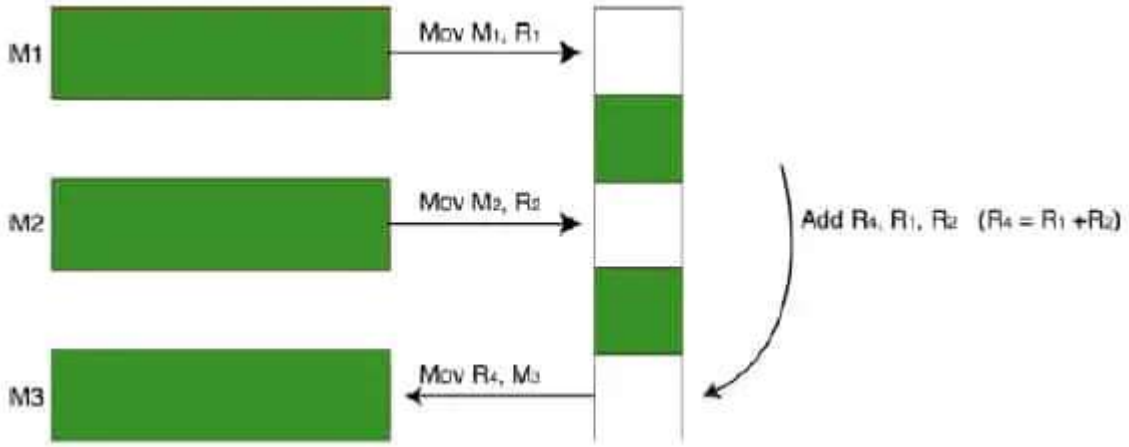
FUNCTIONAL BLOCK DIAGRAM



ARM7 REGISTERS

The ARM-7 is a load and store architecture, where if you want to perform any data processing instructions, then first the data has to move from a memory store into a set of central registers, the data processing instruction has to be executed and then the data again stored back into the memory.

The central set of registers are a bank of 16 registers from R0 – R15. Each of these registers is having 32-bit wide whereas R0 – R12 are user registers and R13 – R15 having some special functions. Where the R13 is called a Stack Pointer (SP), R14 is called Linked Register (**LR**), and the **R15** is the Program Counter (**PC**).

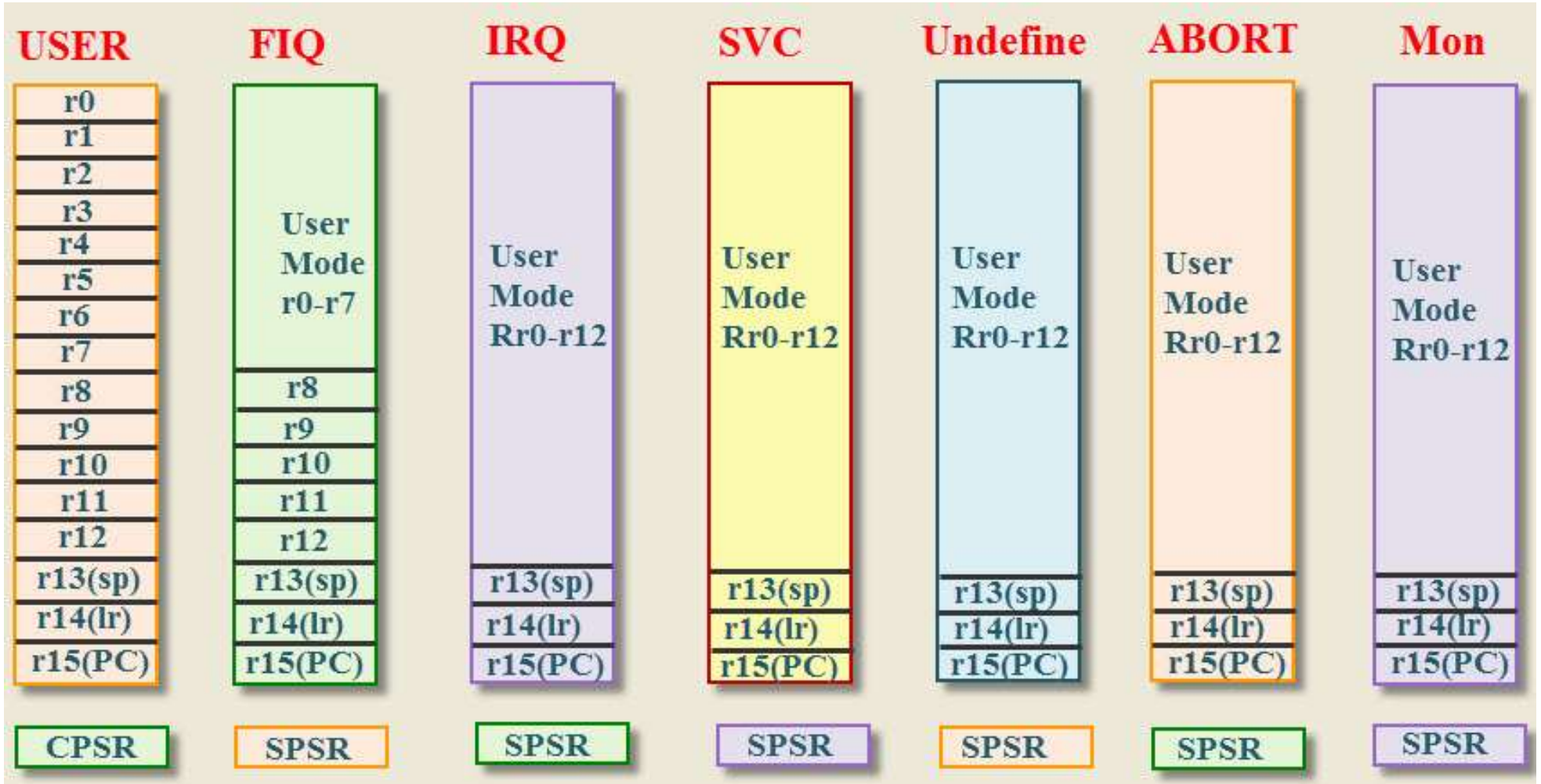


ARM Microcontroller Register Modes

An ARM micrcontroller is a load store reducing instruction set computer architecture means the core cannot directly operate with the memory. The data operations must be done by the registers and the information is stored in the memory by an address. The ARM cortex-M3 consists of 37 register sets wherein 31 are general purpose registers and 6 are status registers.

The ARM uses seven processing modes to run the user task.

- USER Mode
- FIQ Mode
- IRQ Mode
- SVC Mode
- UNDEFINED Mode
- ABORT Mode
- Monitor Mode


USER
FIQ
IRQ
SVC
Undefine
ABORT
Mon
r0
r1
r2
r3
r4
r5
r6
r7
r8
r9
r10
r11
r12
r13(sp)
r14(lr)
r15(PC)
User Mode r0-r7
User Mode Rr0-r12
CPSR
SPSR

USER Mode: The user mode is a normal mode, which has the least number of registers. It doesn't have SPSR and has limited access to the CPSR.

FIQ and IRQ: The FIQ and IRQ are the two interrupt caused modes of the CPU. The FIQ is processing interrupt and IRQ is standard interrupt. The FIQ mode has additional five banked registers to provide more flexibility and high performance when critical interrupts are handled.

SVC Mode: The Supervisor mode is the software interrupt mode of the processor to start up or reset.

Undefined Mode: The Undefined mode traps when illegal instructions are executed. The ARM core consists of 32-bit data bus and faster data flow.

THUMB Mode: In THUMB mode 32-bit data is divided into 16-bits and increases the processing speed.

THUMB-2 Mode: In THUMB-2 mode the instructions can be either 16-bit or 32-bit and it increases the performance of the ARM cortex –M3 microcontroller. The ARM cortex-m3 microcontroller uses only THUMB-2 instructions.

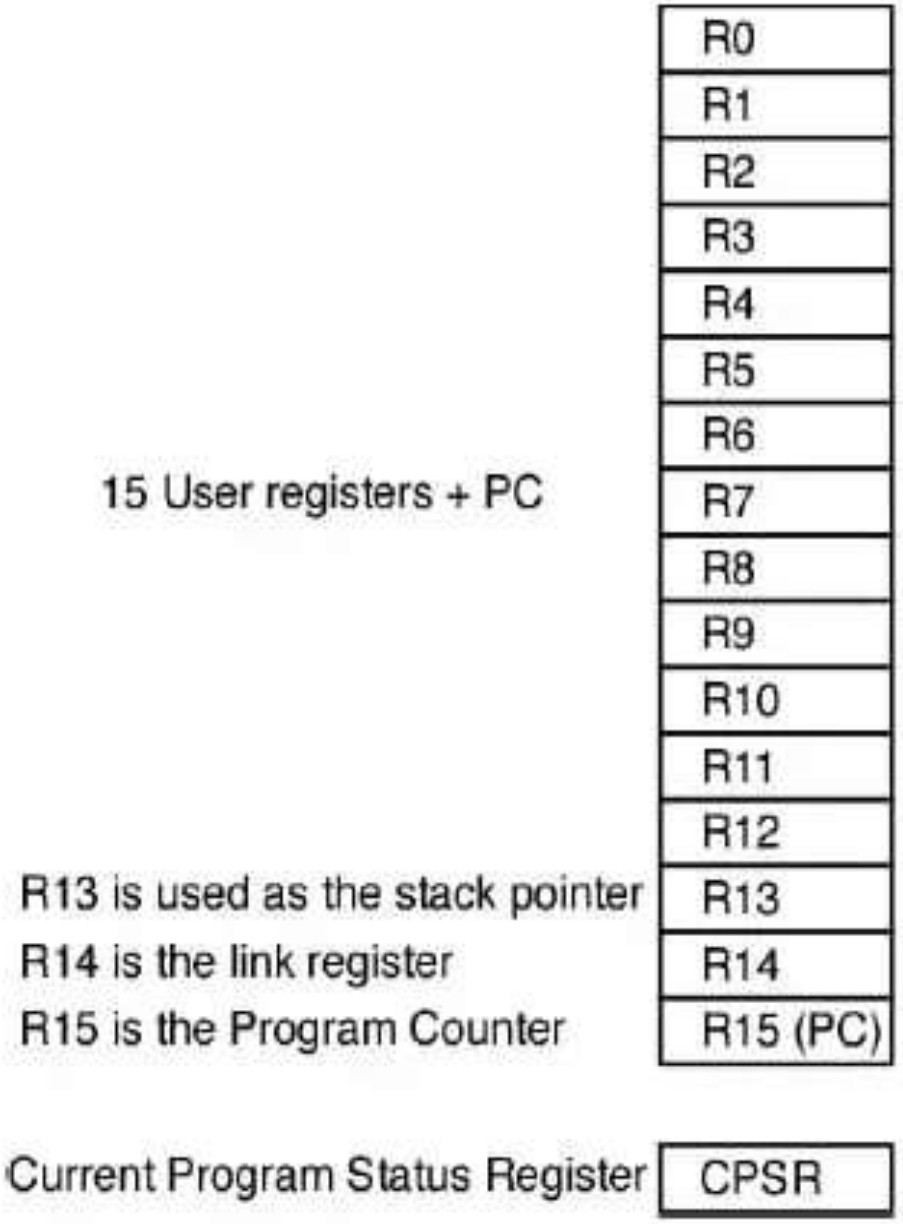
Some of the registers are reserved in each mode for the specific use of the core. The reserved registers are

- Stack Pointer (SP).
- Link Register (LR).
- Program Counter (PC).
- Current Program Status Register (CPSR).
- Saved Program Status Register (SPSR).

The reserved registers are used for specific functions. The SPSR and CPSR contain the status control bits which are used to store the temporary data. The SPSR and CPSR register have some properties that are defined operating modes, Interrupt enable or disable flags and ALU status flag. The ARM core operates in two states 32-bit state or THUMBS state.

LPC-2148 MICROCONTROLLER

The LPC-2148 is the widely used microcontroller from the ARM-7 family. It is manufactured by Philips and added with many inbuilt peripherals which making it more efficient and also it is more reliable for both beginners and high-end developers to learn and research.


15 User registers + PC
R0
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13 is used as the stack pointer
R13
R14 is the link register
R14
R15 is the Program Counter
R15 (PC)
Current Program Status Register
CPSR

STACK POINTER (SP-R13): The stack pointer is a register called **Stack** inside the processor which stores the address of the next instruction in the which is going to be executed.

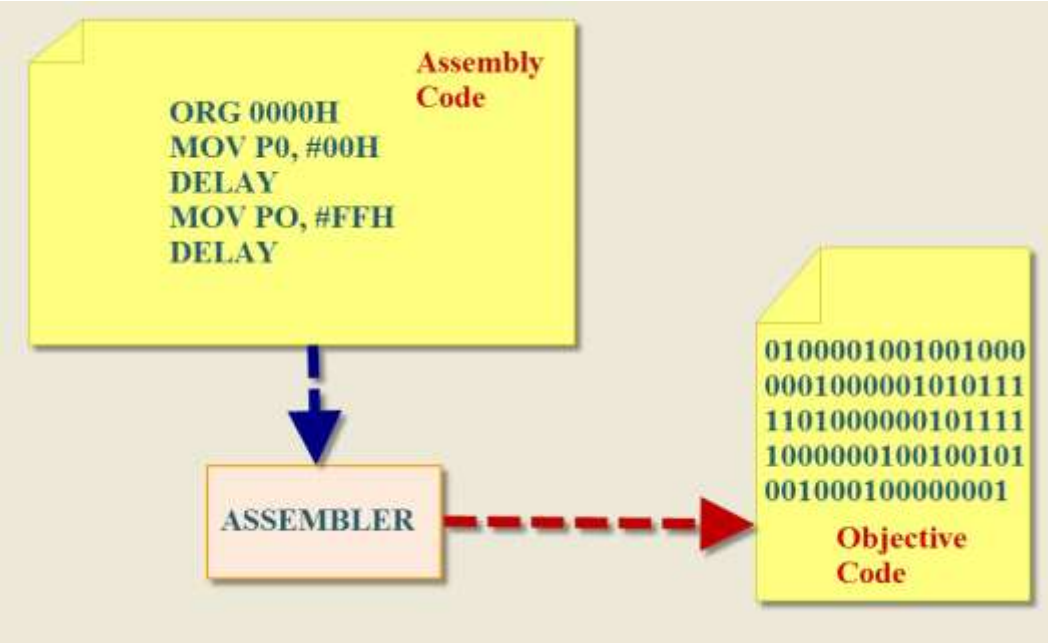
STACK: A stack is a special temporary buffer which stores the data from top-down.

LINKED REGISTER (LR-R14): The R14 is the linked register which stores the return information for subroutines, function calls, and exceptions. On reset, the processor sets the LR value to **0xFFFFFFFF**.

PROGRAM COUNTER (PC-R15): The program counter is the **R15** register in ARM-7 which contains the current address of the instruction which is executing. On reset, the processor loads the PC with the value of the reset vector, which is at address **0x00000004**. Bit[0] of the value is loaded into the **EPSR** T-bit at reset and must be 1.

ARM-Cortex Microcontroller Programming

The ARM microcontrollers runs at 100Mhz frequency and higher performance, therefore it supports the higher level languages. The ARM microcontroller is programmed with different IDES such as keiluvision3, keiluvision4, coocox and so on. A 8-bit microcontroller use 8-bit instructions and the ARM cortex-M uses a 32-instructions.



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Thank you!