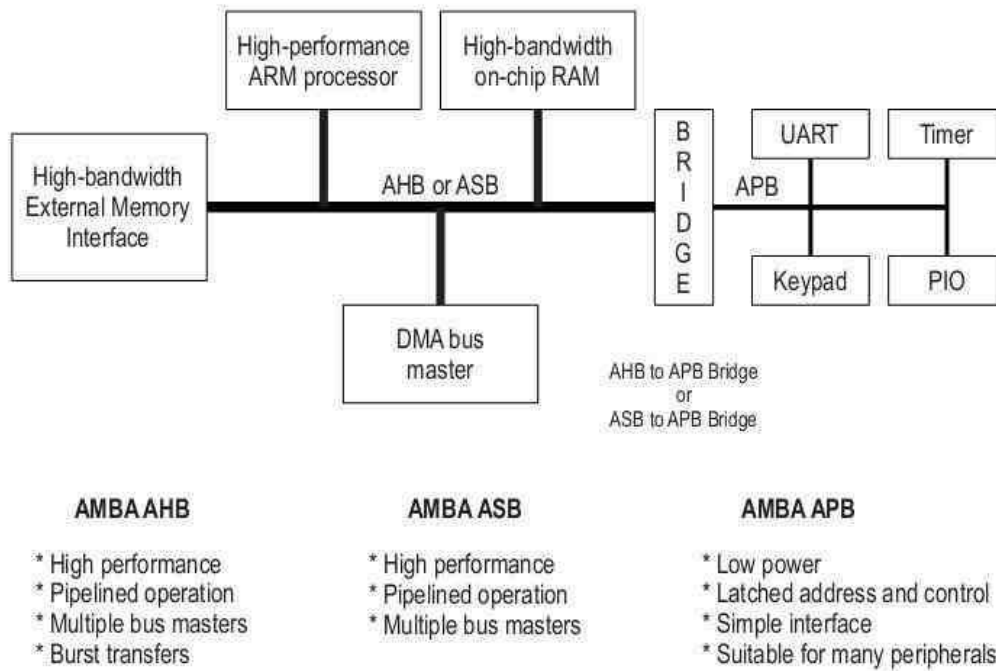# ARM Bus technology

AMBA stands for Advanced Microcontroller Bus Architecture. AMBA specification specifies an on chip communication standard. This is used to design embedded microcontrollers with high performance.

ARM Memory

Memory Width:

Memory width is the number of bits the memory returns on each access-typically 8, 16, 32, or 64 bits.

The memory width has a direct effect on the overall performance and cost ratio. Following table covers fetching instructions from memory.

Instruction size	8 bit memory	16 bit memory	32 bit memory
ARM 32 bit	4 cycles	2 cycles	1 cycle
Thumb 16 bit	2 cycles	1 cycle	1 cycle

Memory types

ROM: Read-only memory (ROM) is the least flexible of all memory types because it contains an image that is permanently set at production time and cannot be reprogrammed. Devices use a ROM to hold boot code Its main use is for holding the device firmware or storing long-term data that needs to be preserved after power is off.

DRAM: Dynamic random access memory (DRAM) is the most commonly used RAM for devices. It has the lowest cost per megabyte compared with other types of RAM. DRAM is dynamic- it needs to have its storage cells refreshed and given a new electronic charge every few milliseconds, so you need to set up a DRAM controller before using the memory.

SRAM: Static random access memory (SRAM) is faster than the more traditional DRAM, but requires more silicon area. SRAM is static-the RAM does not require refreshing.

SDRAM: SDRAM stands for Synchronous Dynamic Random Access Memory. It is one of the DRAM type. It runs at high clock speed compare to conventional memory. It gets synchronize with processor bus as SDRAM is clocked.

ARM peripherals

A peripheral device performs input and output functions for the chip by connecting to other devices or sensors that are off-chip.

All ARM peripherals are memory mapped-the programming interface is a set of memory- addressed registers. The address of these registers is an offset from a specific peripheral base address.

Controllers are specialized peripherals that implement higher levels of functionality within an embedded system.

Memory Controllers

Memory controllers connect different types of memory to the processor bus. On power-up a memory controller is configured in hardware to allow certain memory devices to be active. These memory devices allow the initialization code to be executed. Some memory devices must be set up by software; for example, when using DRAM, you first have to set up the memory timings and refresh rate before it can be accessed.

Interrupt Controllers

There are two types of interrupt controller available for the ARM processor:

Standard interrupt controller: The interrupt handler determines which device requires servicing by reading a device bitmap register in the interrupt controller.

vector interrupt controller (VIC) : Prioritizes interrupts and simplifies the determination of which device caused the interrupt. After associating a priority and a handler address with each interrupt, the VIC only asserts an interrupt signal to the core if the priority of a new interrupt is higher than the currently executing interrupt handler.