SNS COLLEGE OF TECHNOLOGY
(An Autonomous Institution)
COIMBATORE-35
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19EET204 / DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

II YEAR / IV SEMESTER

UNIT-III: DESIGN OF SEQUENTIAL CIRCUITS, PLD, VHDL

PLDs – Program - Examples

TOPIC OUTLINE

PLD Nomenclature

Example problem

Implementation with PROM

with PAL

with PLA

PAL NOMENCLATURE

PAL xxyyzz – IC specification

xx Maximum number of AND array inputs

zz Maximum number of dedicated outputs

yy Type of outputs

Combinational

H	active high
L	active low
P	programmable
C	complementary

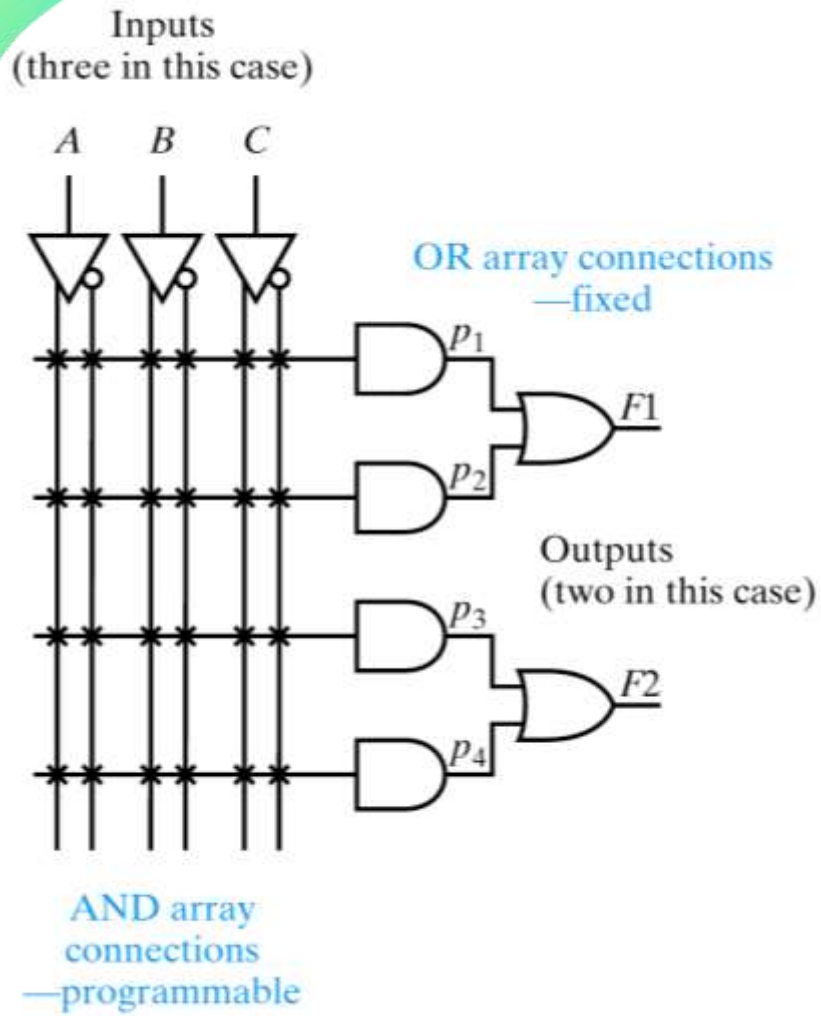
Registered

R	registered
RP	registered, with programmable polarity

Versatile

V	programmable as combinational or registered

Nomenclature Examples



PAL3H2

- 3 inputs
- 2 outputs
- Active H outputs

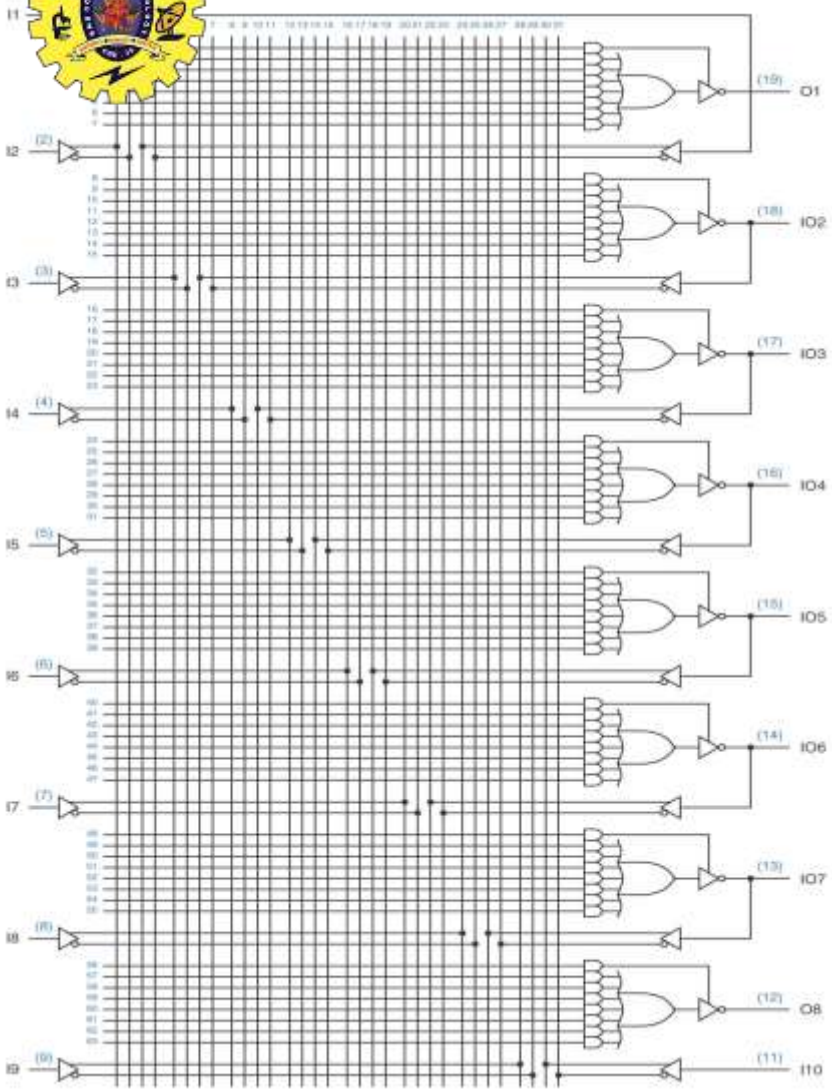
PAL16L8

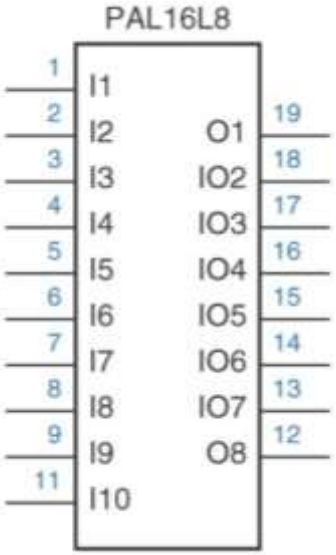
- 16 inputs
- 8 outputs
- Active L (0s of function)

PAL22V10

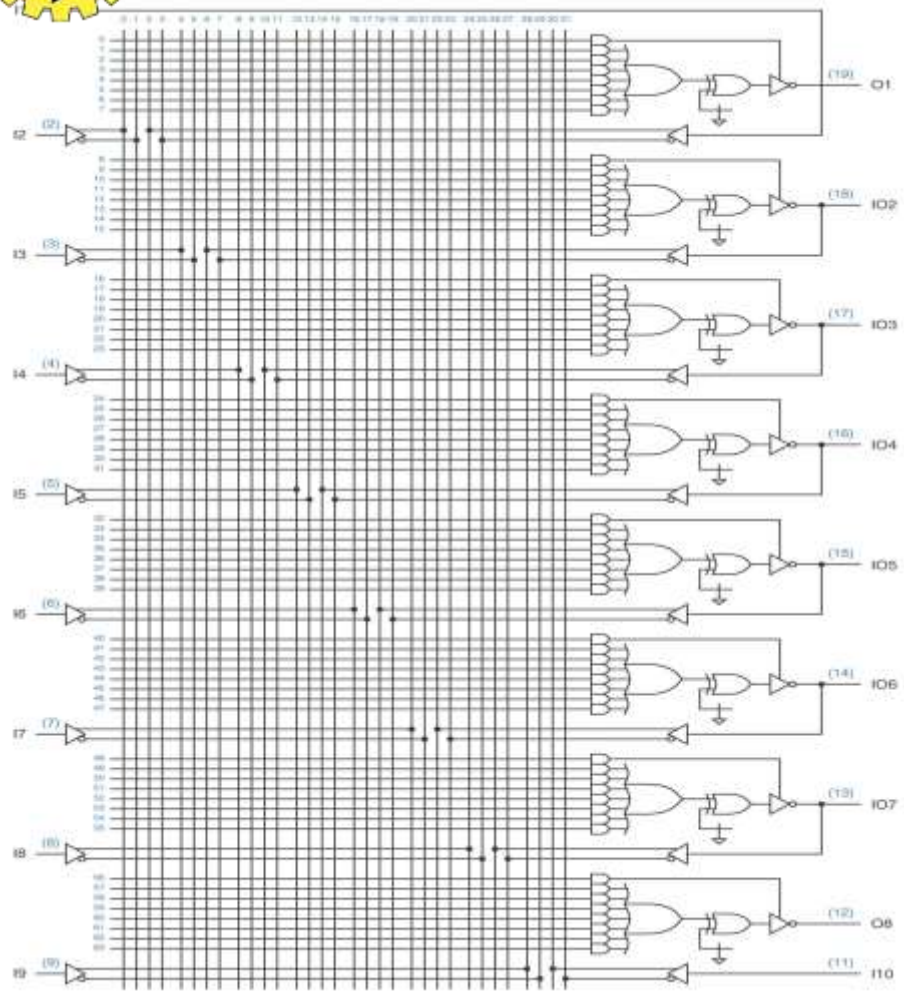
- 22 inputs
- 10 outputs
- Active L or H (1s or 0s)
- Registered if desired

PAL


I1
I2
I3
I4
I5
I6
I7
I8
I9
(19) O1
(18) IO2
(17) IO3
(16) IO4
(15) IO5
(14) IO6
(13) IO7
(12) O8
(11) I10


PAL16L8
1 I1
2 I2
3 I3
4 I4
5 I5
6 I6
7 I7
8 I8
9 I9
11 I10
O1 19
IO2 18
IO3 17
IO4 16
IO5 15
IO6 14
IO7 13
O8 12

GAL



Emulate any PAL

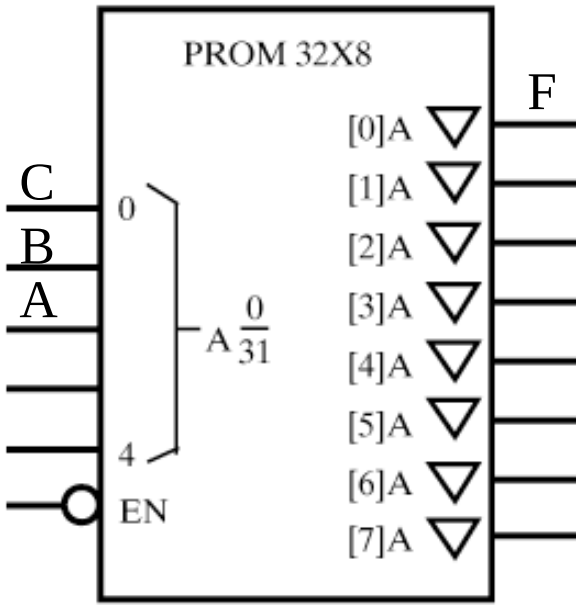
Reprogrammable

- Fuses are non-volatile memory cells

Designing with PROMs

Additional functions/outputs – wider bit word

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



PROM

Address	Data
00000	0XXXXXXX
00001	0XXXXXXX
00010	1XXXXXXX
00011	0XXXXXXX
00100	0XXXXXXX
00101	0XXXXXXX
00110	1XXXXXXX
00111	1XXXXXXX

EXAMPLE

Implement:

- an inverter (NOT)
- an OR gate
- a NAND gate
- an XOR gate

With:

- a PROM
- a PLA
- a PAL

A	B	F1	F2	F3	F4
0	0	1	0	1	0
0	1	1	1	1	1
1	0	0	1	1	1
1	1	0	1	0	0

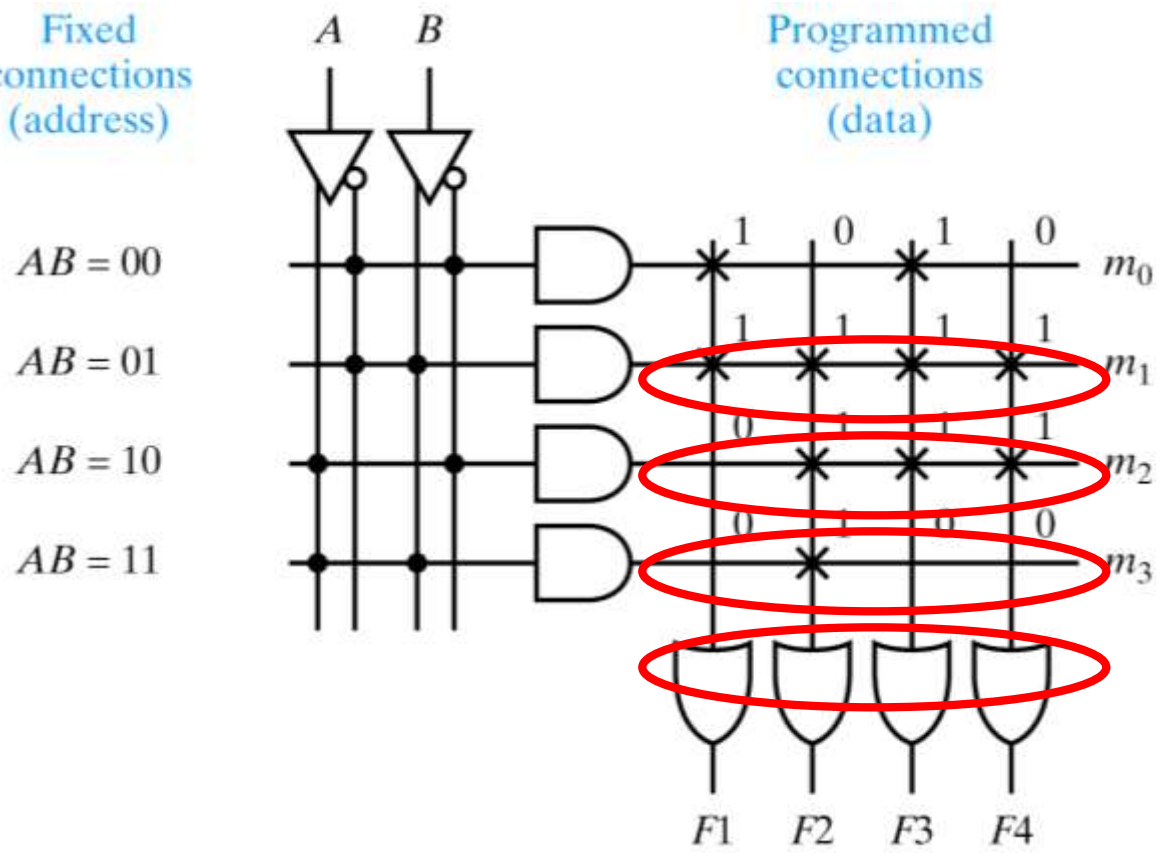
PROM Implementation

NOT, OR, NAND, XOR

A	B	F1	F2	F3	F4
0	0	1	0	1	0
0	1	1	1	1	1
1	0	0	1	1	1
1	1	0	1	0	0

Fuse map

Address	Data
0	A
1	F
2	7
3	4

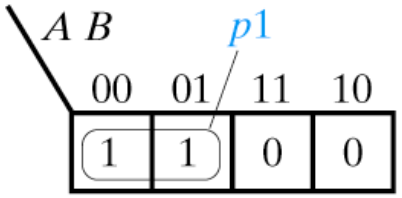


PLA Implementation

A	B	F1	F2	F3	F4
0	0	1	0	1	0
0	1	1	1	1	1
1	0	0	1	1	1
1	1	0	1	0	0

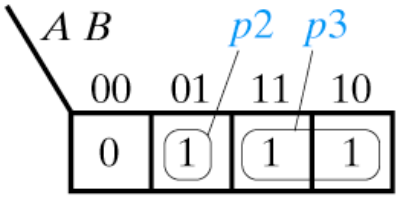
NOT, OR, NAND, XOR

$F1 =$



$F1 = p1 = \overline{A}$

$F2 =$

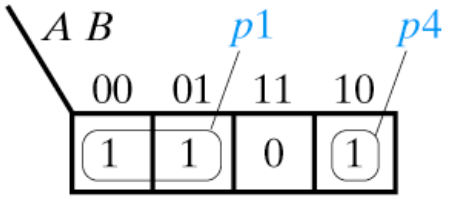


$F2 = p2 + p3$

$= \overline{A} \cdot B + A$

$= A + B$

$F3 =$



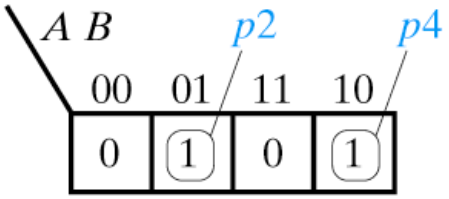
$F3 = p1 + p4$

$= A + A \cdot \overline{B}$

$= A + B$

$= \overline{\overline{A} \cdot B}$

$F4 =$



$F4 = p2 + p4$

$= \overline{A} \cdot B + A \cdot \overline{B}$

$= A \oplus B$

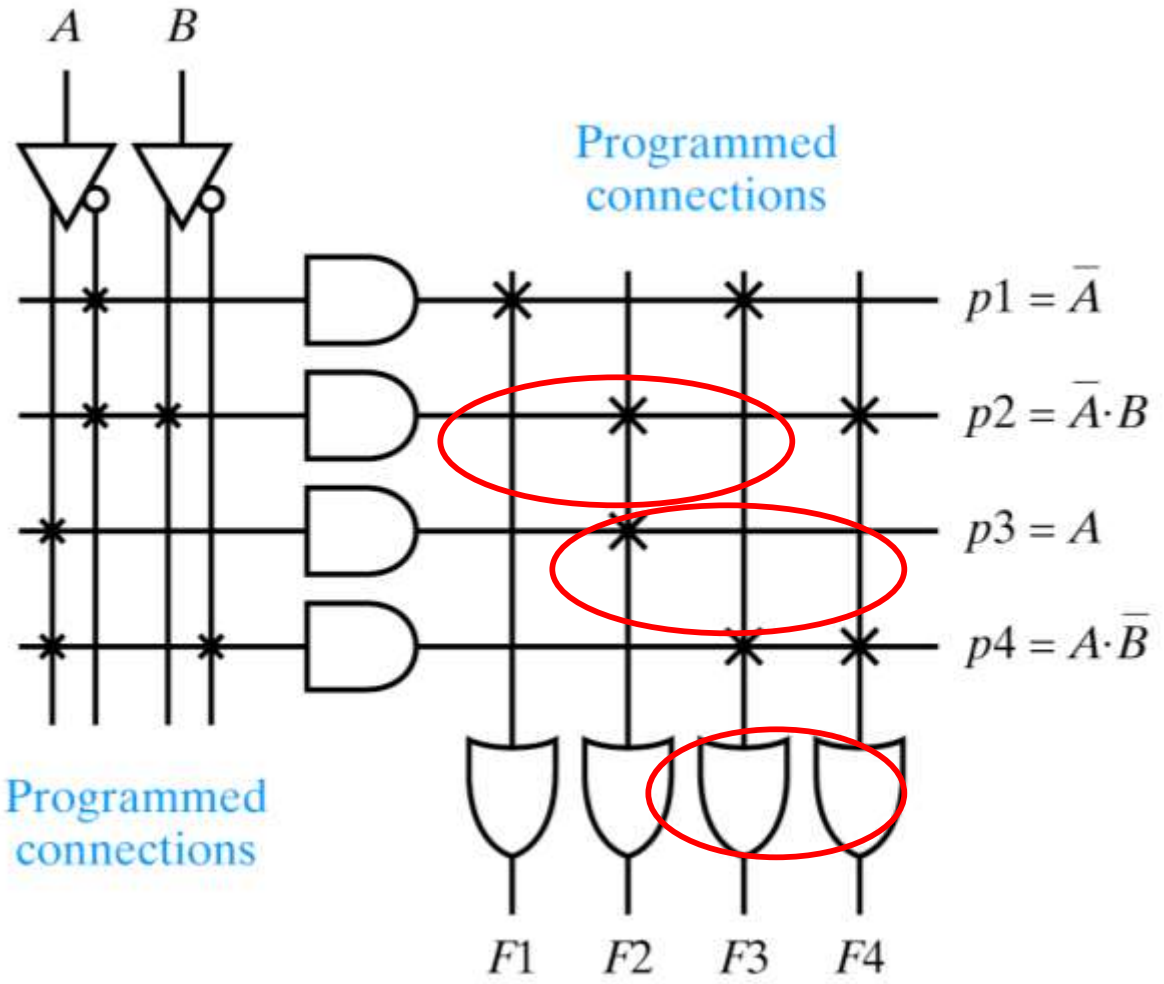
- What would have happened if we'd chosen a different covering for the K-map for F3?
- Same number of terms…
- Unable to share since the B' term isn't used anywhere else

PLA Implementation

NOT, OR, NAND, XOR

A	B	F1	F2	F3	F4
0	0	1	0	1	0
0	1	1	1	1	1
1	0	0	1	1	1
1	1	0	1	0	0

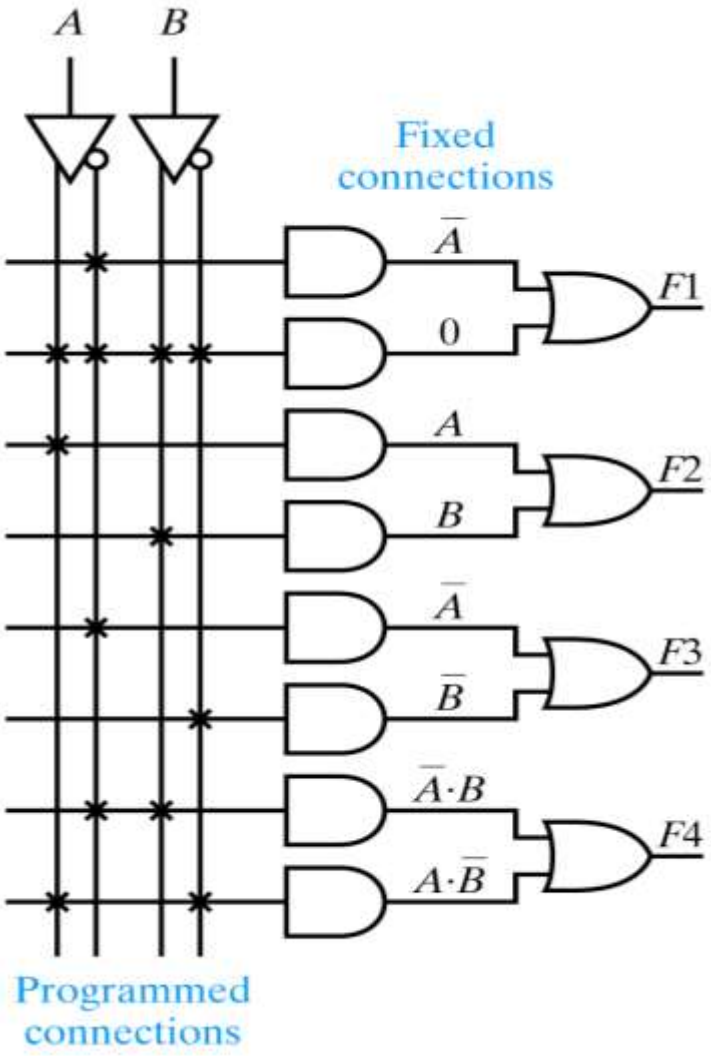
- What are the shared product terms?
- Highlight in red



PAL Implementation

NOT, OR, NAND, XOR

A	B	F1	F2	F3	F4
0	0	1	0	1	0
0	1	1	1	1	1
1	0	0	1	1	1
1	1	0	1	0	0



RECAP..

Thank You