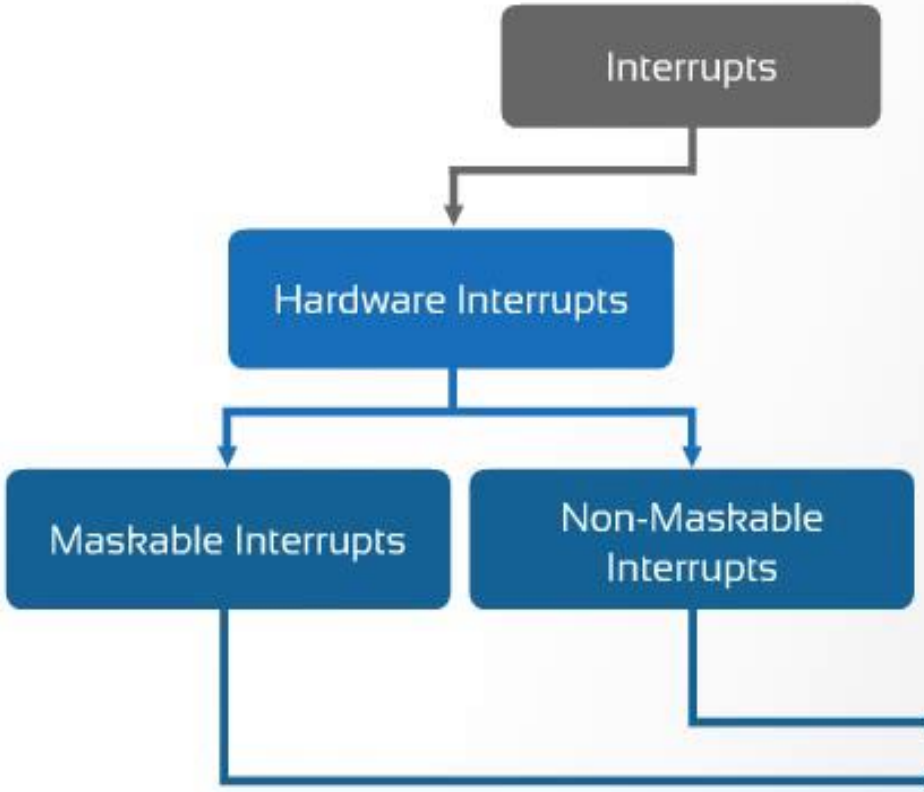
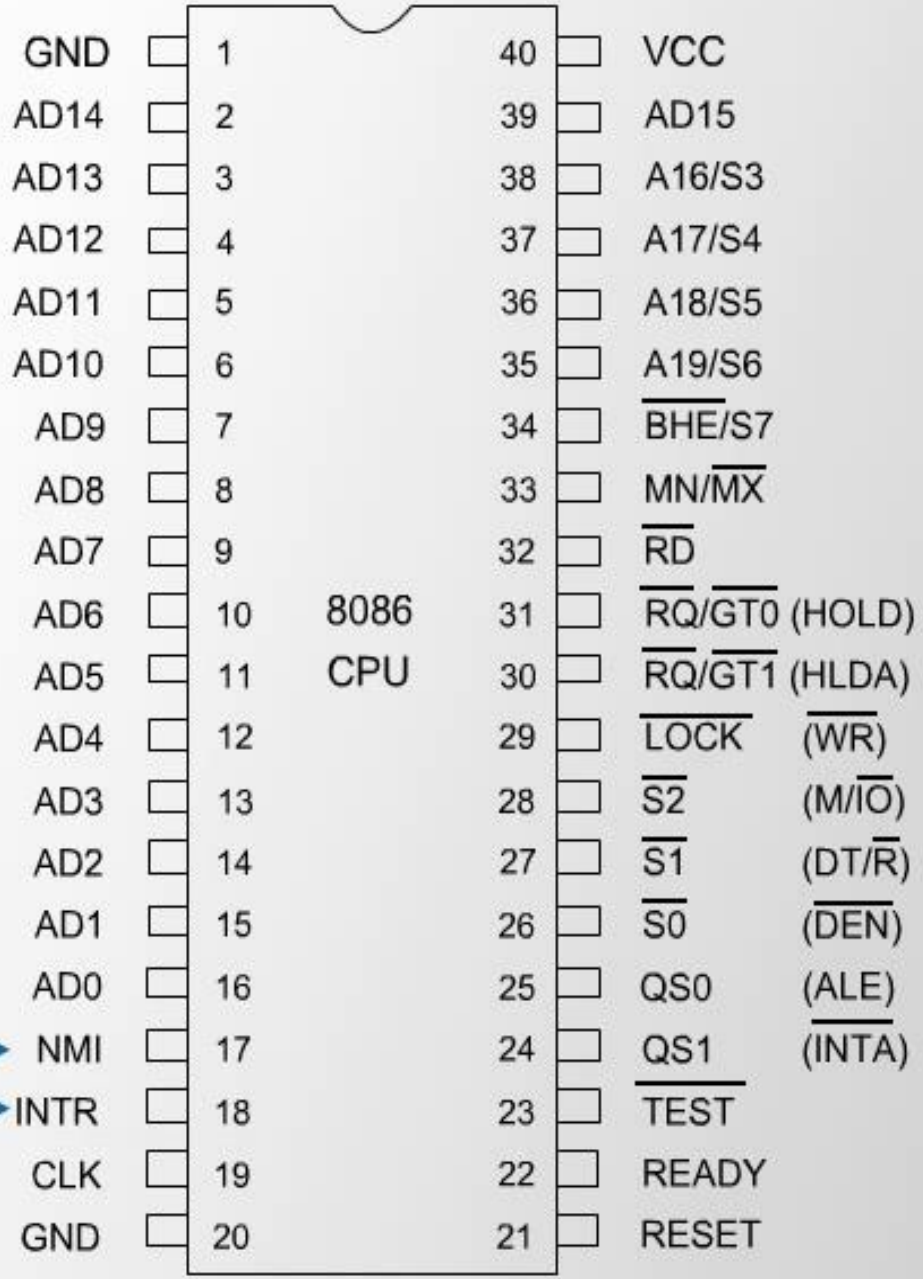
INTERRUPT CONTROLLER

INTEL 8259


Interrupts
Hardware Interrupts
Maskable Interrupts
Non-Maskable Interrupts

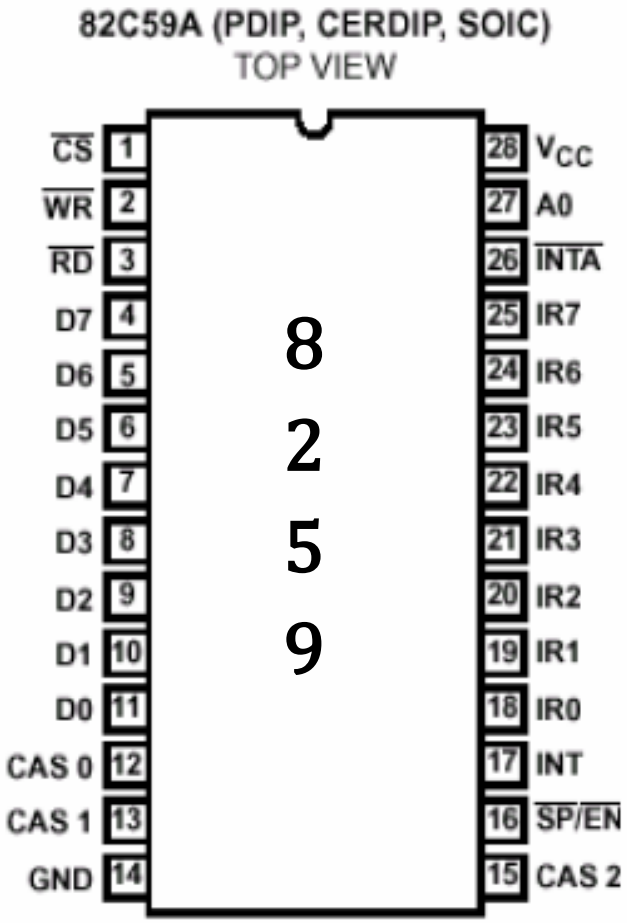
8086 CPU


GND 1
AD14 2
AD13 3
AD12 4
AD11 5
AD10 6
AD9 7
AD8 8
AD7 9
AD6 10
AD5 11
AD4 12
AD3 13
AD2 14
AD1 15
AD0 16
NMI 17
INTR 18
CLK 19
GND 20
8086 CPU
40 VCC
39 AD15
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
34 BHE/S7
33 MN/MX
32 RD
31 RQ/GT0 (HOLD)
30 RQ/GT1 (HLDA)
29 LOCK (WR)
28 S2 (M/IO)
27 S1 (DT/R)
26 S0 (DEN)
25 QS0 (ALE)
24 QS1 (INTA)
23 TEST
22 READY
21 RESET

8259 Programmable Interrupt Controller (PIC)

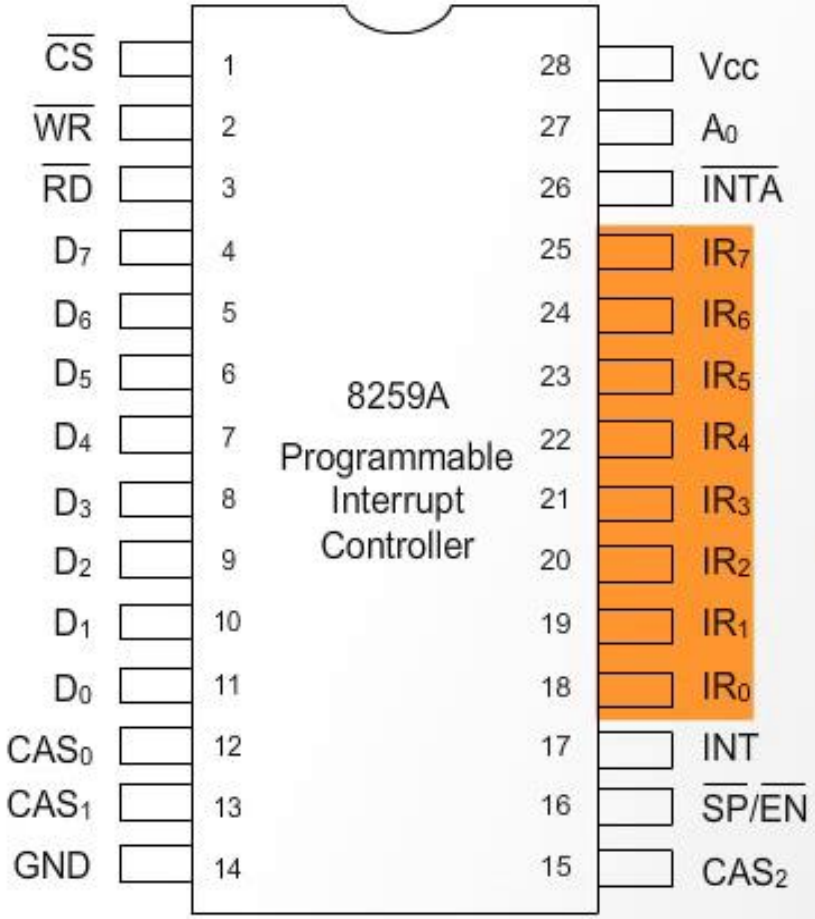
1. This IC is designed to simplify the implementation of the interrupt interface in the 8088 and 8086 based microcomputer systems.
2. This device is known as a 'Programmable Interrupt Controller' or PIC.
3. It is manufactured using the NMOS technology and It is available in 28-pin DIP.
4. The operation of the PIC is programmable under software control (Programmable)and it can be configured for a wide variety of applications.
5. 8259A is treated as peripheral in a microcomputer system.
6. 8259A PIC adds eight vectored priority encoded interrupts to the microprocessor.
7. This controller can be expanded without additional hardware to accept up to 64 interrupt request inputs. This expansion required a master 8259A and eight 8259A slaves.
8. Some of its programmable features are:
    - The ability to accept level-triggered or edge-triggered inputs.
    - The ability to be easily cascaded to expand from 8 to 64 interrupt-inputs.
    - Its ability to be configured to implement a wide variety of priority schemes.

8259A PIC- PIN DIGRAM



PIN	DESCRIPTION
D7 - D0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS 2 - CAS 0	Cascade Lines
$\overline{SP/EN}$	Slave Program Input Enable
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 - IR7	Interrupt Request Inputs

8259 PIC



Upto eight Hardware Interrupting devices are supported.

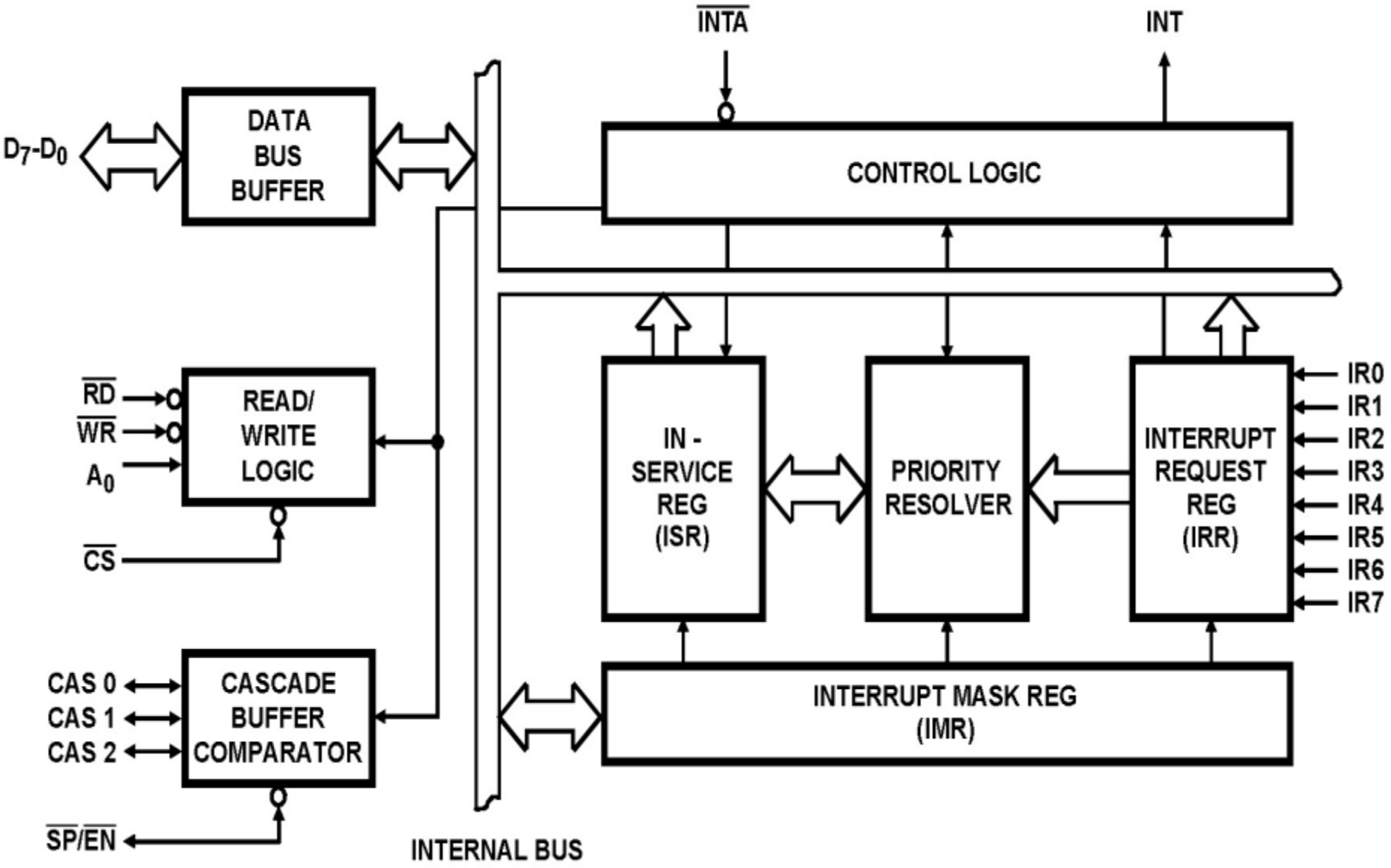
The processor is interrupted whenever the Interrupting device delivers a signal to the 8259.

ASSINGMENT OF SIGNALS FOR 8259:

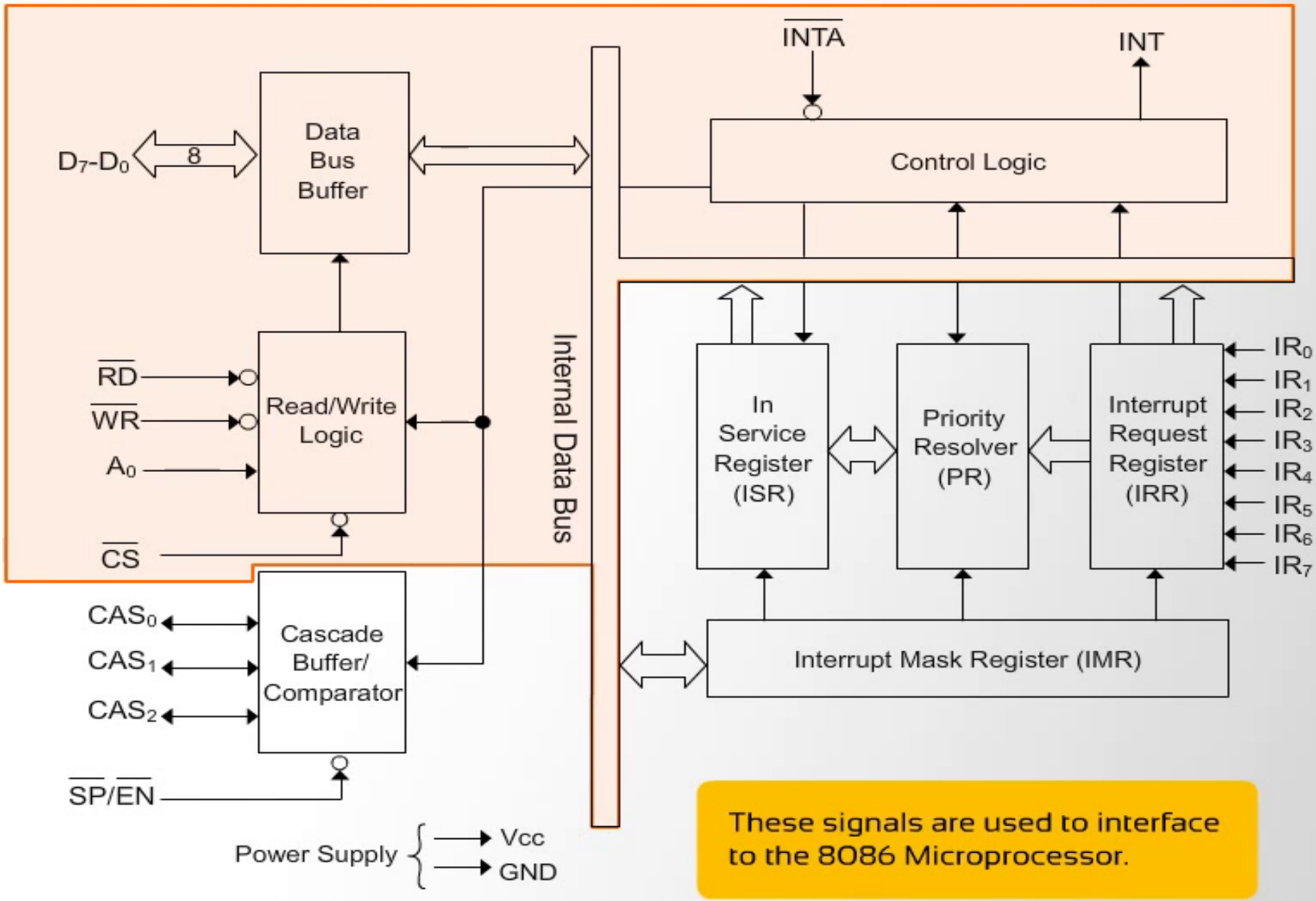
1. **D7- D0** is connected to microprocessor data bus D7-D0 (AD7-AD0).
2. **IR7- IR0**, Interrupt Request inputs are used to request an interrupt and to connect to a slave in a system with multiple 8259As.
3. **$\overline{WR}$ -** the write input connects to write strobe signal of microprocessor.
4. **$\overline{RD}$ -** the read input connects to the IORC signal.
5. **INT -** the interrupt output connects to the INTR pin on the microprocessor from the master, and is connected to a master IR pin on a slave.
6. **$\overline{INTA}$ -** the interrupt acknowledge is an input that connects to the INTA signal on the system. In a system with a master and slaves, only the master INTA signal is connected.
7. **A0** - this address input selects different command words within the 8259A.
8. **$\overline{CS}$** - chip select enables the 8259A for programming and control.
9. **$\overline{SP}/\overline{EN}$ -** Slave Program/Enable Buffer is a dual-function pin.

- When the 8259A is in buffered mode, this pin is an output that controls the data bus transceivers in a large microprocessor-based system.
- When the 8259A is not in buffered mode, this pin programs the device as a master (1) or a slave (0).
- CAS2-CAS0, the cascade lines are used as outputs from the master to the slaves for cascading multiple 8259As in a system.

8259A PIC- BLOCK DIAGRAM

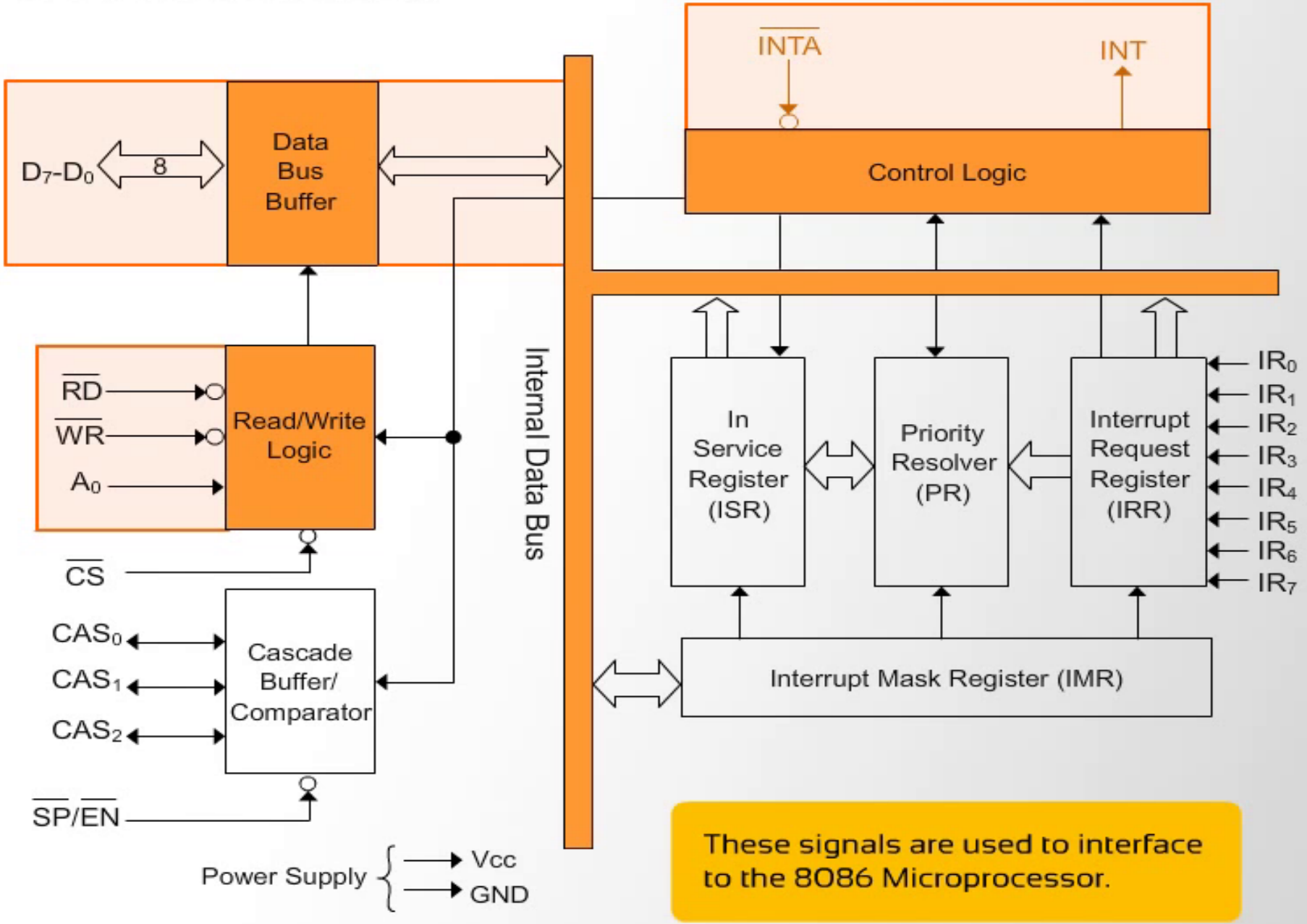


The Internals of 8259



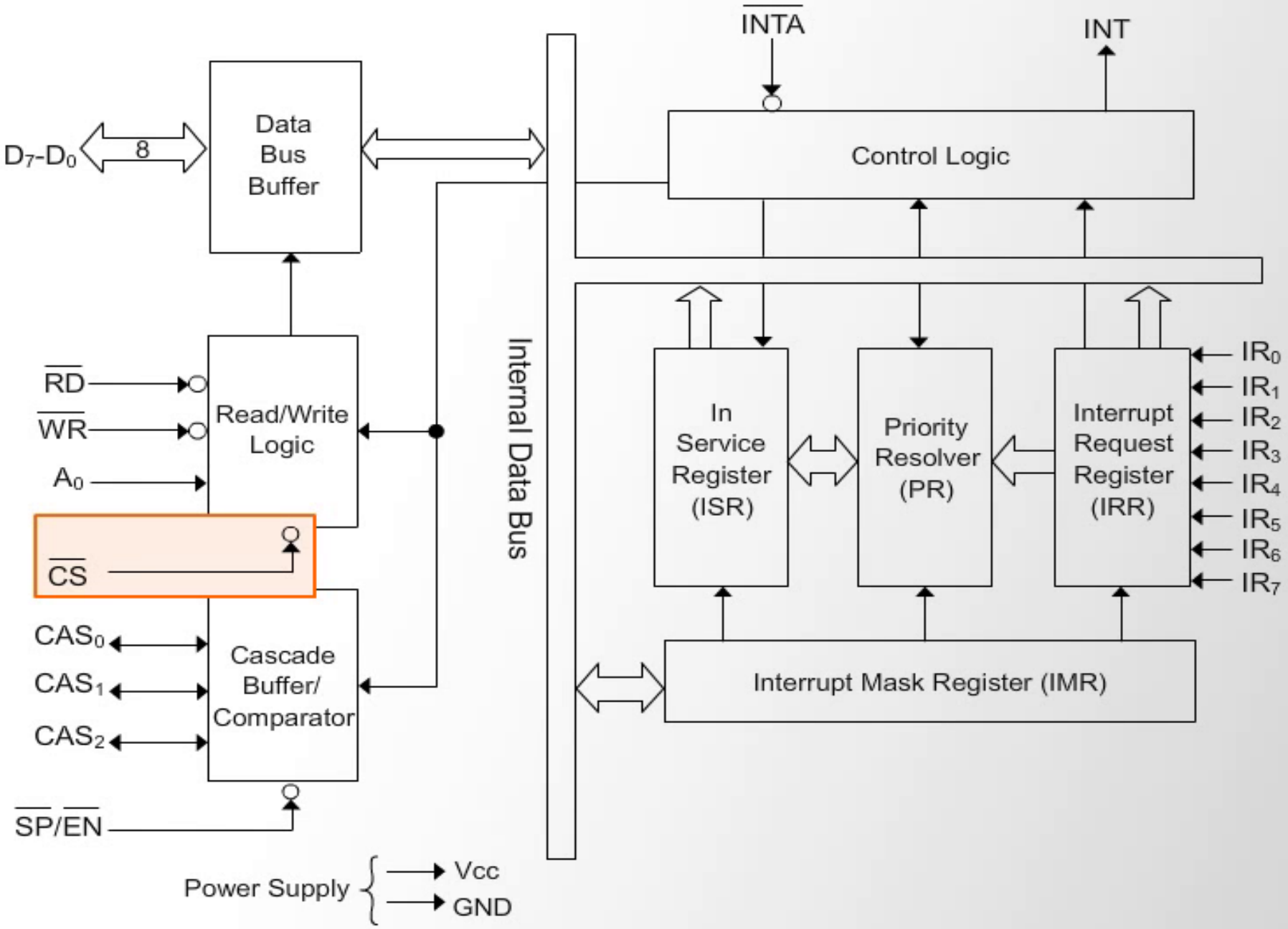
These signals are used to interface to the 8086 Microprocessor.

The Internals of 8259

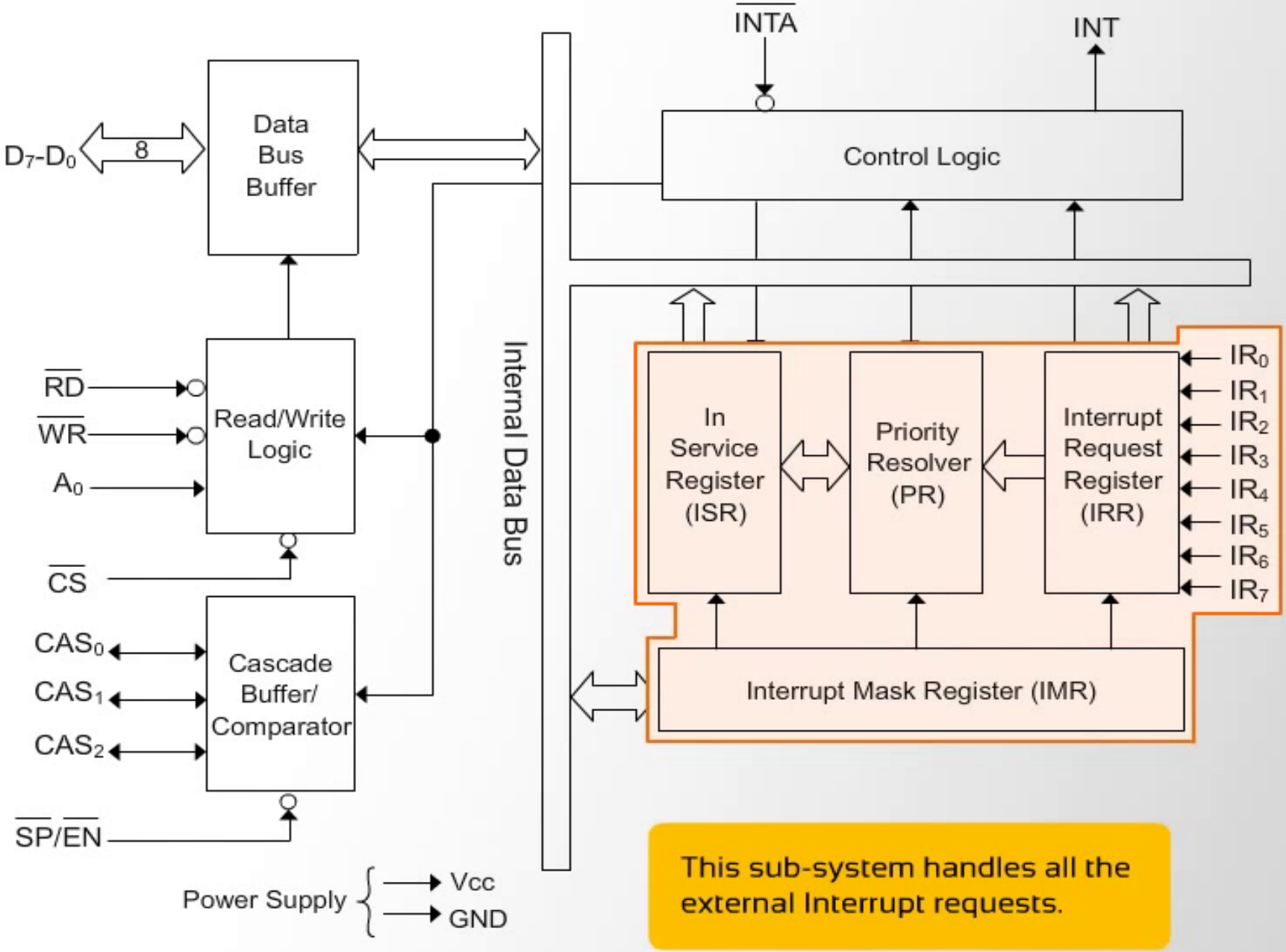


These signals are used to interface to the 8086 Microprocessor.

The Internals of 8259

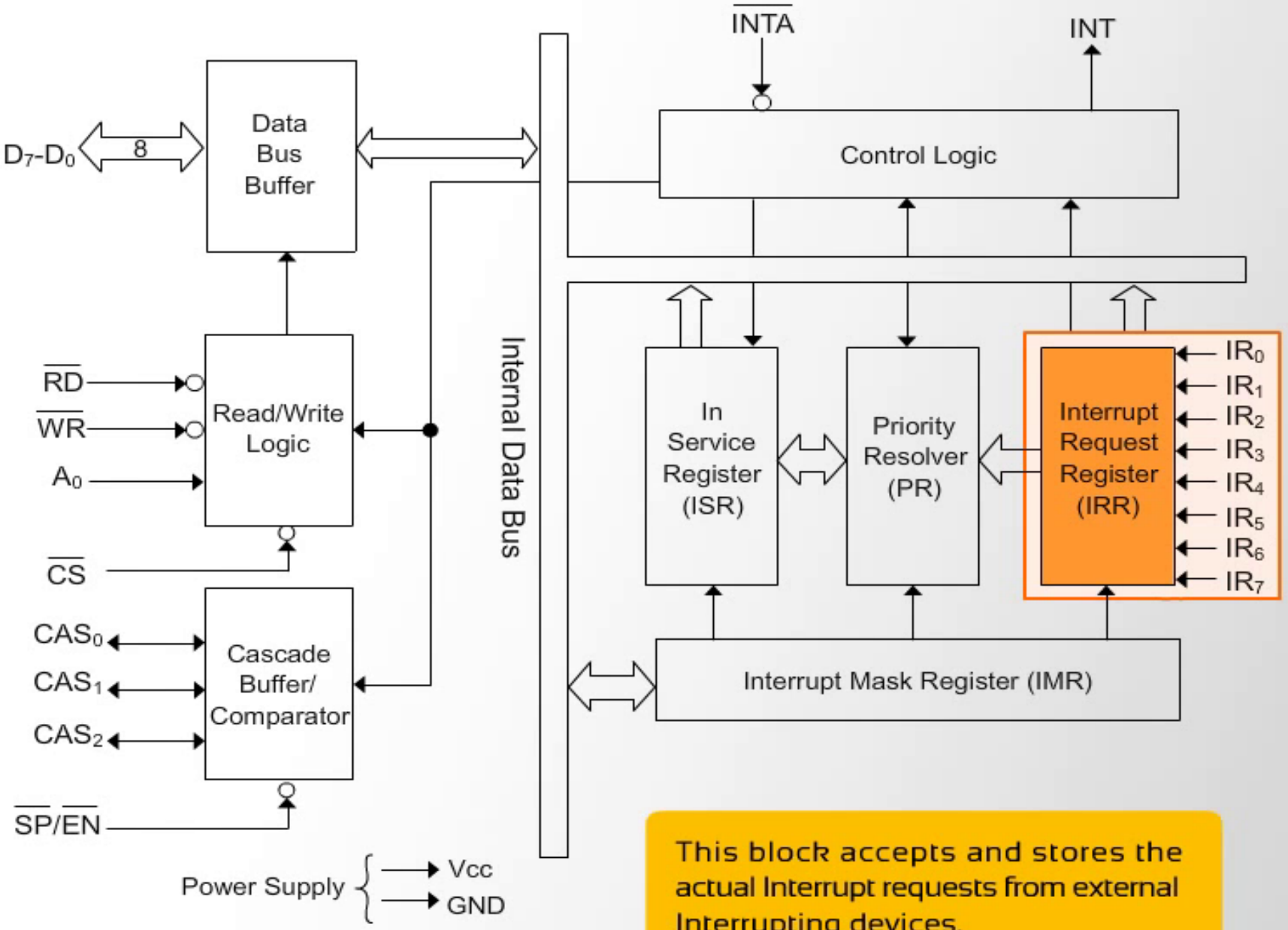


The Internals of 8259



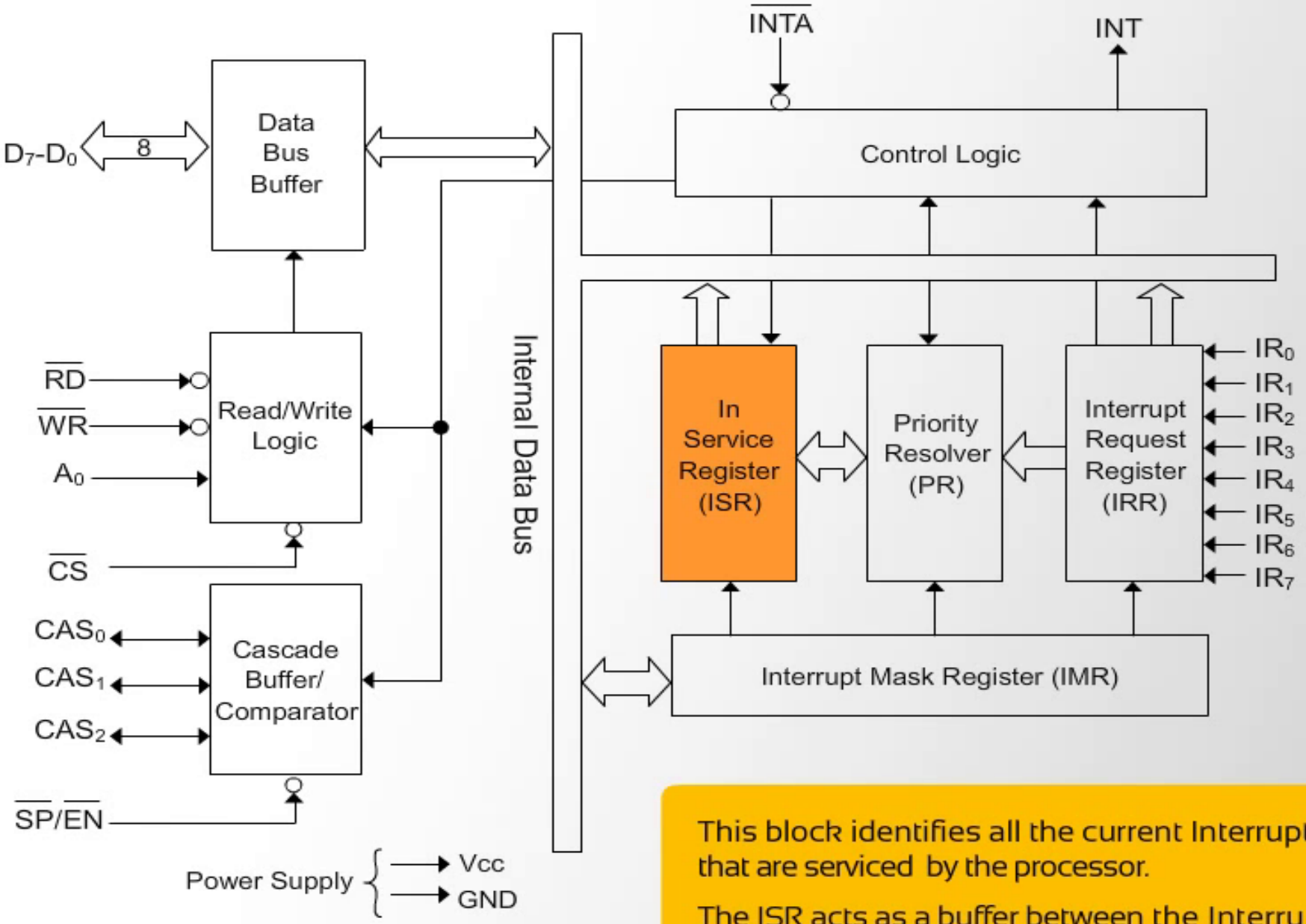
This sub-system handles all the external Interrupt requests.

The Internals of 8259



This block accepts and stores the actual Interrupt requests from external Interrupting devices.

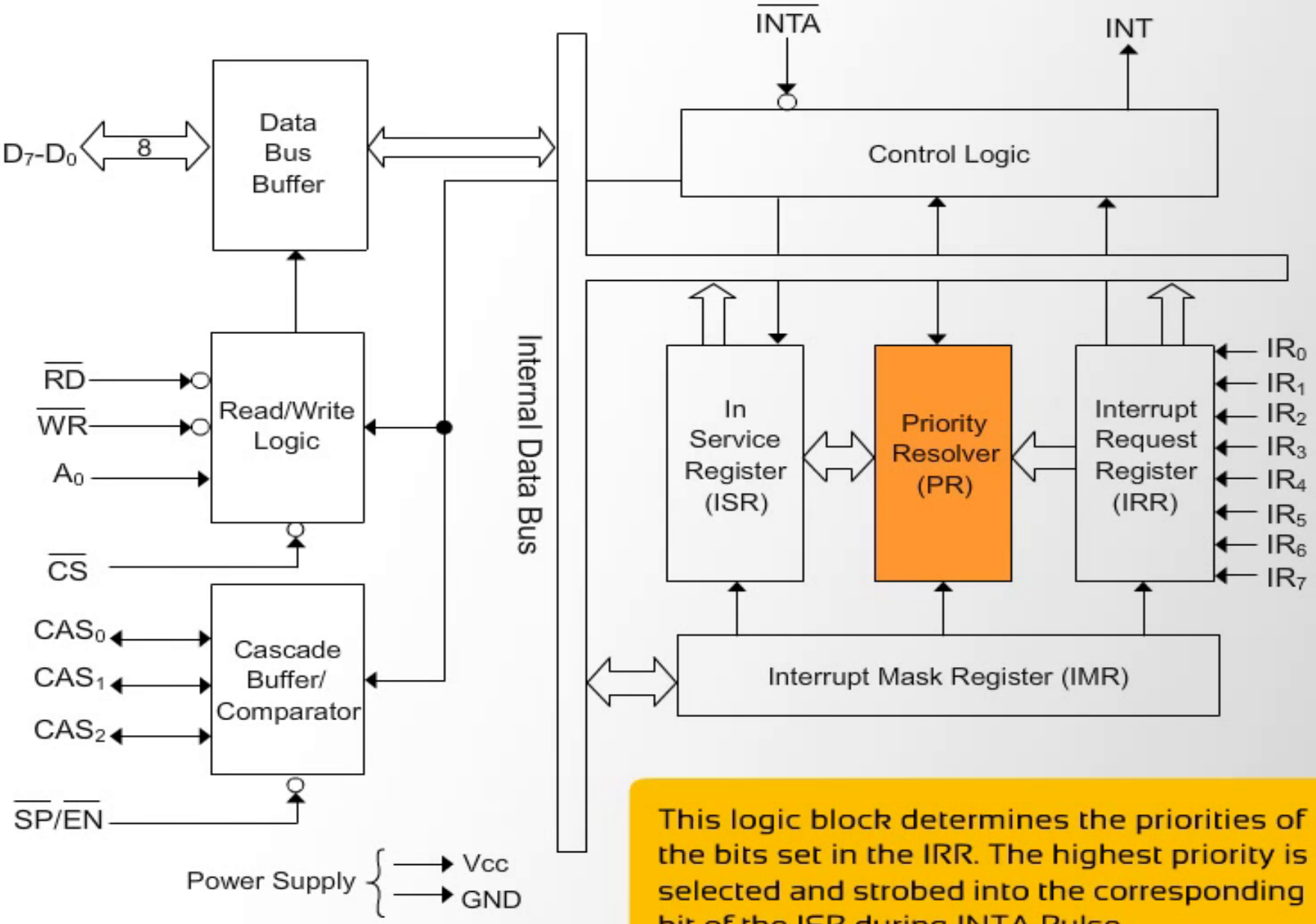
The Internals of 8259



This block identifies all the current Interrupts that are serviced by the processor.

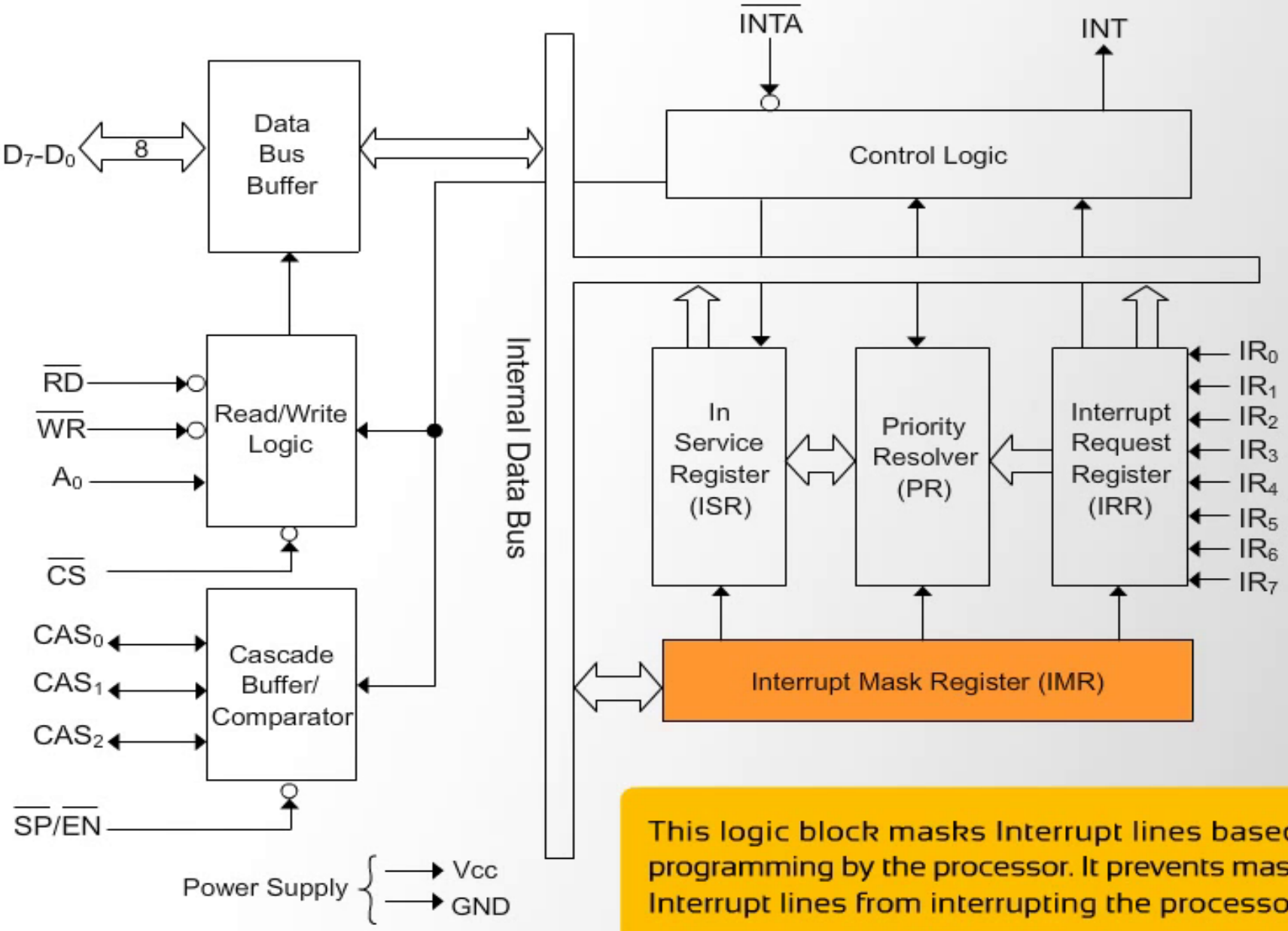
The ISR acts as a buffer between the Interrupt Request Register and the 8086.

The Internals of 8259



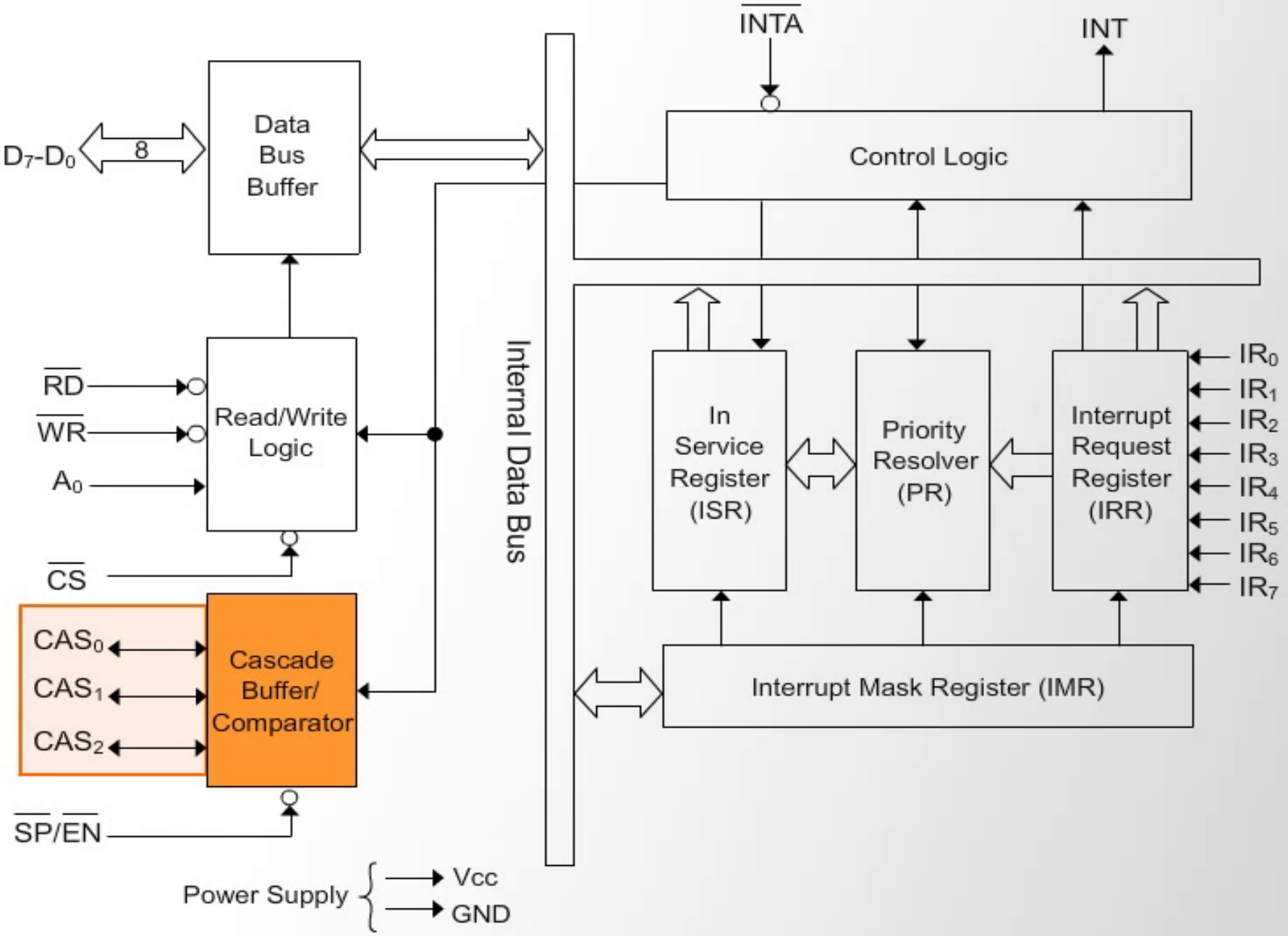
This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during INTA Pulse.

The Internals of 8259

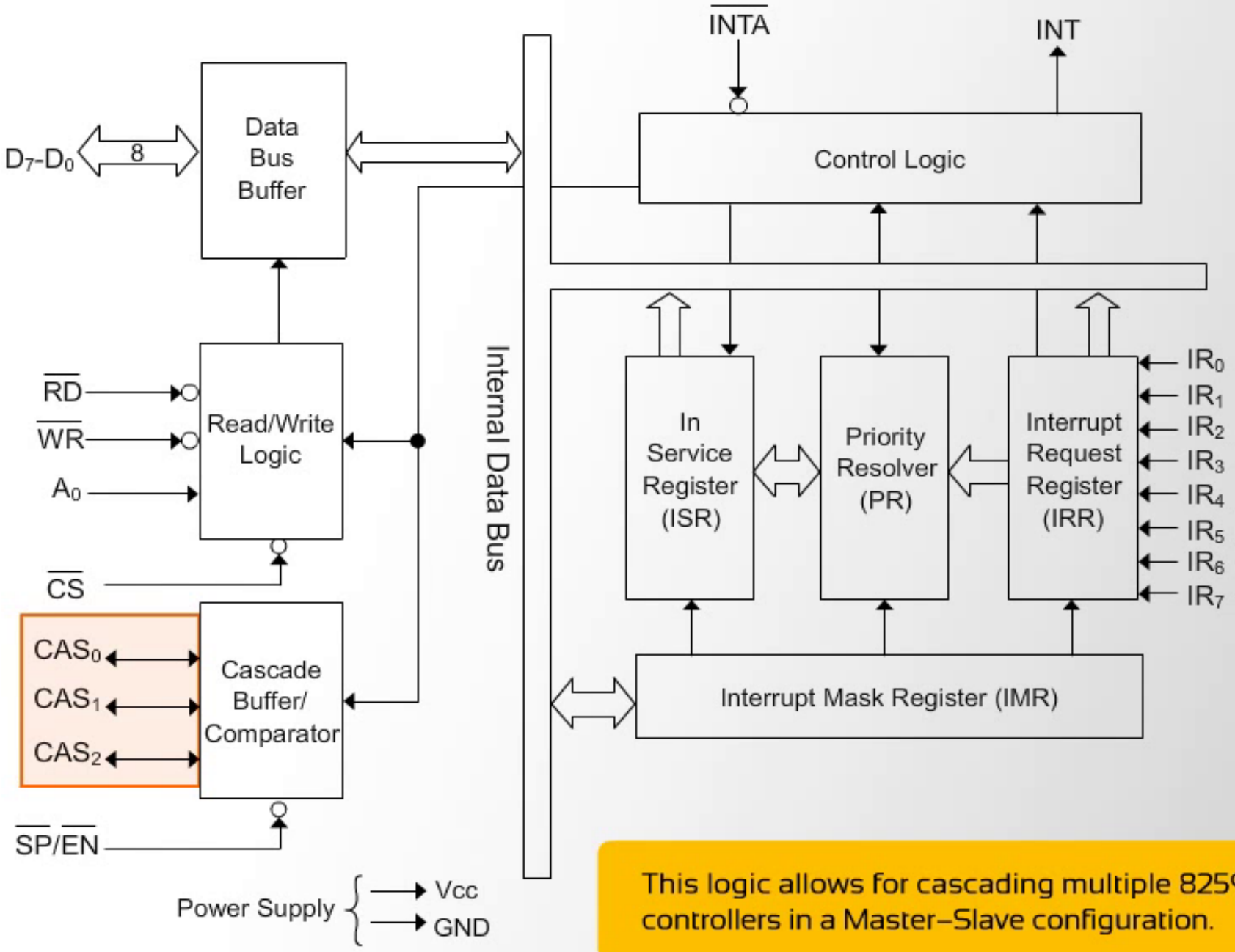


This logic block masks Interrupt lines based on programming by the processor. It prevents masked Interrupt lines from interrupting the processor.

The Internals of 8259

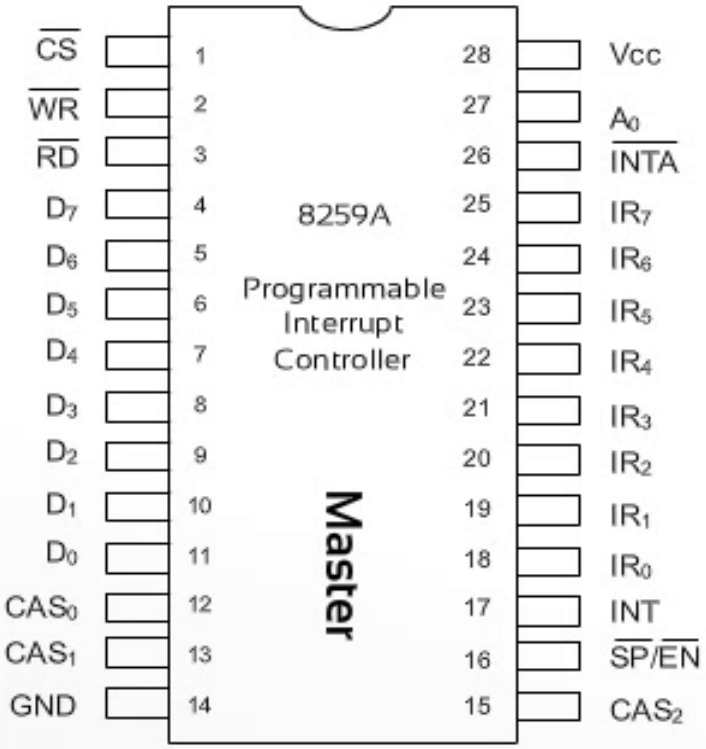


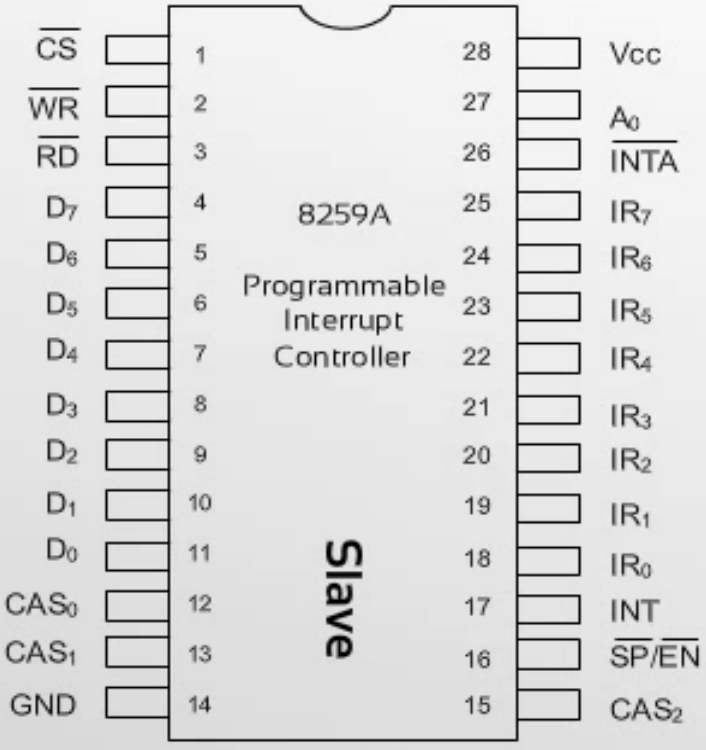
The Internals of 8259



This logic allows for cascading multiple 8259 controllers in a Master–Slave configuration.

Master–Slave Concept in 8259





Master–Slave Concept in 8259

Master–Slave Concept in 8259

Master–Slave Concept in 8259

Master–Slave Concept in 8259

Master–Slave Concept in 8259

Master–Slave Concept in 8259

Programming the 8259A: -

The 82C59A accepts two types of command words generated by the CPU:

1. **Initialization Command Words (ICWs):**

   Before normal operation can begin, each 82C59A in the system must be brought to a starting point - by a sequence of 2 to 4 bytes timed by WR pulses.

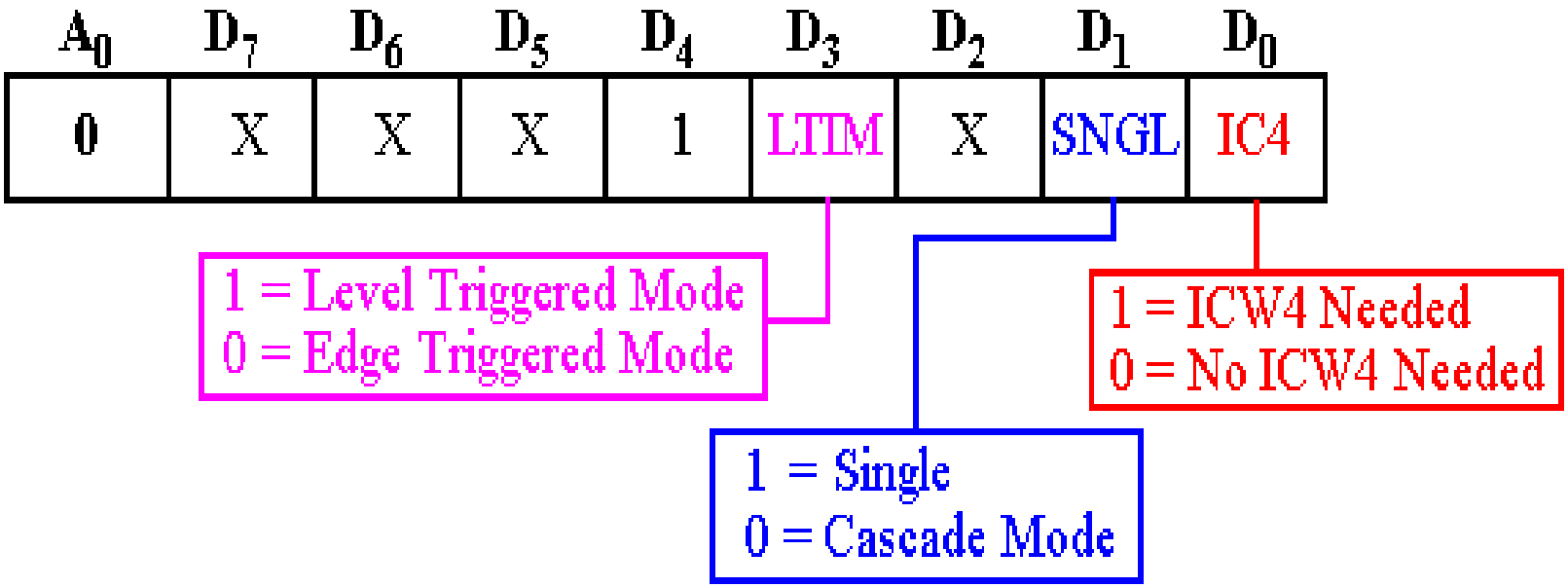
2. **Operational Command Words (OCWs):**

   These are the command words which command the 82C59A to operate in various interrupt modes. Among these modes are:

   a. Fully nested mode.
   b. Rotating priority mode.
   c. Special mask mode.
   d. Polled mode.

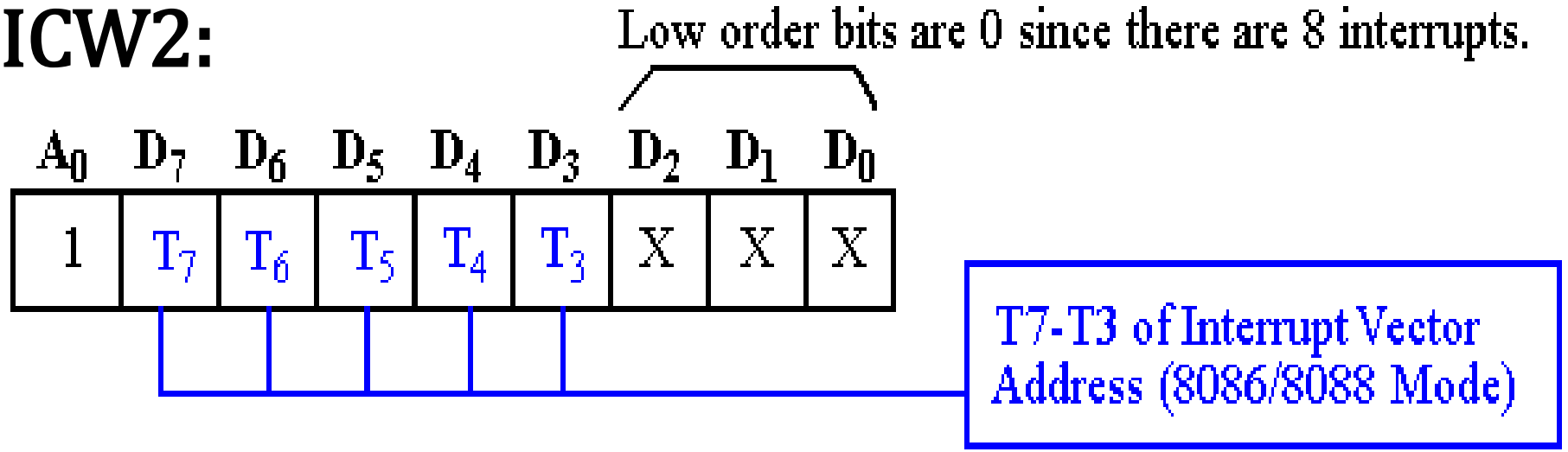
The OCWs can be written into the 82C59A anytime after initialization.

ICW1:



- To program this ICW for 8086 we place a logic 1 in bit IC4.
- Bits D7, D6 , D5and D2 are don't care for microprocessor operation and only apply to the 8259A when used with an 8-bit 8085 microprocessor.
- This ICW selects single or cascade operation by programming the SNGL bit. If cascade operation is selected, we must also program ICW3.
- The LTIM bit determines whether the interrupt request inputs are positive edge triggered or level-triggered.

ICW2:

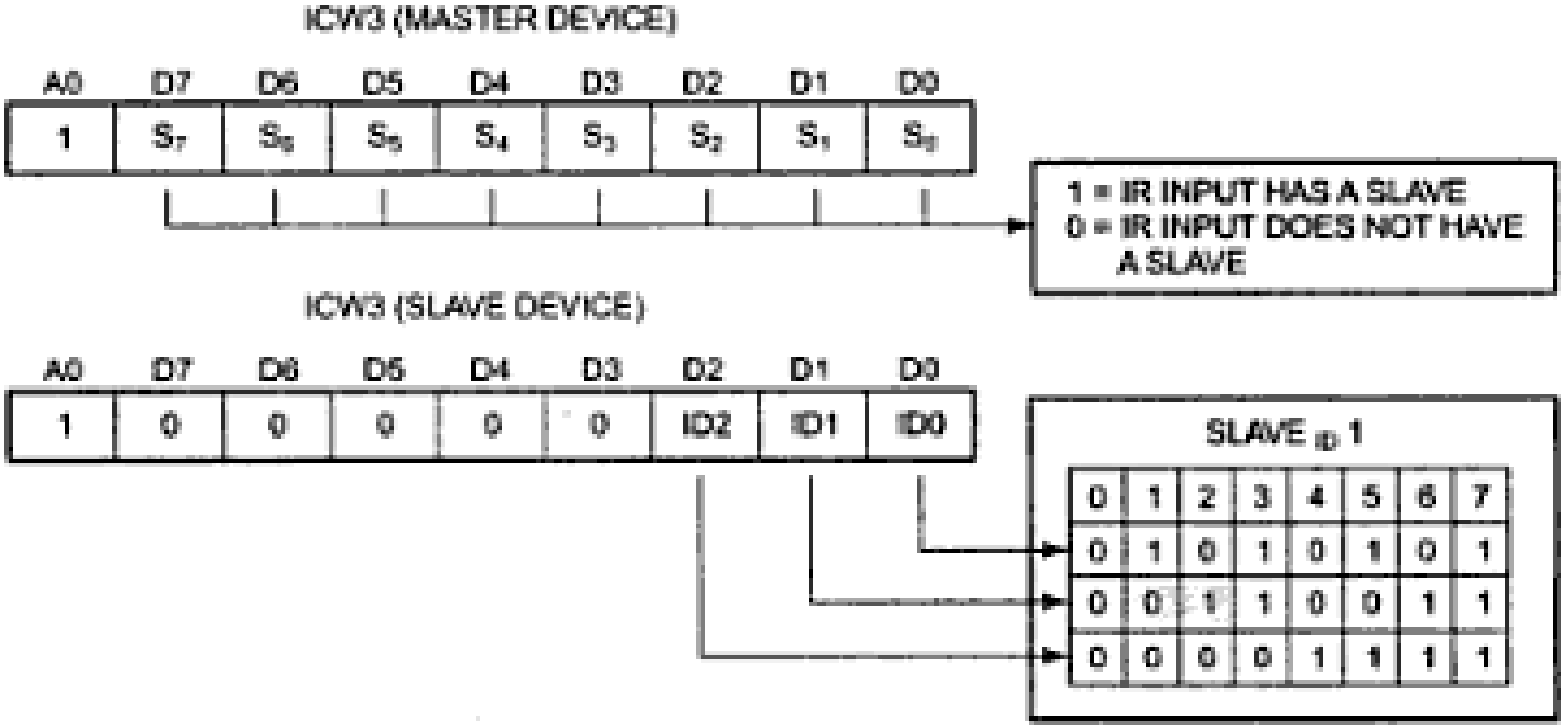


- Selects the vector number used with the interrupt request inputs.
- For example, if we decide to program the 8259A so that it functions at vector locations 08H-0FH, we place a 08H into this command word.
- Likewise, if we decide to program the 8259A for vectors 70H-77H, we place a 70H in this ICW.

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	T_7	T_6	T_5	T_4	T_3	A_{10}	A_9	A_8

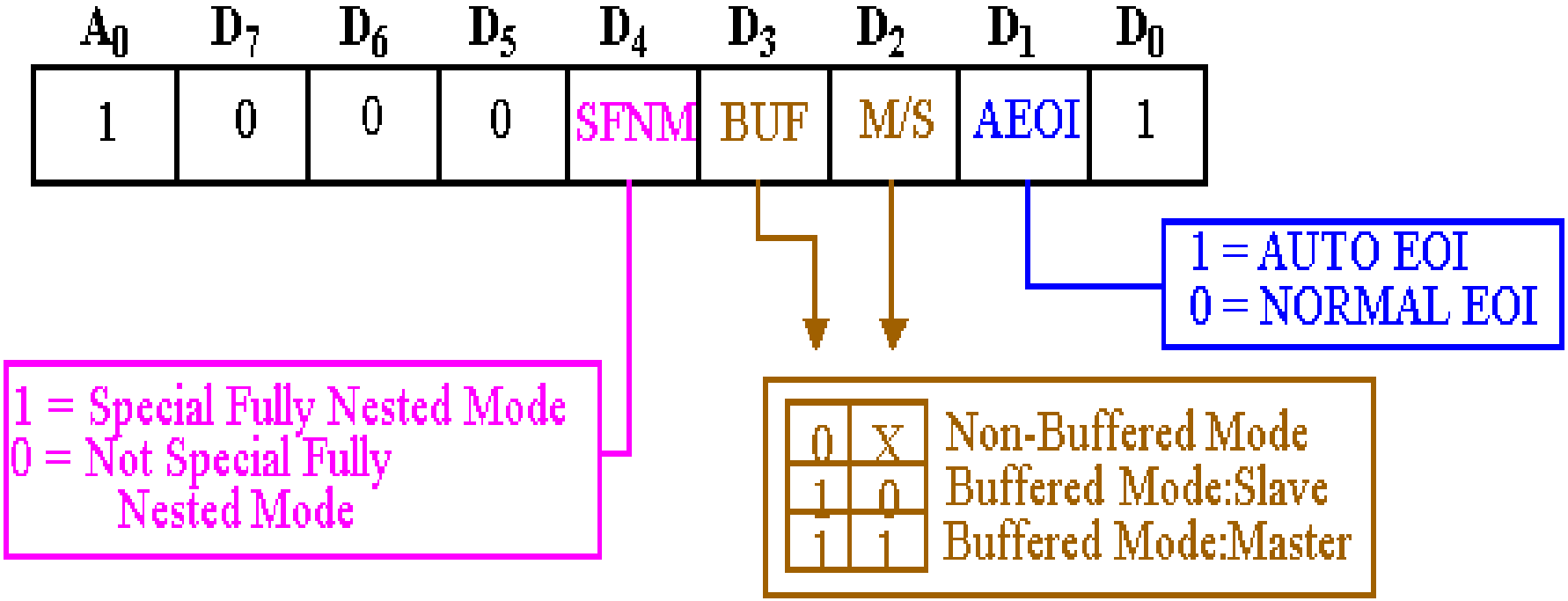
- T_7 – T3 are A3 – A0 of interrupt address
- A_{10} – A_9, A_8 – Selected according to interrupt request level. They are not the address lines of Microprocessor
- A0 =1 selects ICW_2

ICW3:



- Is used only when ICW1 indicates that the system is operated in cascade mode.
- This ICW indicates where the slave is connected to the master.
- For example, if we connected a slave to IR2, then to program ICW3 for this connection, in both master and slave, we place a 04H in ICW3.
- Suppose we have two slaves connected to a master using IR0 and IR1. The master is programmed with an ICW3 of 03H; one slave is programmed with an ICW3 of 01H and the other with an ICW3 of 02H.

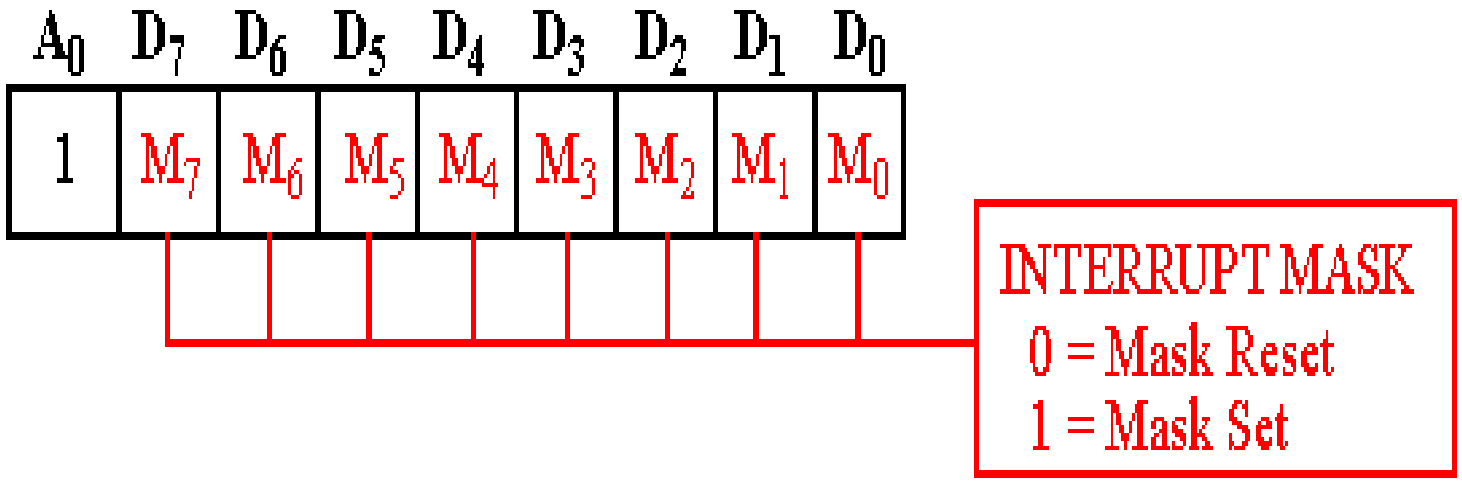
ICW4:



- Is programmed for use with the 8088/8086. This ICW is not programmed in a system that functions with the 8085 microprocessors.
- The rightmost bit must be logic 1 to select operation with the 8086 microprocessor, and the remaining bits are programmed as follows:

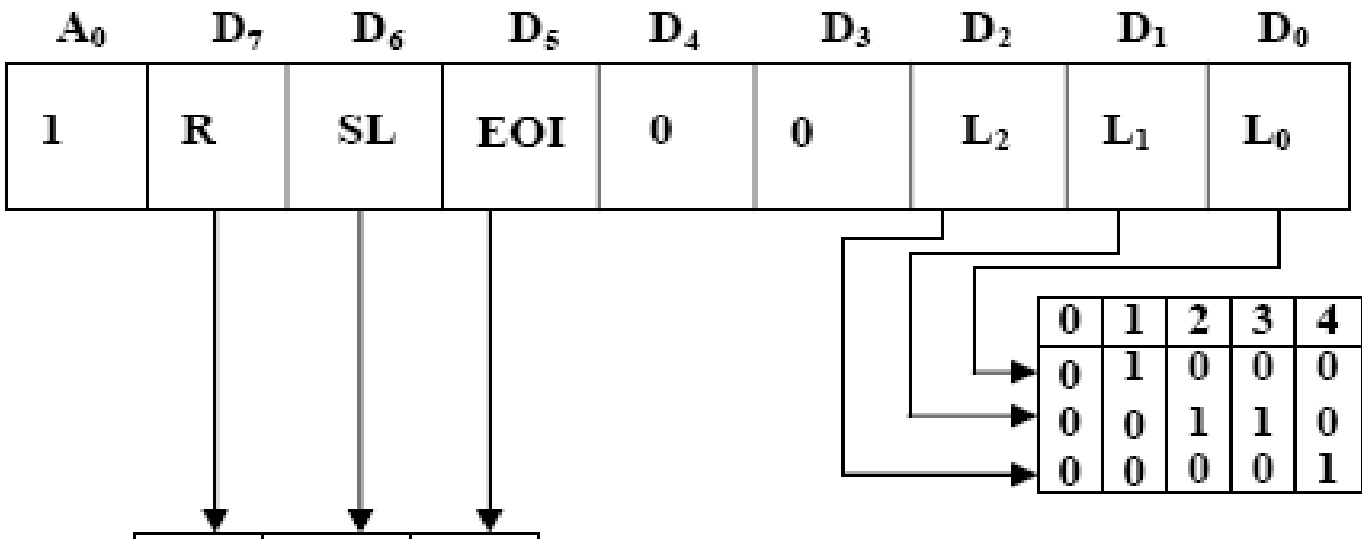
Operation Command Words

OCW1:



- Is used to set and read the interrupt mask register.
- When a mask bit is set, it will turn off (mask) the corresponding interrupt input. The mask register is read when OCW1 is read.
- Because the state of the mask bits is known when the 8259A is first initialized, OCW1 must be programmed after programming the ICW upon initialization.

OCW2:

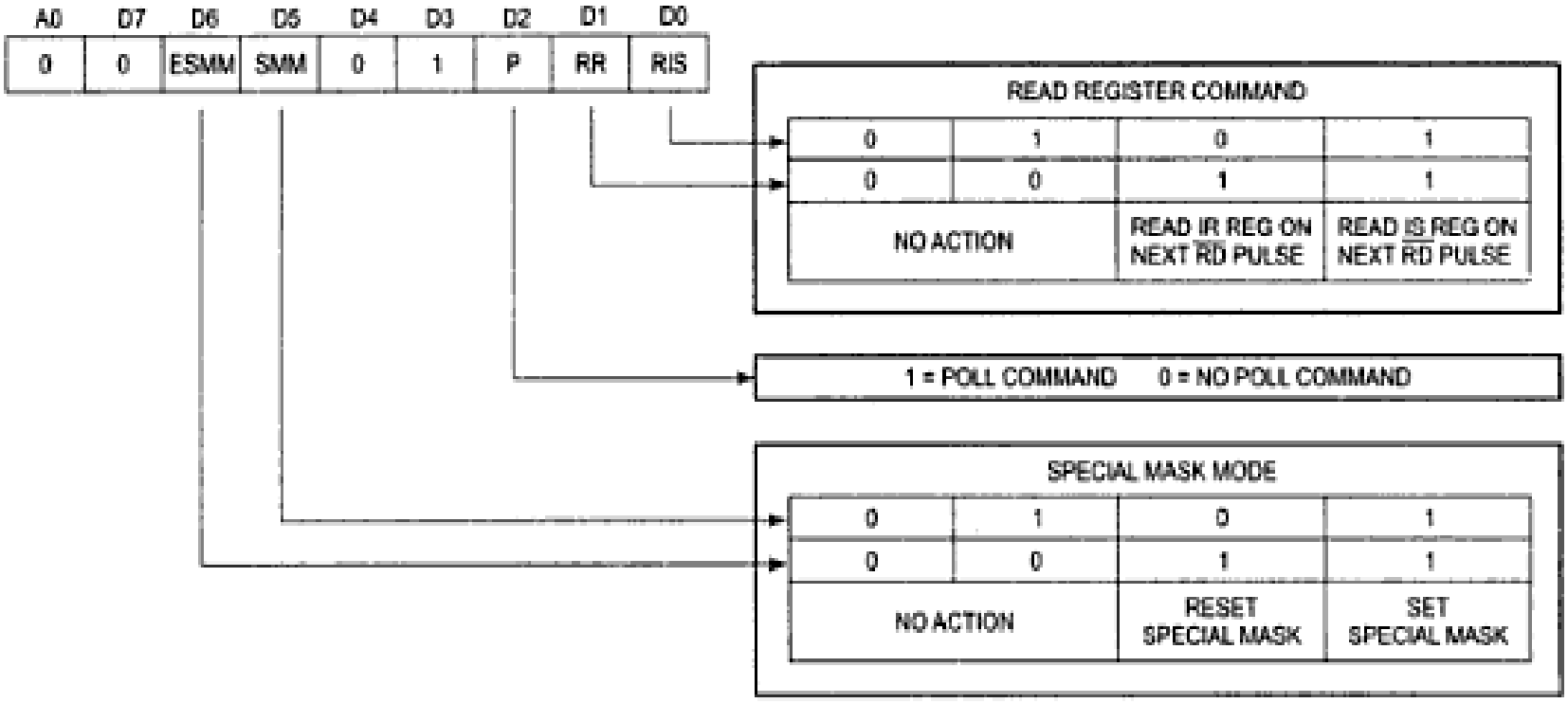


END OF INTERRUPT	0	0	1	NON-SPECIFIC EOI COMMAND
	0	1	1	SPECIFIC EOI COMMAND
AUTOMATIC ROTATION	1	0	1	ROTATE ON NON-SPECIFIC EOI MODE (SET)
	1	0	0	ROTATE IN AUTOMATIC EOI MODE (SET)
	0	0	0	ROTATE IN AUTOMATIC EOI (CLEAR)
SPECIFIC ROTATION	1	1	1	ROTATE ON SPECIFIC EOI COMMAND
	1	1	0	SET PRIORITY COMMAND*
	0	1	0	NO OPERATION

* - In this Mode $L_0 - L_2$ are used

- Is programmed only when the AEOI mod is not selected for the 8259A.
- In this case, this OCW selects how the 8259A responds to an interrupt.
- The modes are listed as follows in next slide:

OCW3:



- Selects the register to be read, the operation of the special mask register, and the poll command.
- If polling is selected, the P-bit must be set and then output to the 8259A. The next read operation would read the poll word. The rightmost three bits of the poll word indicate the active interrupt request with the highest priority.
- The leftmost bit indicates whether there is an interrupt, and must be checked to determine whether the rightmost three bits contain valid information.