SNS COLLEGE OF TECHNOLOGY
(An Autonomous Institution)
COIMBATORE-35
Accredited by NBA-AICTE and Accredited by NAAC – UGC with A+ Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

19EET204 / DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

II YEAR / IV SEMESTER

UNIT-II: DESIGN OF COMBINATIONAL AND SEQUENTIAL CIRCUITS

LATCH & FLIP FLOPS - SR

TOPIC OUTLINE

Memory devices

Latch

SR Flip Flop

D Flip Flop

IC Devices

- Recap

MEMORY DEVICES

Latches :

- A latch is a memory element whose excitation signals control the state of the device.
- A latch has two stages set and reset. Set stage sets the output to 1. Reset stage set the output to 0.
- It is **Asynchronous Sequential Element**

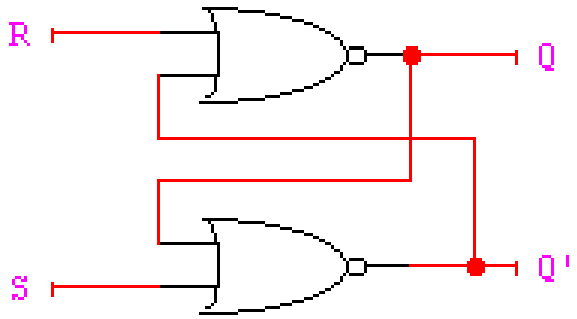
Flip-flops :

- A flip-flop is a memory device that has **clock signals** control the state of the device.
- It is **Synchronous Sequential Element**

LATCH

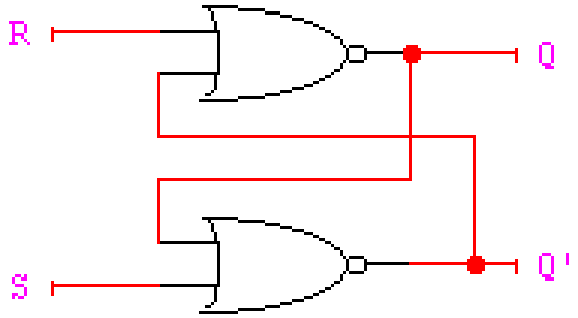
RS Latch

- The RS latch is the basic memory element consists of two cross-coupled NOR gates.
- It has two input signals, S set signal and R reset signal.
- It also has two outputs Q and Q'; and two states, a set state when Q = 1 and a reset state when Q = 0 (Q' = 1)



RS latch – Circuit, Truth table with comments

S	*R*	*Q*	*Q'*
0	0	1	0
0	1	0	1
1	0	1	0
1	1	?	?



S	*R*	Comments
0	0	hold (No change)
0	1	0 reset
1	0	1 set
1	1	unstable (Forbidden)

RS Latch -State table , Ch. Equation

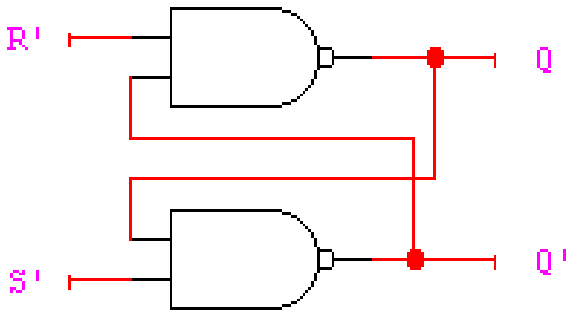
S	*R*	*Q*(*n*)	*Q*(*n*+1)	
0	0	0	0	Hold
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	Set
1	0	1	1	
1	1	0	?	Forbidden
1	1	1	?	

Characteristics Equation:

$Q(t+1) = S(t) + R'(t)Q(t)$

$\boldsymbol{Q^+ = S + R'Q}$

RS latch – Truth table with NAND gates

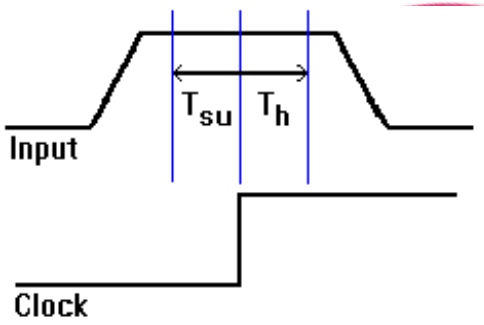


S	*R*	*Q*
0	0	No change
0	1	0 reset
1	0	1 set
1	1	Forbidden

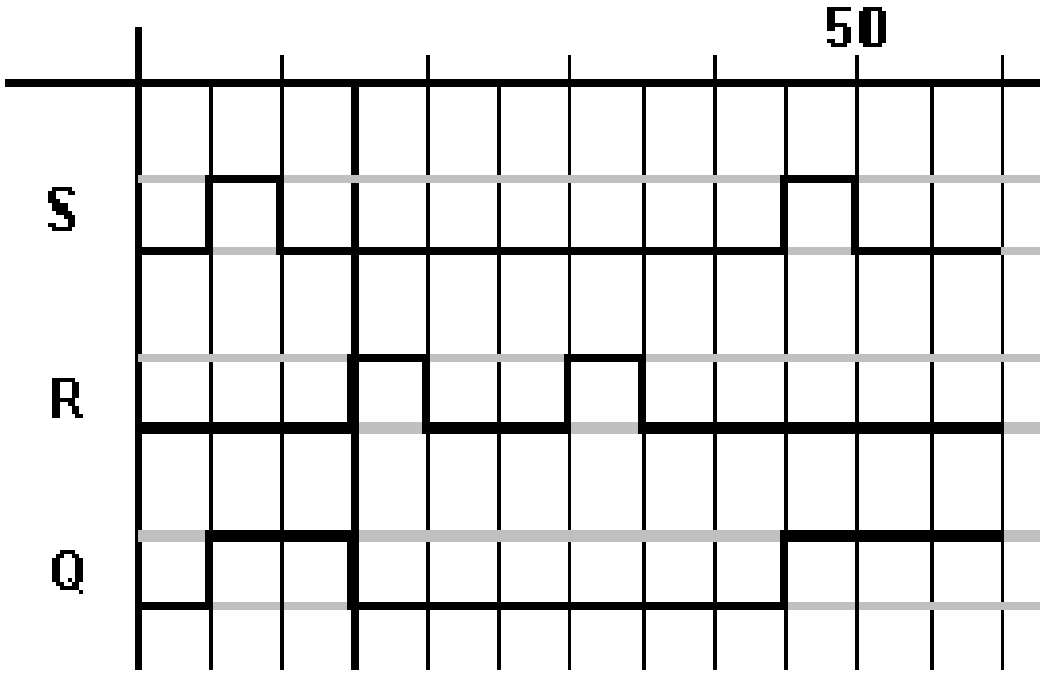
State, Clock, Setup Time, Hold Time

The Clocking event can be either from low to high or from high to low. The input signal around clocking event must remain unchanged in order to have a correct effect on the outcome of the new state.

- T_{su}: the minimum time interval preceding the clocking event during the input signal must remain unchanged
- T_h: the minimum time interval after edge of the clocking event during the input signal must remain unchanged



Timing Diagram of RS-Latch



LATCH / FLIP-FLOP DEVICES

Device	# of Elements	Description
74LS73A	2	Negative-edge triggered JK flip-flop with clear
7474	2	Positive-edge triggered D flip-flop with preset and clear
74LS75	4	D Latch with enable
7476	2	Pulse-edge triggered JK flip-flop with preset and clear
74111	2	Master-slave JK flip-flop with preset, clear, and data lock out
74116	2	4-bit hazard-free D latch with clear and dual enable
74175	4	Positive-edge triggered D flip-flop with clear
74273	8	Positive-edge triggered D flip-flop with clear
74276	4	Negative-edge triggered JK flip-flop with preset and clear
74279	4	SR latch with active-low inputs

SUMMARIZE

…THANK YOU