SNS COLLEGE OF TECHNOLOGY

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB211 – MICROCONTROLLER PROGRAMMING & INTERFACING

II YEAR IV SEM

UNIT II – PIC TIMER, SERIAL PORT AND INTERRUPT

TOPIC 2 – PIC Time Delay and Instruction Pipeline

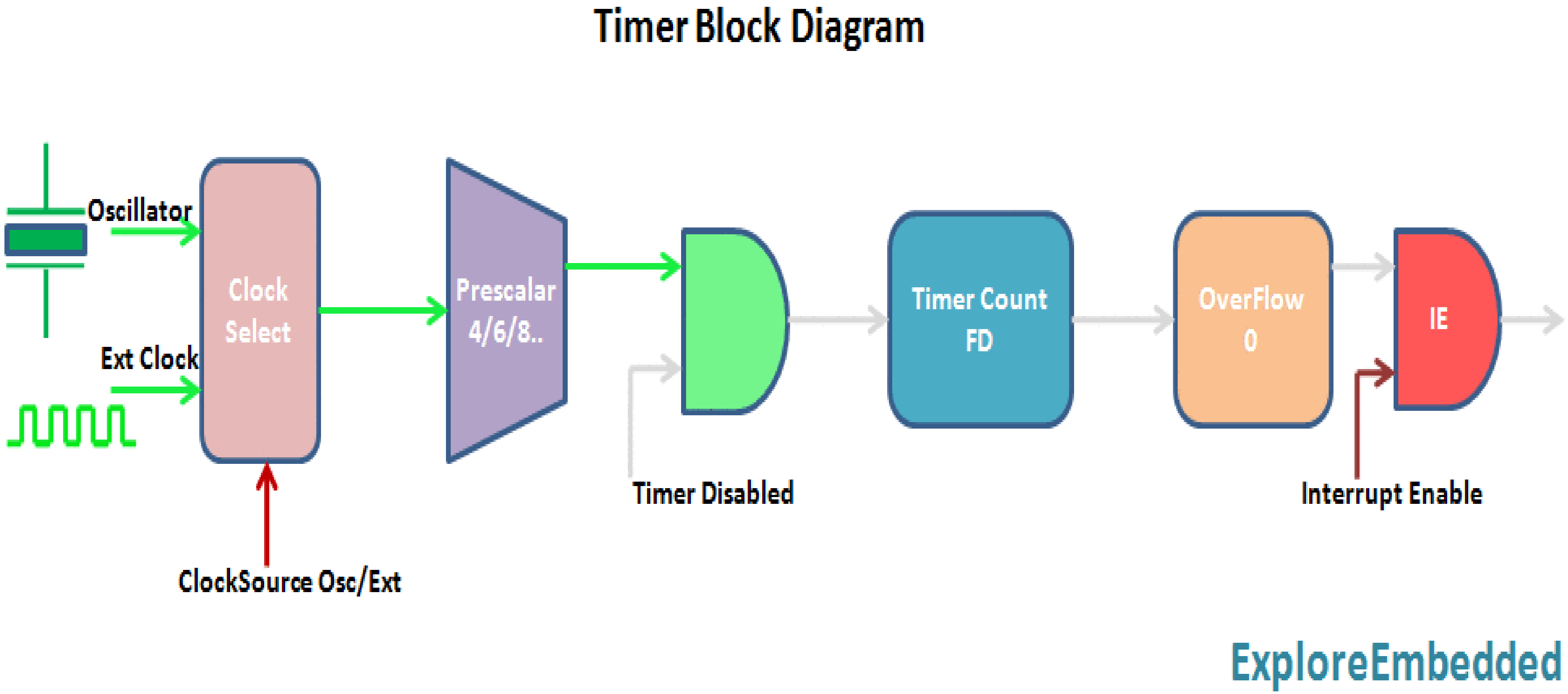
Time Delay

- By utilizing the ability to keep track of time, we can create time delays.
- There are just 2 factors that control the length of a time delay
  1. The number the timer counts to
  2. The rate at which it counts

TIMER

- Timer is nothing but a simple binary counter that can be configured to count clock pulses(Internal/External).
- Once it reaches the Max value, it will roll back to zero setting up an Overflow flag and generates the interrupt if enabled.

Time Delay


Timer Block Diagram
Oscillator
Ext Clock
Clock Select
ClockSource Osc/Ext
Prescalar 4/6/8..
Timer Disabled
Timer Count FD
OverFlow 0
IE
Interrupt Enable
ExploreEmbedded

Time Delay

- The PIC18F4525 microcontroller has 4 timers: timer0, timer1, timer2, and timer3
- A single timer cycle in the PIC18F family is given by (Fosc/4)
- since a single timer cycle uses 4 instruction cycles.
- Thus the time delay used for a single timer cycle is **(4/Fosc)**.

Time Delay

- The PIC microcontroller uses a crystal oscillator or a RC circuit to generate the clock signal needed to control its operation
- The instruction execution time is measured by using the instruction cycle clock
- One instruction cycle is equal to four times the crystal oscillator clock period
- Select an appropriate instruction that will take a multiple of 10 or 20 multiple cycles to execute
- A desirable time delay is created by repeating the chosen instruction sequence for certain number of lines
- The nop

  1. An instruction that does nothing
  2. But its not completely useless
  3. Its perfect for creating time delays
  4. Executing nop takes 1 instruction cycle

PIC Instruction Pipeline

- Instruction pipelining is a technique used in the design of modern microprocessors, microcontrollers and CPUs to increase their instruction throughput (the number of instructions that can be executed in a unit of time)

- The CPU consists internally of logic and memory (flip flops)

PIC Instruction Pipeline

- The control unit in all Central Processing Units (CPUs) follows the same basic instruction processing sequence:

  fetch the instruction

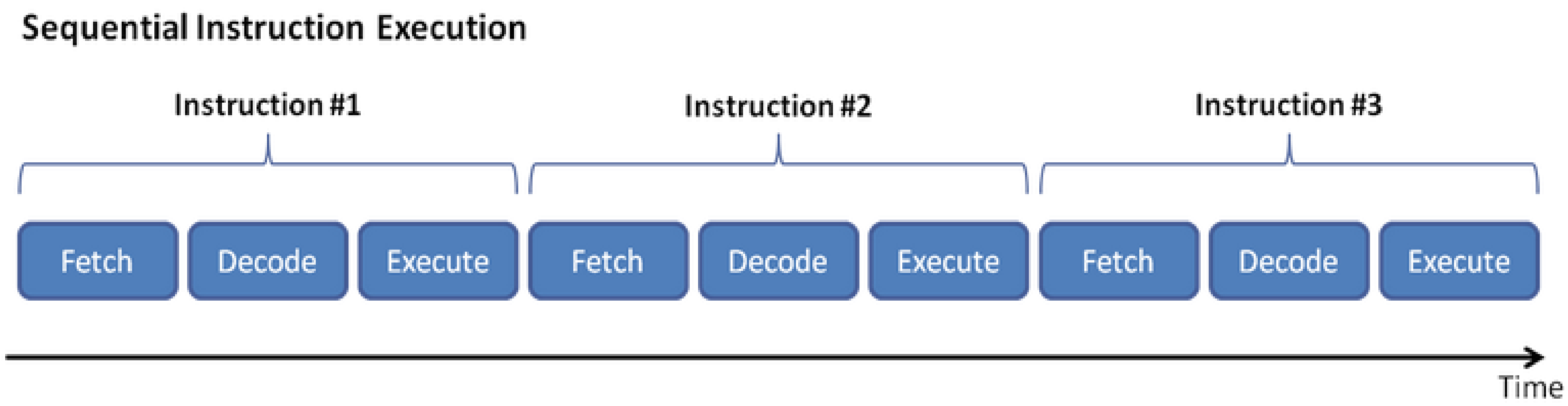
  decode the instruction

  execute the instruction

- Modern, high-performance CPUs (like MIPS®) use a technique called **Pipelining**

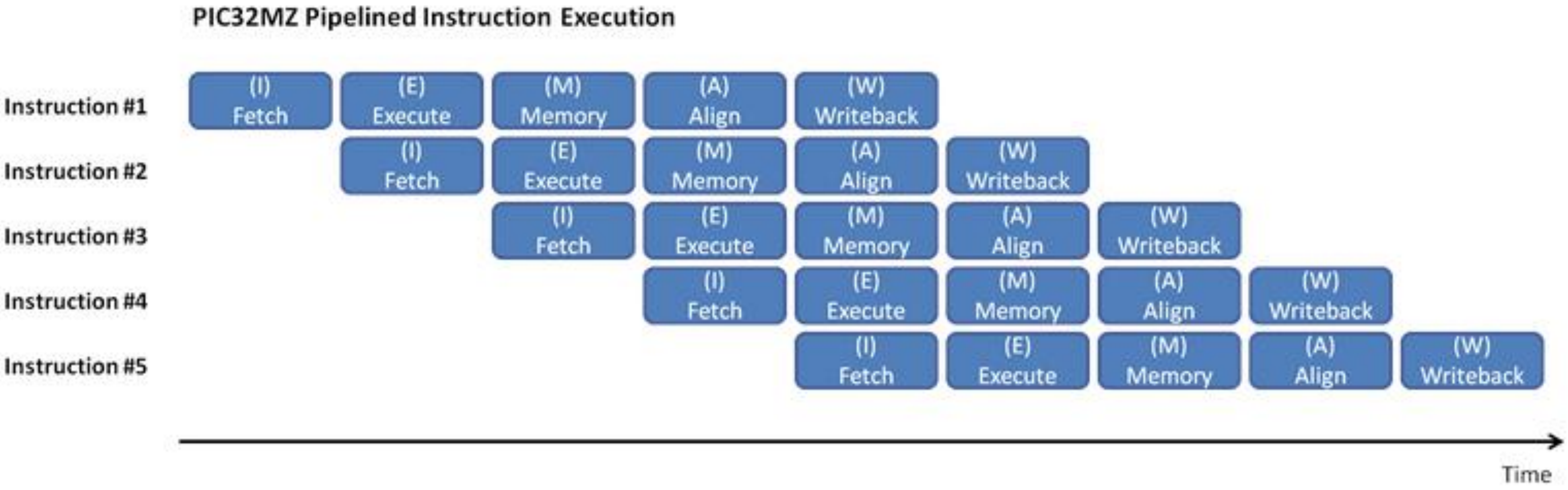
PIC Instruction Pipeline

- phases of instruction processing are executed in independent overlapping stages



- N-stage pipelines therefore have n-instructions at different stages of execution moving through the pipeline, similar to an automotive assembly line.

General Instruction Pipeline

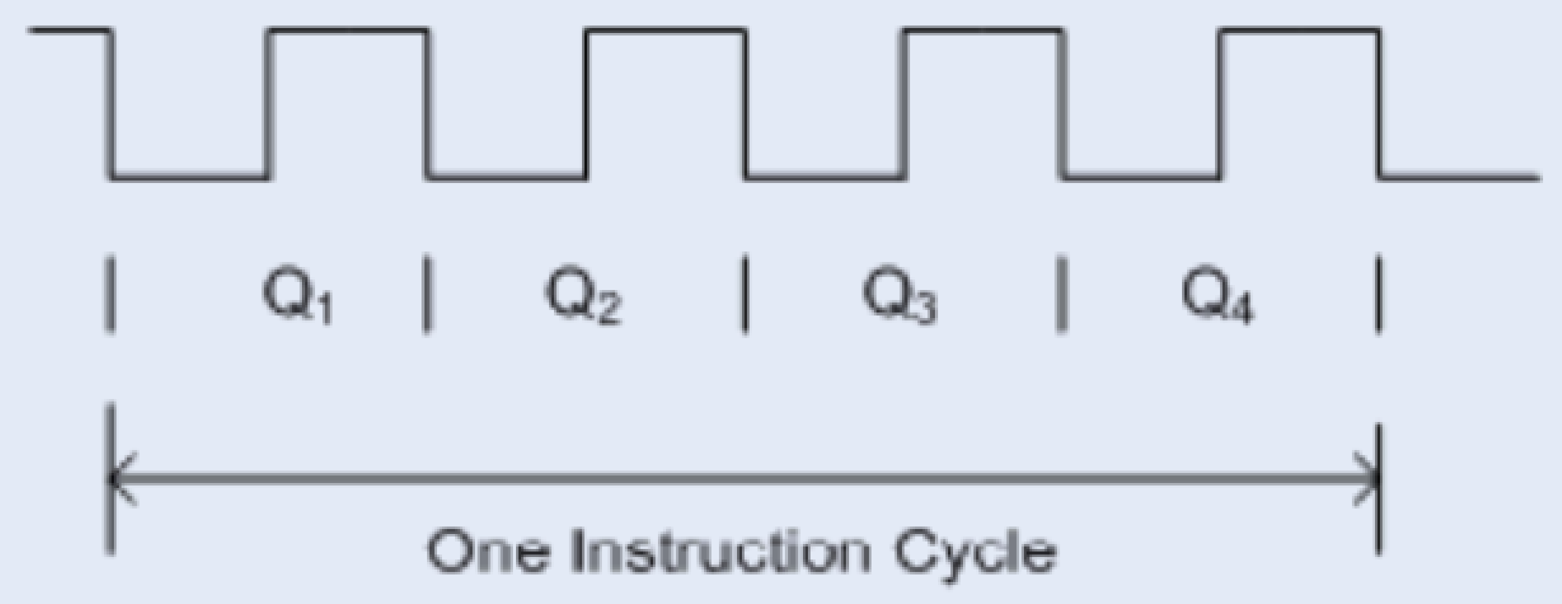


PIC32MZ Pipelined Instruction Execution

Instruction #1	(I) Fetch	(E) Execute	(M) Memory	(A) Align	(W) Writeback				
Instruction #2		(I) Fetch	(E) Execute	(M) Memory	(A) Align	(W) Writeback			
Instruction #3			(I) Fetch	(E) Execute	(M) Memory	(A) Align	(W) Writeback		
Instruction #4				(I) Fetch	(E) Execute	(M) Memory	(A) Align	(W) Writeback	
Instruction #5					(I) Fetch	(E) Execute	(M) Memory	(A) Align	(W) Writeback

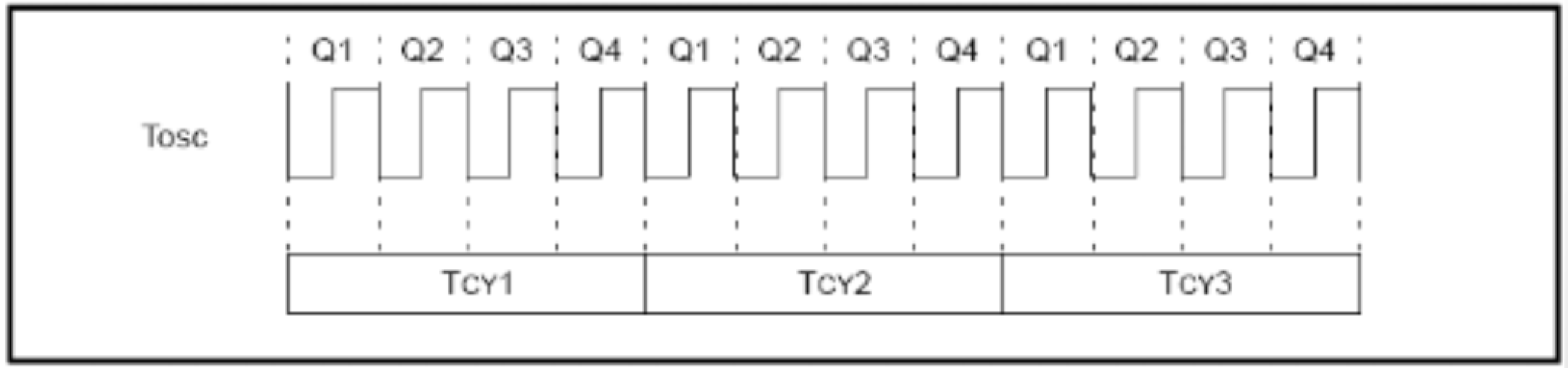
PIC Clock & Instruction Cycle

- Clock from the oscillator enters a microcontroller via OSC1 pin where internal circuit of a microcontroller divides the clock into four even clocks Q1, Q2, Q3 and Q4 which do not overlap.
- These four clocks make up one **instruction cycle** (also called machine cycle) during which one instruction is executed.



PIC Clock & Instruction Cycle

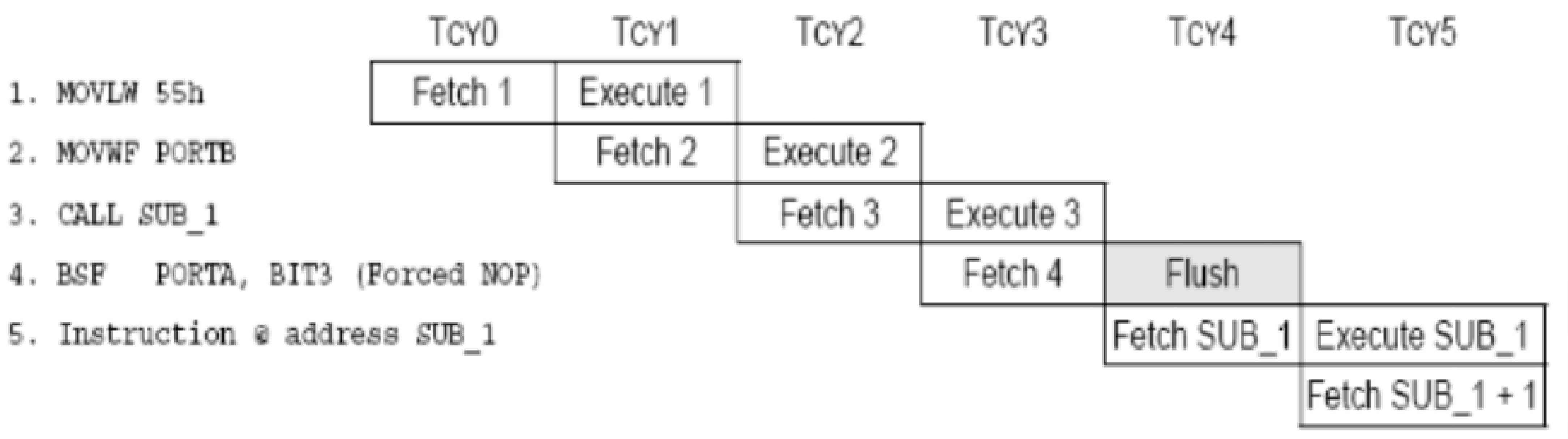
- Execution of instruction starts by calling an instruction that is next in string.
- Instruction is called from program memory on every Q1 and is written in Instruction Register (IR) on Q4.
- Decoding and execution of instruction are done between the next Q1 and Q4 cycles. The following diagram shows the relationship between instruction cycle and clock of the oscillator (OSC1) as well as that of internal clocks Q1 – Q4.
- Program Counter (PC) holds information about the address of the next instruction.



Pipelining in PIC16F877A

- There are 35 single word instructions. A two-stage pipeline overlaps fetch and execution of instructions. As a result, all instructions execute in a single cycle except for program branches. These take two cycles since the fetch instruction is “flushed” from the pipeline while the new instruction is being fetched and then executed.
- A typical picture of the pipeline is shown in Figure 3.

Figure3: Instruction Pipeline Flow



	TCY0	TCY1	TCY2	TCY3	TCY4	TCY5
1. MOVLW 55h	Fetch 1	Execute 1				
2. MOVWF PORTB		Fetch 2	Execute 2			
3. CALL SUB_1			Fetch 3	Execute 3		
4. BSF PORTA, BIT3 (Forced NOP)				Fetch 4	Flush	
5. Instruction @ address SUB_1					Fetch SUB_1	Execute SUB_1
						Fetch SUB_1 + 1

References

https://www.embedded.com/the-evolution-of-embedded-devices-addressing-complex-design-challenges/

http://iamtechnical.com/org-origin-end-list-include-config-radix-directives

https://www.electronicspecifier.com/products/design-automation/embedded-systems-the-evolution-of-embedded-system-design

Mazidi M. A., McKinlay R. D., Causey D. “PIC Microcontroller And Embedded Systems” Pearson Education International, 2008(Unit I,II,III, IV & V)