SNS COLLEGE OF TECHNOLOGY

(An Autonomous Institution)
COIMBATORE - 35

DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING (UG & PG)

QUESTION BANK WITH ANSWER

Subject Code & Name: 19ITT202 Computer Architecture and Organization

Staff Name: Jacquelin Anushya.P AP/CSE

UNIT – IV

I. 2 mark

1. Define Memory Access Time?
It is the time taken by the memory to supply the contents of a location, from the time, it receives "READ".

2. Define memory cycle time.
It is defined as the minimum time delay required between the initaiation of two successive memory operations.

3. What is RAM?
This storage location can be accessed in any order and access time is independent of the location being accessed

4. Explain virtual memory.
The data is to be stored in physical memory locations that have addresses different from those specified by the program. The memory control circuitry trlates the address specified by the program into an address that can be used to access the physical memory.

5. List the various semiconductors RAMs?

- Static RAM.
- Dynamic RAM

6. What do you mean by static memories?
Memories that consist of circuits capable of retaining their state as long as power is applied are known as static memories.

7. Define DRAM's.
Static Rams are fast but their cost is high so we use dynamic RAMs which do not

retain their state indefinitely but here the information are stored in the form of charge on a capacitor

8. Define DDR SDRAM.

The double data rate SDRAMs are the faster version of SDRAM. It trfers data on both edges of the clock.

9. What is ROM?

ROM is by definition Non Volatile Preprogrammed with information permanently encoded in the chip.

10. What is the mapping procedures adopted in the organization of a Cache Memory?

i) Associative mapping.

ii) Direct mapping.

iii) Set-associative mapping

11. Define Hit and Miss?

The performance of cache memory is frequently measured in terms of a quantity called hit ratio. When the CPU refers to memory and finds the word in cache, it is said to produce a hit. If the word is not found in cache, then it is in main memory and it counts as a miss.

16. Write the formula for the average access time experienced by the processor in a system with two levels of caches.

The formula for the average access time experienced by the processor in a system with two levels of caches is

t_{ave}= h1C1+(1-h1)h2C2+(1-h1)(1-h2)M

h1= hit rate in the L1 cache.

h2= hit rate in the L2 cache.

C1=time to access information in the L1 cache.

C2= time to access information in the L1 cache.

M= time to access information in the main memory.

17. What are the enhancements used in the memory management?

1) Write Buffer

2) Pre fetching

3) Look- up Cache.

18. What do you mean by memory management unit?

The memory management unit is a hardware unit which trlates virtual addresses into physical addresses in the virtual memory techniques.

19. Explain main (primary) memory.

This memory stores programs and data that are active in use. Storage locations in main memory are addressed directly by the CPU's load and store instructions.

20. What do you mean by seek time?

It is the time required to move the read/write head in the proper track.

21. What isRAID?

High performance devices tend to be expensive. So we can achieve very high performance at a reasonable cost by using a number of low-cost devices oerating in parallel. This is called RAID(Redundant array of Inexpensive Disks).

22. Define data stripping?

A single large file is stored in several separate disk units by breaking the file up into a number of smaller pieces and storing these pieces on different disks. This is called data stripping.

23. How the data is organized in the disk?

Each surface is divided into concentric tracks and each track is divided into sectors. The set of corresponding tracks on all surfaces of a stack of disks forms a logical cylinder. The data are accessed by using read/write head.

24. Define latency time.

This is the amount of time that elapses after the head is positioned over the correct track until the starting position of the addressed sector passes under the read/write head.