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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB211 – MICROCONTROLLER PROGRAMMING & INTERFACING

II YEAR IV SEM

UNIT I – PIC MICROCONTROLLER : HISTORY , FEATURES & ARCHITECTURE

TOPIC 5– Use of Instructions with the Default Access Bank

File Register & Access Bank in PIC

- There is a limitation in the instructions that the PIC uses to address iRAM locations (basically all of the instructions which have an “f” in them).
- Byte-oriented instructions which address the registers are in the format of –

Code (text):

Code (text):

OPCODE						DEST	A6	A5	A4	A3	A2	A1	A0
x	x	x	x	x	x	0/1	f	f	f	f	f	f	f

File Register & Access Bank in PIC

- Byte-oriented instructions which address the registers are in the format of –

Code (text):

Code (text):

```
|     OPCODE     |Bit Number |A6 |A5 |A4 |A3 |A2 |A1 |A0 |
| x | x | x | x | b | b | b | f | f | f | f | f | f | f |
```

Use of Instructions in Access Bank of PIC

- The opcode is the instruction itself.
- In the first table, DST is the destination bit that tells the PIC whether to store the result in W (0) or in the file register (1) who's address is in bits AD0-AD6.
- In the second table, the 4 MSBs are the instruction, the 3 "BIT" bits are the bit that the instruction will be executed on (0-7), while AD0-AD6 are the address in the file where the bit to be manipulated resides.

Use of Instructions in Access Bank of PIC

- Basically, instructions which directly address the iRAM register locations can only provide 7 of the address bits.
- Since 7 bits can only count to 0x7F (decimal 127), this limits the instruction itself to only access 128 RAM locations on its own…hence the limitation.

So how can we overcome the limitation so that we can address the entire iRAM space?

- With the addition of two more bits of course, but where would they come from?

the STATUS register!

- It is referred to as the “bank select” bits but this is just a convention that Microchip decided to use for its “register banking” concept.
- Bits RP1 and RP0 (Register Page 1 and Register Page 0 respectively) serve as the upper 2 address bits for instructions which directly address the iRAM locations.

Use of Instructions in Access Bank of PIC

- For instance we wanted to move a value in W to register TRISA, which has iRAM address 0x85 (b'010000101).
- The instruction could not supply the leading "01" in the address, so these two bits must come from register bits RP0 and RP1.
- So prior to writing the contents of W to register TRISA, we must first execute these two instructions –

bsf STATUS,RP0

bcf STATUS,RP1

Use of Instructions in Access Bank of PIC

- With a more conventional processor like the Intel 8051, a mov instruction is 8 bits long, followed by 1 or 2 more bytes that provide the address(es) that the mov instruction is being executed on.
- With an instruction set of this nature, no iRAM ‘banking’ is required.
- If we were to use the FSR to indirectly address register TRISA, we could simply load the FSR with the value of 0x85, load W with the immediate value to write to TRISA, then load the value in W into the INDF register without having to bank select

Use of Instructions in Access Bank of PIC

- This is because register FSR is an 8 bit register and can supply 8 of the 9 address bits on its own.
- However, we must ensure that bit IRP in the STATUS register is clear prior to doing this otherwise we would end up writing to iRAM register address 0x185 instead of 0x085.

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