The Status Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IRP	RP1	RP0	TO	PD	Z	DC	C

The STATUS register is of most importance to programming the PIC, it contains the arithmetic status of the ALU (Arithmetic Logic Unit), the RESET status and the bank select bit for data memory. As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the TO and PD bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended. For example, `CLRF STATUS` will clear the upper-three bits and set the Z bit. This leaves the STATUS register as 000u u1uu (where u = unchanged).

The first three bits (STATUS<0> to STATUS<2>) are the carry (C), digit carry (DC) and zero (Z) flags of the ALU respectively. The values of these bits change depending on the results of arithmetic or logical operations performed during program execution. Bits 3 and 4 are the power down PD and watchdog timer timeout TO bits respectively and bits 5and6(RP0 and RP1) are the bank selection bits.

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	TO	PD	Z	DC	C
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

R = Readable bit
W= Writable bit
U = Unimplemented bit, read as '0'
-n= Value at POR reset

The Status Register

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IRP	RP1	RP0	TO	PD	Z	DC	C

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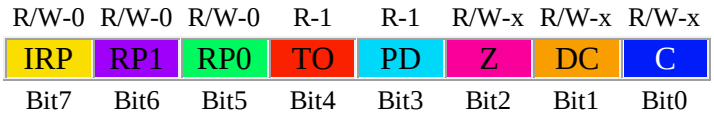

bit 7:
IRP: Register Bank Select bit (used for indirect addressing)
0 = Bank 0, 1 (00h - FFh)
1 = Bank 2, 3 (100h - 1FFh)
The IRP bit is not used by the PIC16F8X. IRP should be maintained clear.

bit 6-5:
RP1:RP0: Register Bank Select bits (used for direct addressing)
00 = Bank 0 (00h - 7Fh)
01 = Bank 1 (80h - FFh)
10 = Bank 2 (100h - 17Fh)
11 = Bank 3 (180h - 1FFh)
Each bank is 128 bytes. Only bit RP0 is used by the PIC16F8X. RP1 should be maintained clear.

bit 4:
TO: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3:
PD: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the `SLEEP` instruction

bit 2:
Z: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero
bit (for `ADDWF` and `ADDLW` instructions) (For borrow the polarity is reversed)

bit 1:

DC: Digit carry/borrow
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result
bit (for ADDWF and ADDLW instructions)

bit 0:
C: Carry/borrow
1 = A carry-out from the most significant bit of the result occurred
0 = No carry-out from the most significant bit of the result occurred
Note: For borrow the second operand the polarity is reversed. A subtraction is executed by adding the two's comp
of. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register