UNIT V

IC MOSFET AMPLIFIERS

IC Biasing

* In Integrated circuit designs biasing circuits use constant - current sources.

* Here, the constant d.c current called reference current is generated at one location & is then replicated at various other locations for biasing the various stages of amplifiers present in the circuit.

* This process is known as current steering. ✳ 2 Mark

Advantages of current steering process ✳ 2 Mark

* The external components such as precision resistors required to generate a predictable & stable reference current, need not be repeated for every amplifier stage.

* The bias currents of the various stages track each other when there is any change due to power-supply voltage (or) temperature.

MOSFET Current Sources

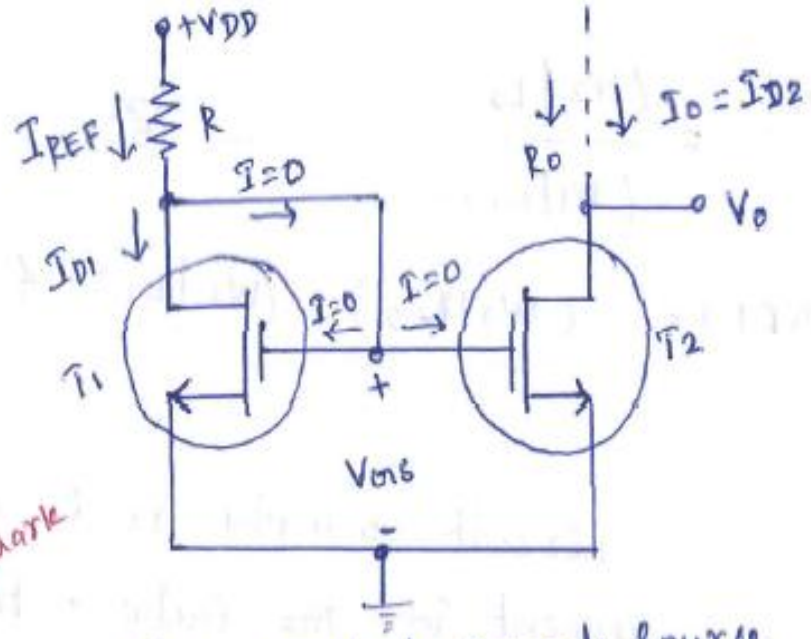


Fig: Constant Current Source Using MOSFET

* The circuit uses 2 MOSFETs T1 & T2.
* The drain & gate of MOSFET T1 is shorted, it's operated in saturation region.
* Neglecting channel length modulation ($\lambda = 0$) The drain

Current of T_1 is given by

$$I_{REF} = I_{D1}$$

$$= \frac{1}{2} K_n' \left(\frac{W_1}{L_1}\right) (V_{GS} - V_{T1})^2 \quad -(1)$$

$$I_{REF} = K_{n1}(V_{GS}-V_{T1})^2 \Rightarrow \frac{I_{REF}}{K_{n1}} = (V_{GS}-V_T)^2$$

$$V_{GS} = V_{T1} + \sqrt{\frac{I_{REF}}{K_{n1}}} \quad -(2)$$

W.K.T

$$I_{REF} = I_{D1} \Rightarrow$$

$$I_{REF} = \frac{V_{DD}-V_{GS}}{R} \quad -(3)$$

* The MOSFET T_2 has the same V_{GS} at T_1 : Thus if we assume that it's operating in saturation we have

$$I_O = I_{D2} = \frac{1}{2} K_n' \left(\frac{W_2}{L_2}\right)(V_{GS}-V_{T2})^2 \quad -(4)$$

$$= K_{n2}(V_{GS}-V_{T2})^2$$

* $V_{GS1} = V_{GS2}$ & substituting value of V_{GS} from

eqn ② we have

$$I_O = K_{n2}\left(V_{T1} + \sqrt{\frac{I_{REF}}{K_{n1}}} - V_{T2}\right)^2 .$$

* Here also we can neglect the channel length modulation ($\lambda = 0$).

* Taking the ratio of eqns ① & ④ we get

$$\frac{I_O}{I_{REF}} = \frac{I_{D2}}{I_{D1}} = \frac{(W_2/L_2)}{(W_1/L_1)} \quad \text{— ⑤}$$

* For identical MOSFETs, $(W_2/L_2) = (W_1/L_1)$ & hence

$I_O = I_{REF}$.

* In such situation the circuit simply replicates (or) mirrors the reference current in the output terminal.

* For the reason, when 2 MOSFETs are identical, the circuit shown in above fig is known as current Mirror circuit.

Effect of V_o on I_o

* T_2 operated in saturation.

$$V_o \geq V_{GS} - V_T \quad \text{---} \quad (6)$$

(or)

$$V_o \geq V_{ov} \quad \text{---} \quad (7)$$

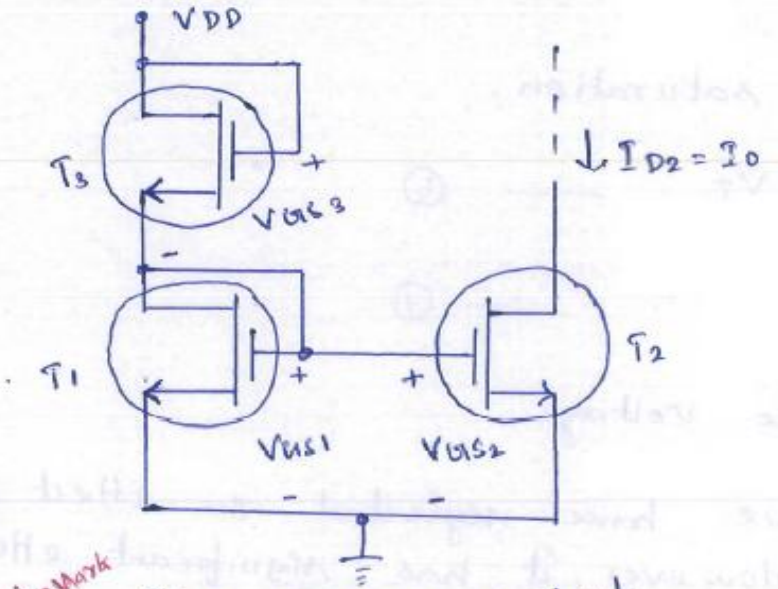
where

V_{ov} - overdrive voltage

2 Mark

* In initial analysis we have neglected the effect of channel length modulation. However, it has significant effect on the operation of the current source circuit.

Replacing R by another MOSFET



X-2 Marks

Fig: MOSFET constant current source

* R is replaced by another MOSFET.
* Here, The MOSFET is configured like a resistor.
* Since T_1 & T_3 are connected in series $I_{D1} = I_{D3}$.
* Neglecting channel length modulation ($\lambda = 0$) we can write

$$K_{n1}(V_{GS1} - V_{T1})^2 = K_{n3}(V_{GS3} - V_{T3})^2 \quad \text{— (1)}$$

* From the circuit we have

$$V_{GS1} + V_{GS3} = V_{DD}$$

* load current I_O with $\lambda = 0$ we can be given by

$$I_O = \frac{K_n'}{2}\left(\frac{W_2}{L_2}\right)(V_{GS2} - V_T)^2 .$$

MOSFET Current Source Circuit - Cascode Current Mirror.

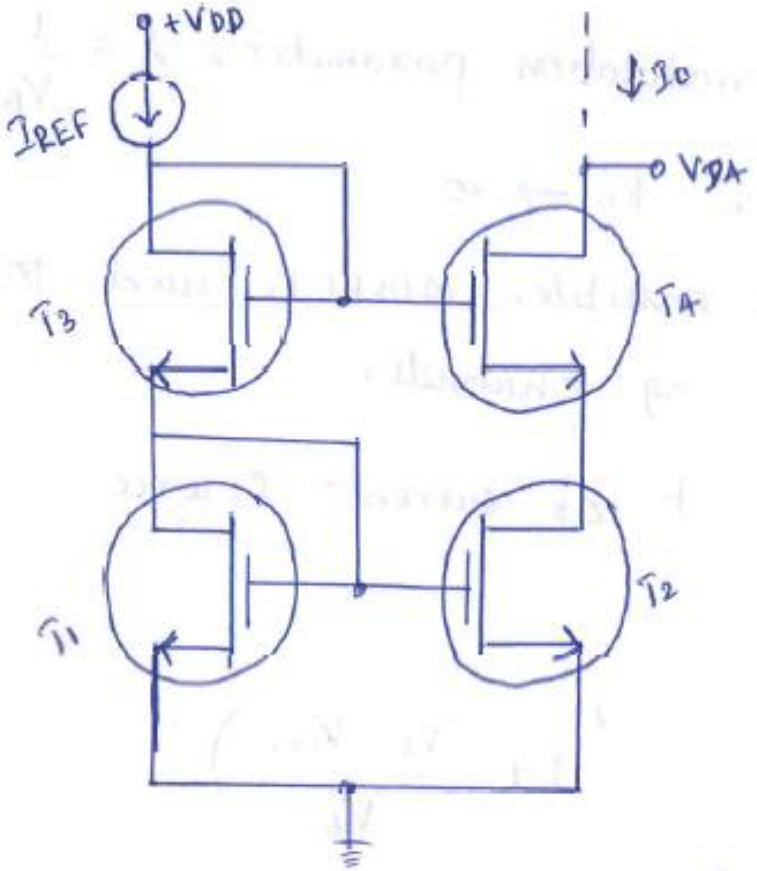
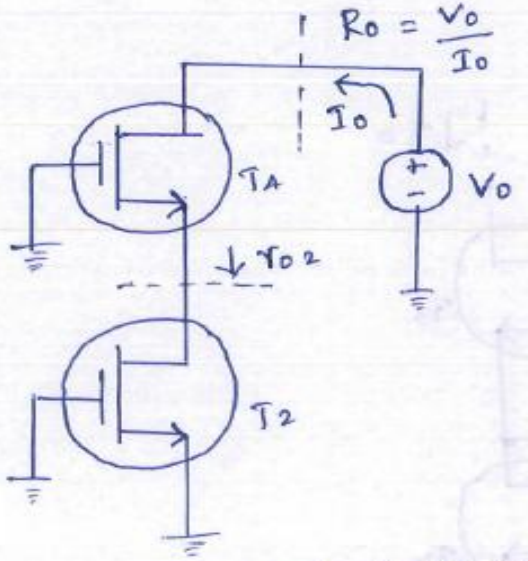


Fig: MOSFET Cascode Current Mirror Circuit

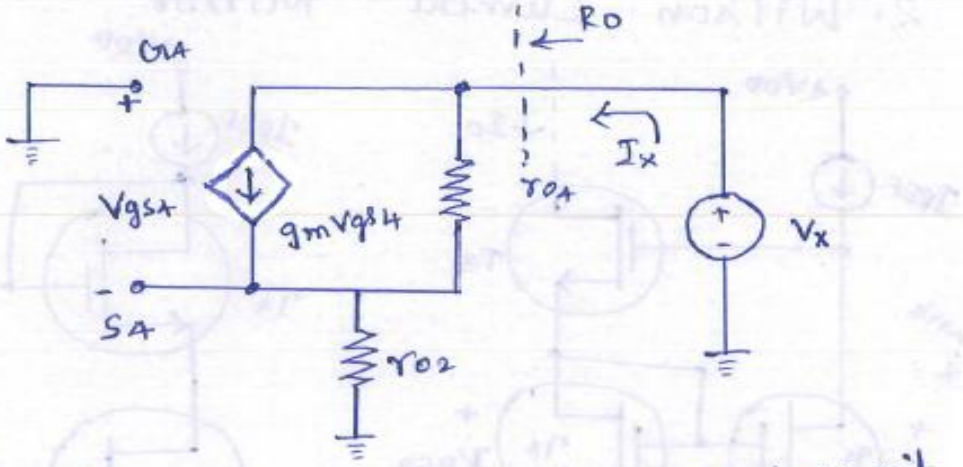
* The Output resistance is a measure of stability of Io with respect to the changes in the Output voltage.

* Here the MOSFETs T3 & T4 are included to provide higher Output resistance.

* This circuit is known as cascode current mirror circuit.



(a) Equivalent Circuit



(b) Small Signal Equivalent Circuit

* The gate voltage for T_1 & T_3 & hence for T_2 & T_4 are constant, They are shown grounded for a.c circuits.
* In the small signal equivalent circuit to obtain R_O.
* Here T_2 is replaced by equivalent resistance r_{O2}.
* Applying KCL to output node we have

$$I_x = g_m V_{gs4} + \frac{V_x - (-V_{gs4})}{r_{O4}} \quad -①$$

$$V_{gs4} = -I_x r_{O2} \quad -②$$

* substitute eqn ② in ①

$$I_o' = -g_m I_x r_{o2} + \frac{V_x - (I_x r_{o2})}{r_{o4}} \quad -③$$

$$\therefore I_x + g_m I_x r_{o2} + \frac{I_x r_{o2}}{r_{o4}} = \frac{V_x}{r_{o4}}$$

$$\therefore R_o = \frac{V_x}{I_x} = r_{o4} + g_m r_{o2} r_{o4} + r_{o2}$$

$$R_o = r_{o4} + r_{o2}(1 + g_m r_{o4}) \quad -④$$

2 Mark

* Since $g_m r_{o2} >> 1$, The Output resistance of the Cascode current mirror is much greater than basic 2 MOSFET current Source.

Amplifiers with Active Load

* When MOSFET itself is used as a load device, it's referred to as active load.

* There are 3 types of load devices

X 2 Mark

1. n-channel enhancement mode device
2. n-channel depletion-mode device
3. p-channel enhancement mode device

1. NMOS Amplifier with Enhancement Load

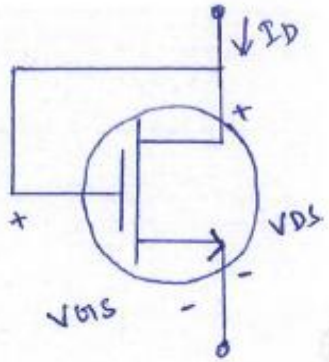


Fig: N-channel enhancement mode MOSFET with gate & drain shorted

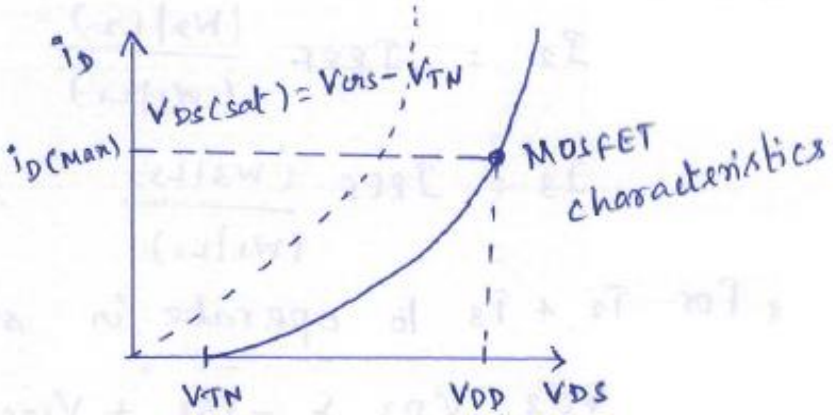


Fig: current - voltage characteristics for n-channel enhancement load device

* In this, the MOSFET act as a non-linear resistor & is called enhancement load device.

* Since MOSFET is in enhancement mode $V_T > 0$.

* For this circuit $V_{DS}(sat) = V_{GS} - V_T$ which means that the MOSFET is always in the saturation region.

* The I-V characteristics is a plot of equation

$$i_D = K_n (V_{GS} - V_T)^2$$

* The enhancement load circuit alone can't be used as an amplifier, however, if it's connected in a circuit with another MOSFET. This circuit can be used as an amplifier (or) as an inverter in a digital circuit.

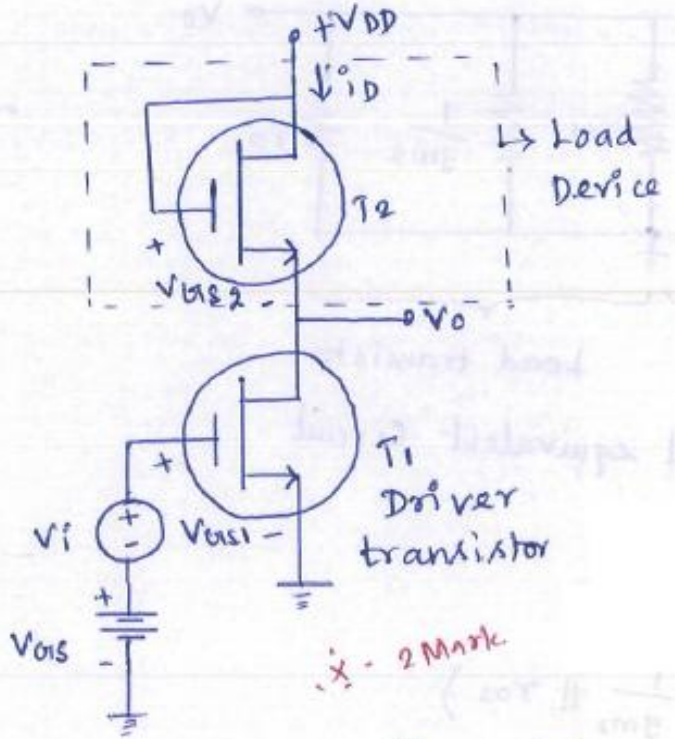


Fig: NMOS amplifier with enhancement load device

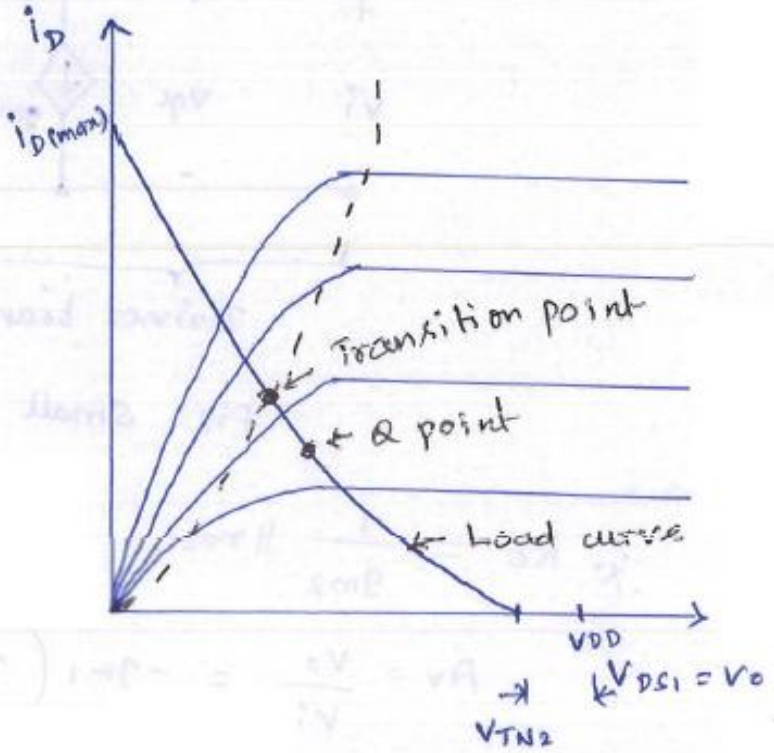
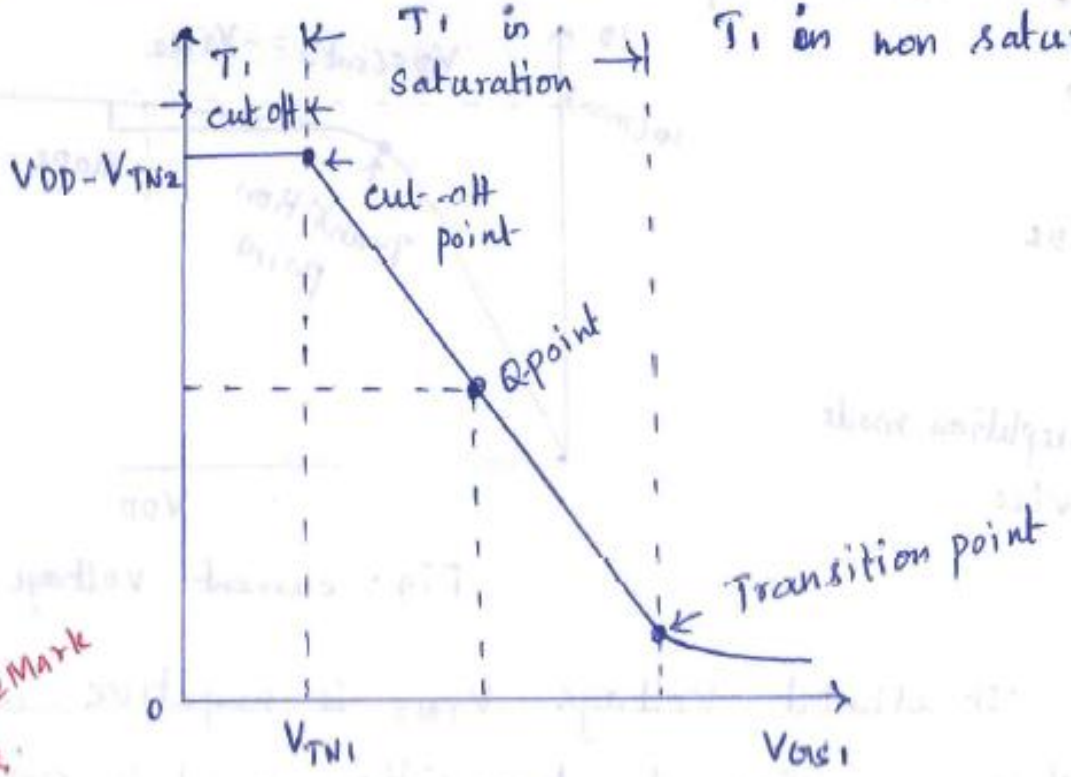


Fig: V-I characteristics

* Here the MOSFET T_2 is used as a load & MOSFET 'T_1' is used as a driver transistor.
* The load device T_2 is always biased in the saturation region.
* The V-I characteristics of the load device is non-linear, the load curve is also non-linear.

* At $V_{DD} - V_{TN2}$, the load curve intersects the voltage axis & the current in the enhancement load goes to zero.



2 Mark

Fig: Voltage Transfer characteristics

* In the characteristics fig: the Q-point should be in the Saturation region to use circuit as an amplifier.

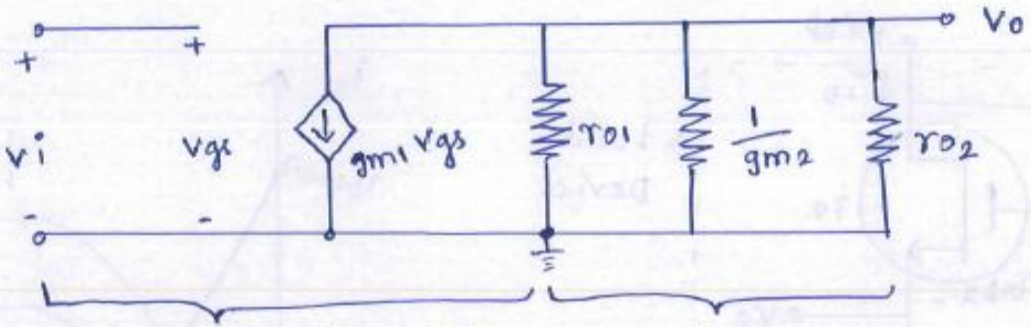


Fig: Small signal equivalent circuit

$$\therefore R_o = \frac{1}{g_{m2}} \parallel r_{o2}$$

$$A_v = \frac{v_o}{v_i} = -g_{m1}\left(r_{o1} \parallel \frac{1}{g_{m2}} \parallel r_{o2} \right)$$

Since $\frac{1}{g_{m2}} << r_{o2}$ & $\frac{1}{g_{m1}} << r_{o1}$, the Av can be approximated as

$$A_v = \frac{-g_{m1}}{g_{m2}} = -\sqrt{\frac{K_{n1}}{K_{n2}}} = -\sqrt{\frac{(W_1/L_1)}{(W_2/L_2)}}$$

2 Marks

⇒ * This is related to the size of the transistor.

2 Marks

* To obtain larger voltage gain we can use depletion-mode MOSFET.

NMOS Amplifier with Depletion Load

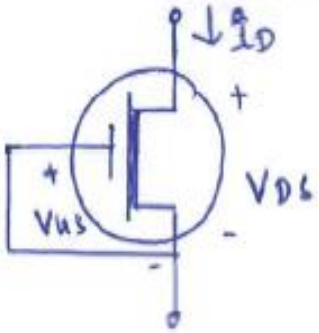


Fig: NMOS depletion mode device

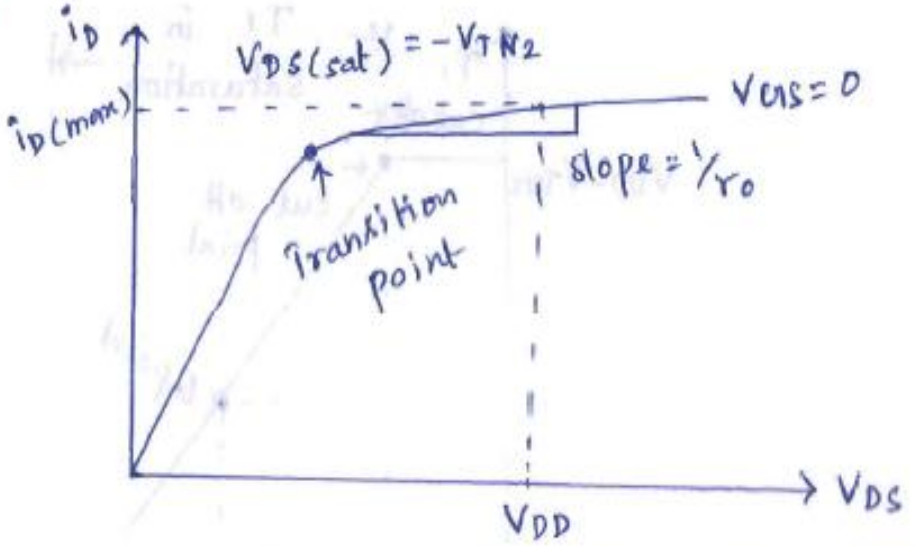


Fig: current - voltage characteristics

* Here, the Threshold voltage V_{TN2} is negative, which means that the value of V_{DS} at transition point is positive.

* Non-zero slope in the saturation region indicates that a finite resistance r_o exists in this region.

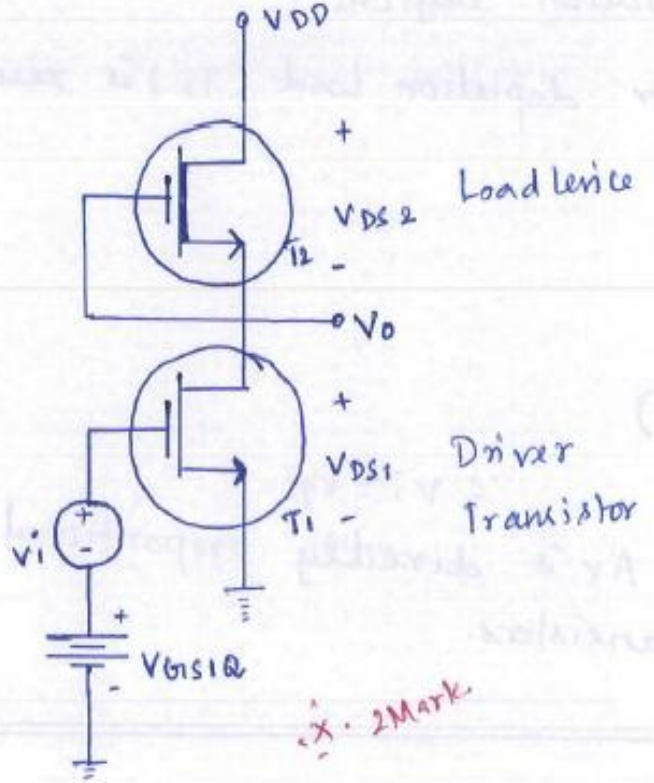


Fig: NMOS amplifier with depletion load device

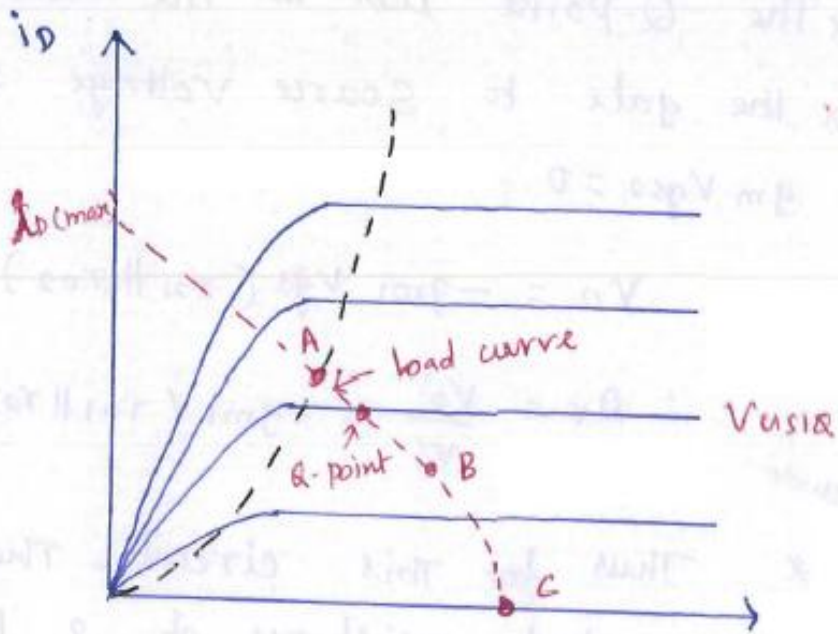


Fig: Driver transistor characteristics

A - Transition point for T_1

B - Transition point for T_2

* Here, T_1 is used as a driver & T_2 is used as a load.

* The I-V characteristics of the loaddevice is non-linear. The load curve is also non-linear.

* points A & B are transition points for T_1 & T_2.
* Q-point is approximately midway between 2 transition points.
* For amplifier operation, both MOSFET should be biased in Saturation region.

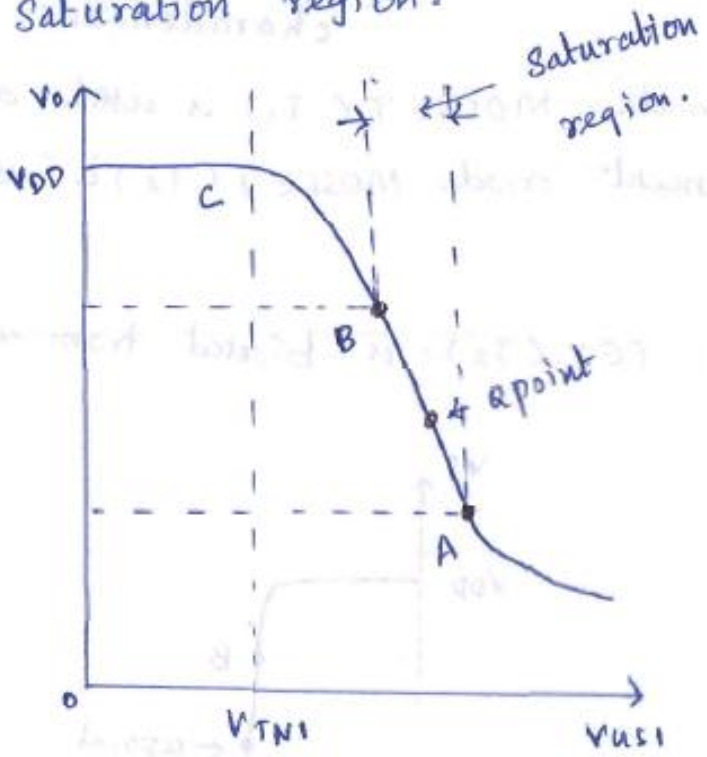


Fig: Voltage Transfer characteristics

~~X~~ 2Mark.

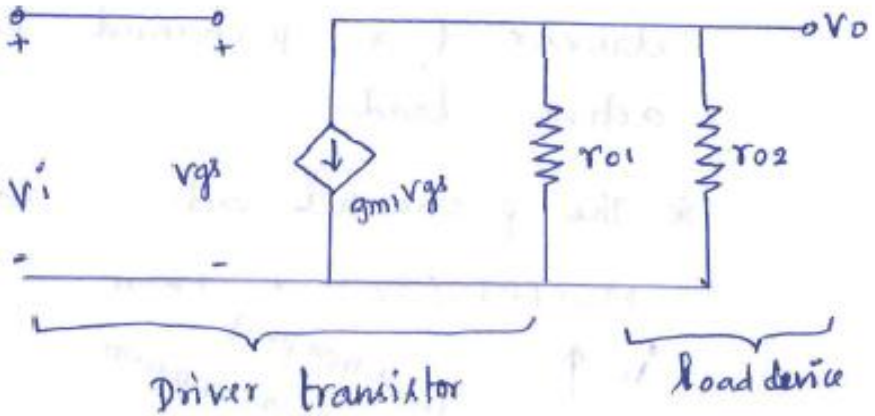


Fig: Small signal equivalent circuit

* The Q-point lies in the saturation region.
* The gate to source voltage for depletion load (T_2) is zero, $g_m V_{gs2} = 0$.

$$V_o = -g_{m1} V_{gs} (r_{o1} \| r_{o2})$$

$$\therefore A_v = \frac{V_o}{V_i} = -g_{m1} (r_{o1} \| r_{o2})$$

$\because V_i = V_{gs}$

* Thus for this circuit, the A_v is directly proportional to the output resistance of 2 transistors.

CMOS Differential Amplifier

* In differential amplifier the Output signal is the amplified version of the difference of 2 inputs of the amplifier.

* In CMOS differential amplifier a current mirror circuit is employed as an active load for the Source-coupled pair.

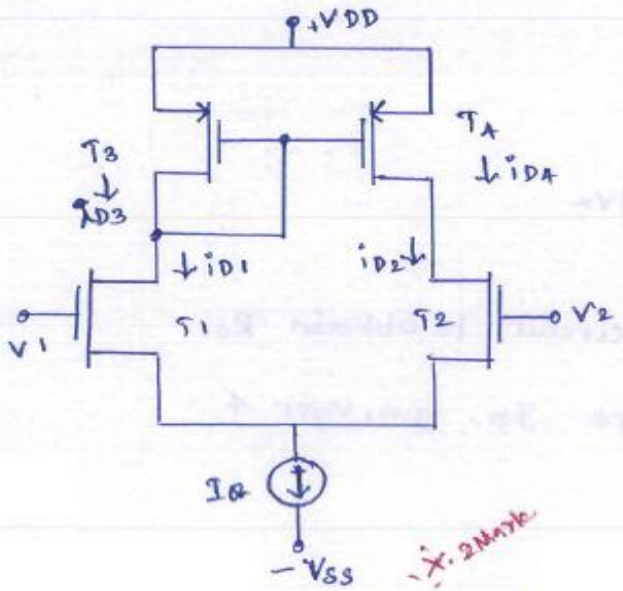


Fig: CMOS Differential amplifier with active load

* Here, Transistor T_1 & T_2 are n-channel devices & forms the differential pair biased with I_Q.

* The load circuit consists of Transistor T_3 & T_4 both p-channel devices.

* Here (T_1, T_2) & (T_3, T_4) are mutually identical with each other thus the tail current I_Q is equally divided between T_1 (T_3) & T_2 (T_4) when common mode voltage $V_1 = V_2 = V_{cm}$ is applied.

$$\therefore I_{D1} = i_{D2} = \frac{I_Q}{2} \quad \text{—— (1)}$$

* The gate currents are zero, $i_{D1} = i_{D3}$ & $i_{D2} = i_{D4}$.

* When small differential mode voltage $V_d = V_1 - V_2$ is applied we have

$$i_{D1} = \frac{I_Q}{2} + i_d \quad \text{—— (2)}$$

$$i_{D2} = \frac{I_Q}{2} - i_d \quad \text{—— (3)}$$

* where i_d is the signal current.

* Since T_1 & T_2 and T_3 & T_4 are in series we have

$$i_{D3} = \frac{I_Q}{2} + i_d = i_{D1} \quad \text{— (4)}$$

$$i_{D4} = \frac{I_Q}{2} - i_d = i_{D2} \quad \text{—— (5)}$$

* For small values of V_d, we have

$$i_d = g_m \frac{V_d}{2} \quad \text{—— (6)}$$

* Let the below fig: The small signal equivalent circuit at the drain node of T_2 & T_4.

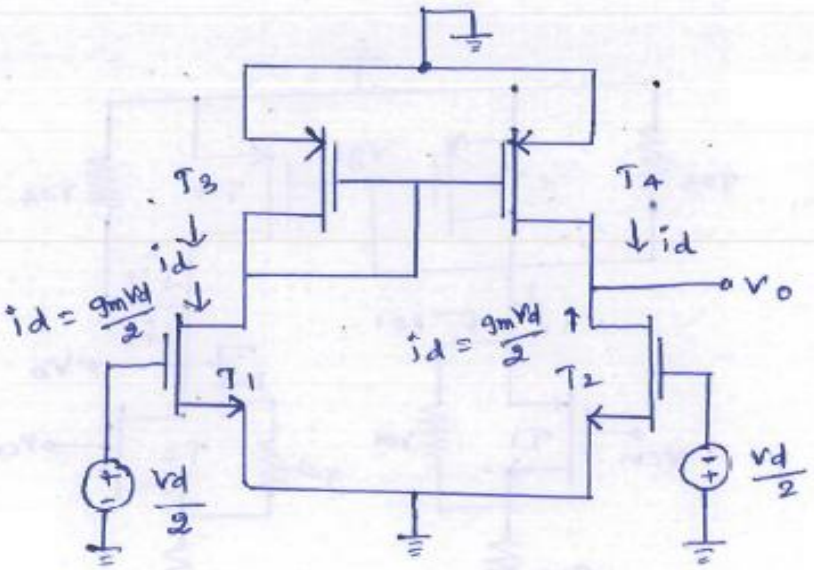


Fig: ac equivalent circuit

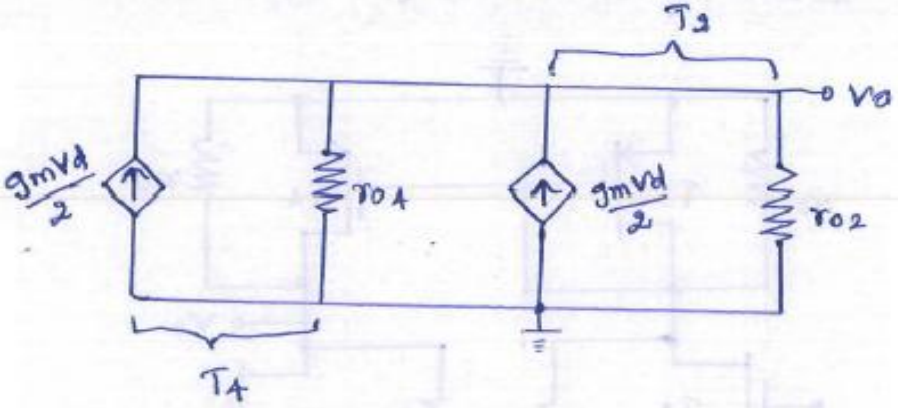


Fig: Small-signal equivalent circuit at drain node of T2 & T4

Differential gain (Ad)

From the equivalent circuit

$$V_o = \left(\frac{g_m V_d}{2} + \frac{g_m V_d}{2} \right) (r_{o2} \| r_{o4})$$

$$\therefore A_d = \frac{V_o}{V_d} = g_m (r_{o2} \| r_{o4})$$

$$= \frac{g_m}{\frac{1}{r_{o2}} + \frac{1}{r_{o4}}} = \frac{g_m}{g_{o2} + g_{o4}} \quad \text{——— (7)}$$

W.k.T

$$g_m = 2\sqrt{k_n I_D} = \sqrt{2 k_n I_Q} \qquad \because I_D = \frac{I_Q}{2}$$

$$g_{o2} = \lambda_2 I_{DQ2} = \lambda_2 \frac{I_Q}{2}$$

$$g_{o4} = \lambda_4 I_{DQ4} = \lambda_4 \frac{I_Q}{2}$$

Substitute g_m, g_{o2} & g_{o4} in eqn (1) we get

$$A_d = \frac{\sqrt{2 k_n I_Q}}{\lambda_2 \frac{I_Q}{2} + \lambda_4 \frac{I_Q}{2}} = \frac{2\sqrt{2 k_n I_Q}}{I_Q(\lambda_2 + \lambda_4)} = 2\sqrt{\frac{2k_n}{I_Q}} \cdot \frac{1}{\lambda_2 + \lambda_4} \quad \text{—(2)}$$

$$\therefore \boxed{A_d = 2\sqrt{\frac{2k_n}{I_Q}} \cdot \frac{1}{\lambda_2 + \lambda_4}}$$

Common Mode gain (Acm)

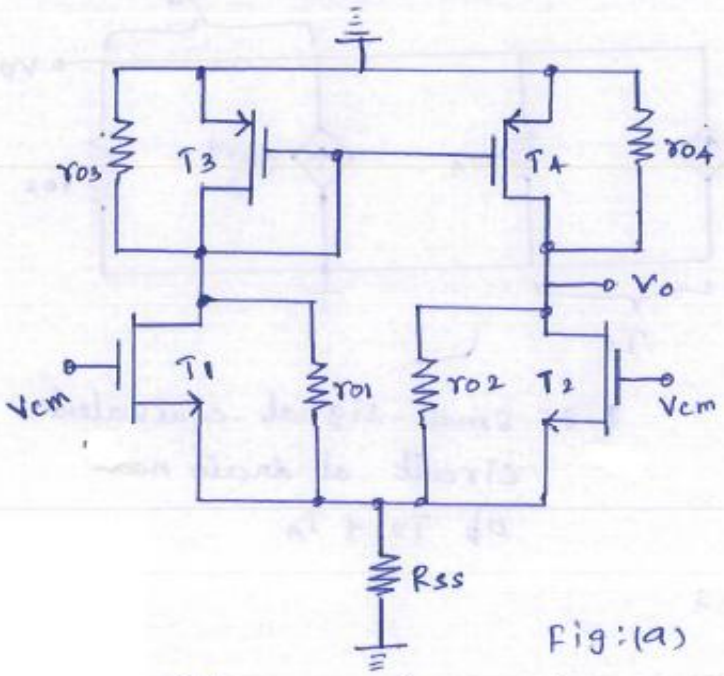


Fig:(a)

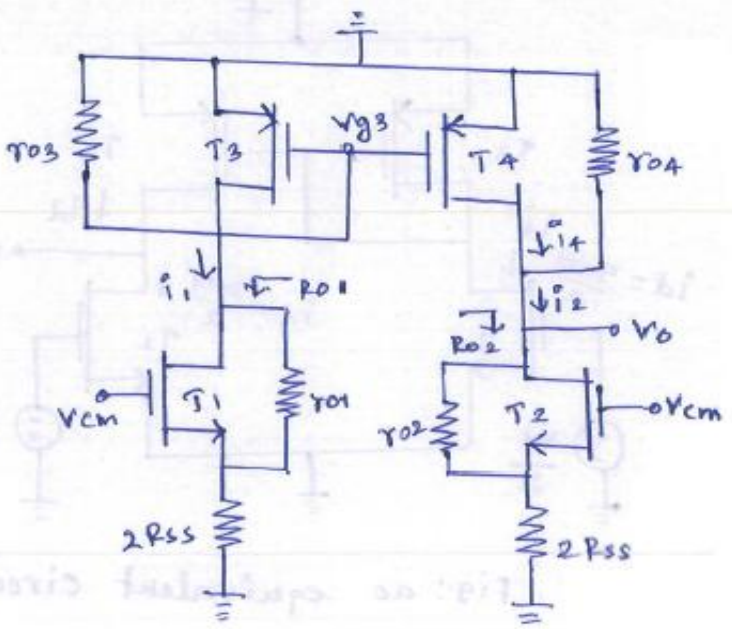


Fig: (b)

Fig: (a) & (b) Determining the common mode gain

* Here, the resistance Rss is the Output resistance of the bias current source I.
* We can split Rss equally between T_1 & T_2 as shown in Fig: b
* From fig(b) we can write

$$i_1 = i_2 \cong \frac{V_{cm}}{2R_{ss}} \quad \because 2R_{ss} >> \frac{1}{g_m} \text{ & effect of } r_{o1} \text{ & } r_{o2}$$

is negligible.

* The output resistance of each of T_1 & T_2 is given by

$$R_{O1} = R_{O2} = r_o + 2R_{SS} + 2g_m r_o R_{SS}$$

$$r_{O1} = r_{O2} = r_O$$

&

$$g_{m1} = g_{m2} = g_m$$

* It's Important to know that-

$$R_{O1} >> \left(r_{O3} \parallel \frac{1}{g_{m3}}\right) \text{ & } R_{O2} >> \left(r_{O4} \parallel \frac{1}{g_{m4}}\right)$$

* We can neglect R_{O1} & R_{O2} in finding the total resistance between each of the drain nodes & ground.

* The current i_1 is passed through the parallel resistance of T_3 to produce voltage V_{g3} as

$$V_{g3} = -i_1 \left(\frac{1}{g_{m3}} \| r_{o3} \right)$$

* The transistor T_4 senses this voltage & produces

$$i_4 = -g_{m4} V_{g3} = i_1 g_{m4} \left(\frac{1}{g_{m3}} \| r_{o3} \right)$$

* At the Output node, the current difference between i_4 & i_2 passes through r_{o4} ($R_{O2} >> r_{o4}$ & hence neglected) to provide V_o.

$$\therefore V_o = (i_4 - i_2) r_{o4}$$

* Substitute value of i_4 we have

$$V_o = \left[i_1 g_{m4} \left(\frac{1}{g_{m3}} \| r_{o3} \right) - i_2 \right] r_{o4}$$

* substitute values of i_1, i_2 & setting $g_{m3} = g_{m4}$ we have

$$V_o = \left[\frac{V_{cm}}{2R_{ss}} g_{m3} \left(\frac{1}{g_{m3}} \| r_{o3} \right) - \frac{V_{cm}}{2R_{ss}} \right] r_{o4}$$

$$= \frac{V_{cm}}{2R_{ss}} \left[g_{m3} \left(\frac{r_{o3} / g_{m3}}{r_{o3} + \frac{1}{g_{m3}}} \right) - 1 \right] r_{o4}$$

$$= \frac{V_{cm}}{2R_{ss}} \left[\frac{g_{m3} r_{o3}}{g_{m3} r_{o3} + 1} - 1 \right] r_{o4}$$

$$= \frac{V_{cm}}{2R_{ss}} \left[\frac{-1}{g_{m3} r_{o3} + 1} \right] r_{o4}$$

$$\therefore \boxed{A_{cm} = \frac{V_o}{V_{cm}} = \frac{-1}{2R_{ss}} \cdot \frac{r_{o4}}{g_{m3} r_{o3} + 1}}$$

* Considering the fact $g_{m3} r_{o3} >> 1$ & $r_{o3} = r_{o4}$ we have

$$\boxed{A_{cm} \cong \frac{-1}{2R_{ss}} \cdot \frac{1}{g_{m3}} = \frac{-1}{2R_{ss} g_{m3}}}$$

* Since R_{ss} is very large; common mode gain is very small.

Common Mode Rejection Ratio (CMRR)

$$CMRR = \frac{|Ad|}{|Acm|} = [g_m (r_{o2} \| r_{o4})] [2R_{ss} g_{m3}]$$

When

$$r_{o2} = r_{o4} = r_o$$

&

$$g_m = g_{m3}$$

So

$$\boxed{CMRR = \frac{|Ad|}{|Acm|} = (g_m r_o)(R_{ss} g_m)}$$

∴ 2Mark.

PROBLEMS

Design the MOSFET current source for following specifications.
$V_{DD} = 4V$, $I_{REF} = 120\mu A$, $L_1 = L_2 = 1\mu m$, $W_1 = W_2 = 10\mu m$, $V_T = 0.7V$ & $K_n' = 200\ \mu A/V^2$. Find the value of R, calculate the lowest possible value of V_o & calculate r_{o2} if early voltage $V_A' = 20V/\mu$ find the change in Output current if change in V_O is $+2V$.

Given Data:

$V_{DD} = 4V$, $I_{REF} = 120\mu A$ $L_1 = L_2 = 1\mu m$ $W_1 = W_2 = 10\mu m$

$V_T = 0.7V$ $K_n' = 200\ \mu A/V^2$ $V_{A2}' = 20\ V/\mu m$

Solution:

Here $L_1 = L_2$ & $W_1 = W_2$ $\Rightarrow$ So MOSFETs are identical

& $I_O = I_{REF} = 120\mu A$.

$$I_{D1} = I_{REF} = \frac{1}{2} K_n' \left(\frac{W_1}{L_1}\right) (V_{us} - V_T)^2$$

$$120 = \frac{1}{2} \times 200 \times 10 (V_{us} - V_T)^2$$

$$(V_{us} - V_T)^2 = V_{ov}^2 = 0.12$$

$$V_{ov} = 0.3464\ V$$

$$V_{GS} = V_T + V_{OV} = 0.7 + 0.3464 = 1.0464\ V$$

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{4 - 1.0464}{120 \times 10^{-6}} = 24.61\ k\Omega$$

$$V_{omin} = V_{OV} = 0.3464\ V$$

$$V_{A2} = V'_{A2} \times L_2 = 20 \times 1 = 20\ V$$

$$r_{o2} = \frac{V_{A2}}{I_O} = \frac{20}{120 \times 10^{-6}} = 166.67\ k\Omega$$

$$\Delta I_O = \frac{\Delta V_O}{r_{o2}} = \frac{2}{166.67 k\Omega^3} = 12\ \mu A$$

Design a MOSFET current source amplifier for following specifications: $V_{DD} = 5V$, $K_n' = 40\ \mu A/V^2$ $V_T = 1V$ $\lambda = 0$ $I_{REF} = 0.2mA$, $I_O = 0.1mA$ & $V_{DS2}(sat) = 0.8V$

Given Data:

$V_{DD} = 5V$, $K_n' = 40\ \mu A/V^2$, $V_T = 1V$, $\lambda = 0$, $I_{REF} = 0.2mA$

$I_O = 0.1mA$ $V_{DS2}(sat) = 0.8V$

Solution:

$$V_{DS2}(sat) = V_{OV} = 0.8V$$

$$V_{GS2} = V_{OV} + V_T = 0.8 + 1.0 = 1.8V$$

$$I_O = \frac{1}{2} K_n' \left(\frac{W_2}{L_2}\right)(V_{GS2} - V_T)^2$$

$$\frac{W_2}{L_2} = \frac{I_O}{\frac{1}{2} K_n' (V_{GS2} - V_T)^2} = \frac{0.1 \times 10^{-3}}{\frac{1}{2} \times 40 \times 10^{-6} (1.8-1)^2} = 7.81$$

$$I_{REF} = \frac{1}{2} \left(\frac{W_1}{L_1}\right) K_n' (V_{GS1} - V_T)^2$$

$$\frac{W_1}{L_1} = \frac{I_{REF}}{\frac{1}{2} K_n' (V_{GS1} - V_T)^2}$$

Since $V_{GS1} = V_{GS2}$

$$\frac{W_1}{L_1} = \frac{0.2 \times 10^{-3}}{\frac{1}{2} \times 40 \times 10^{-6} (1.8-1)^2} = 15.62$$

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{5 - 1.8}{0.2 \times 10^{-3}} = 16K$$

TWO MARKS

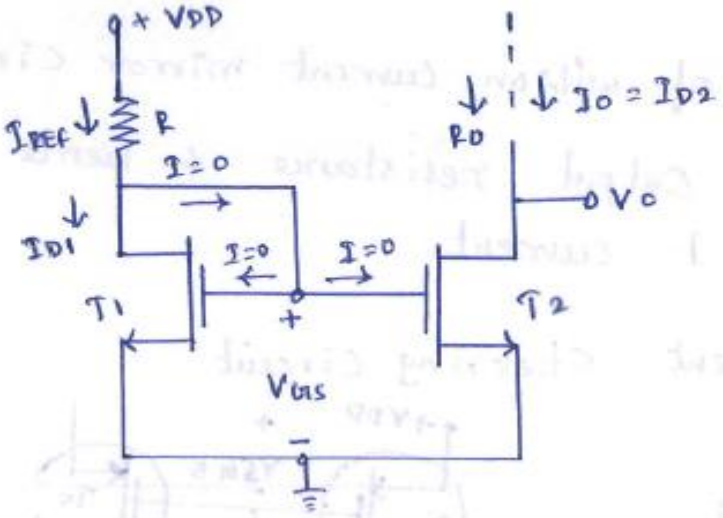
Define Current Steering.

The constant dc current called reference current is generated at one location & is then replicated at various other locations for biasing the various stages of amplifier present in the circuit. This process is known as current steering.

State the advantages of current steering process.

1. The external components such as precision resistors required to generate a predictable & stable reference current, need not be repeated for every amplifier stage.
2. The bias currents of the various stages track each other when there is any change due to power-supply voltage (or) temperature.

Draw the basic constant current source circuit using MOSFET



Draw the wilson current mirror circuit.