

BIST

Built In Self Test

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Built-in Self-test



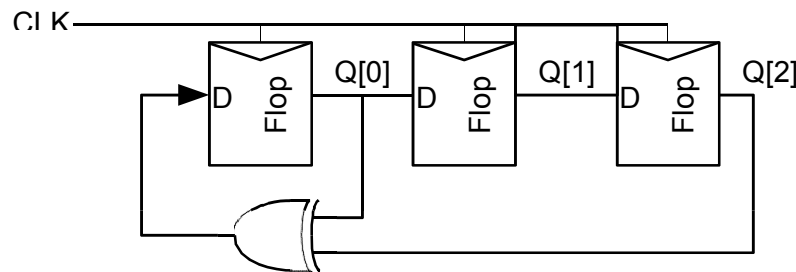
- ❑ Built-in self-test lets blocks test themselves
 - Generate pseudo-random inputs to comb. logic
 - Combine outputs into a *syndrome*
 - With high probability, block is fault-free if it produces the expected syndrome

PRSG



❑ Linear Feedback Shift Register

- Shift register with input taken from XOR of state
- *Pseudo-Random Sequence Generator*

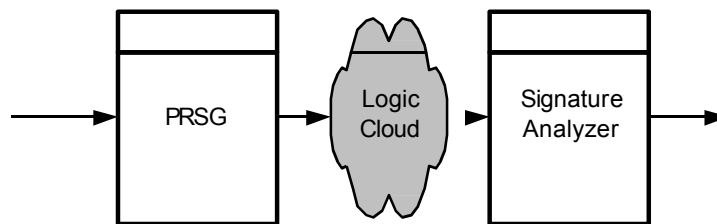
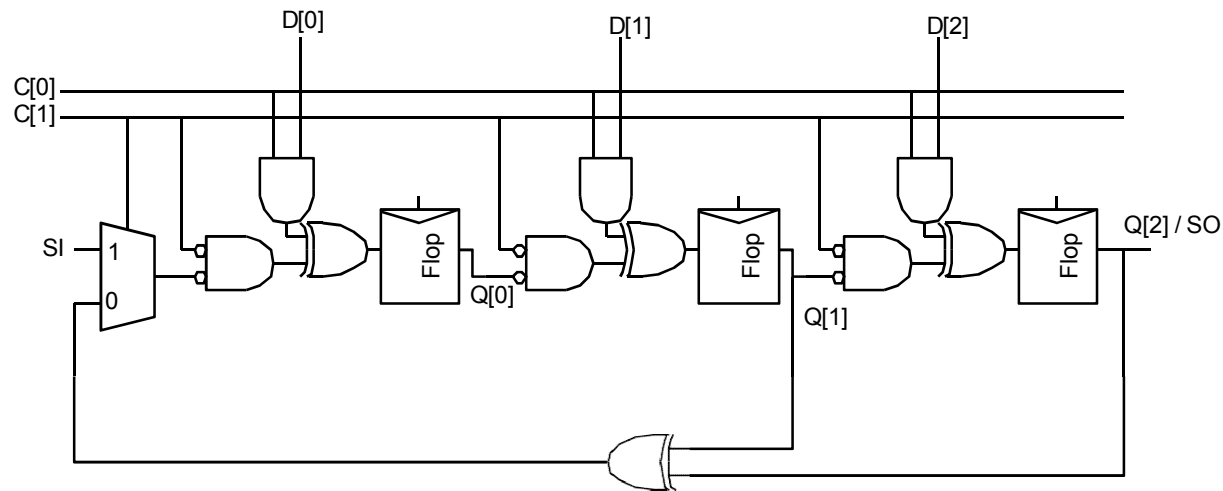


Step	Q
0	111
1	110
2	101
3	010
4	100
5	001
6	011
7	111 (repeats)

BILBO



- ❑ Built-in Logic Block Observer
 - Combine scan with PRSG & signature analysis



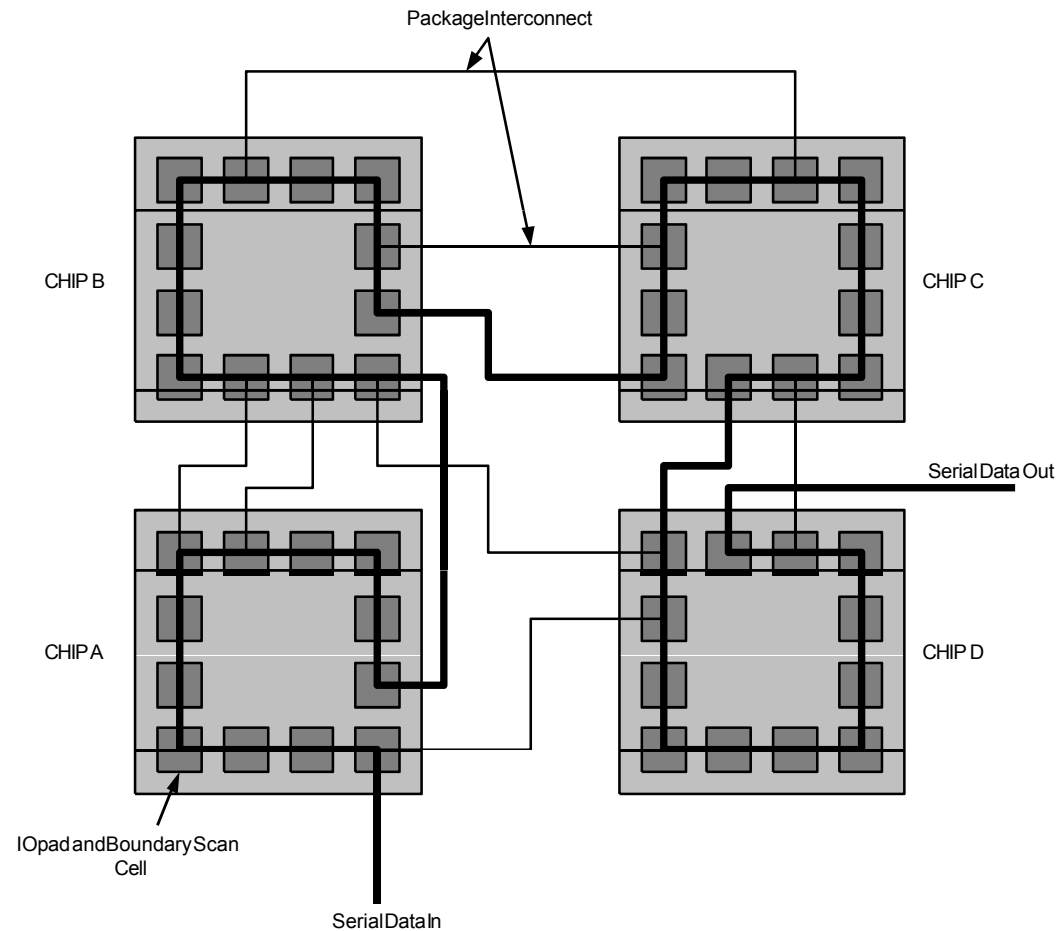
MODE	C[1]	C[0]
Scan	0	0
Test	0	1
Reset	1	0
Normal	1	1

Boundary Scan



- ❑ Testing boards is also difficult
 - Need to verify solder joints are good
 - Drive a pin to 0, then to 1
 - Check that all connected pins get the values
- ❑ Through-hole boards used “bed of nails”
- ❑ SMT and BGA boards cannot easily contact pins
- ❑ Build capability of observing and controlling pins into each chip to make board test easier

Boundary Scan Example



Boundary Scan Interface



- ❑ Boundary scan is accessed through five pins
 - TCK: test clock
 - TMS: test mode select
 - TDI: test data in
 - TDO: test data out
 - TRST*: test reset (optional)

- ❑ Chips with internal scan chains can access the chains through boundary scan for unified test strategy.

Summary



- BIST
- PRSG
- BILBO
- BOUNDARY SCAN WITH EXAMPLE
- INTERFACE