SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

19ECB231 –DIGITAL ELECTRONICS

II YEAR/ III SEMESTER

UNIT 5 –DEGITAL LOGIC FAMILIES AND PLD

TOPIC 6 – Introduction to PLD

Problem definition

- ***Problems by Using Basic Gates***
- Many components on PCB:
  - As no. of components rise, nodes interconnection complexity grow exponentially
  - Growth in interconnection will cause increase in interference, PCB size, PCB design cost, and manufacturing time

- ***Solution***

- The purpose of a PLD device is to permit elaborate digital logic designs to be implemented by the user in a single device.

- Can be erased electrically and reprogrammed with a new design, making them very well suited for academic and prototyping

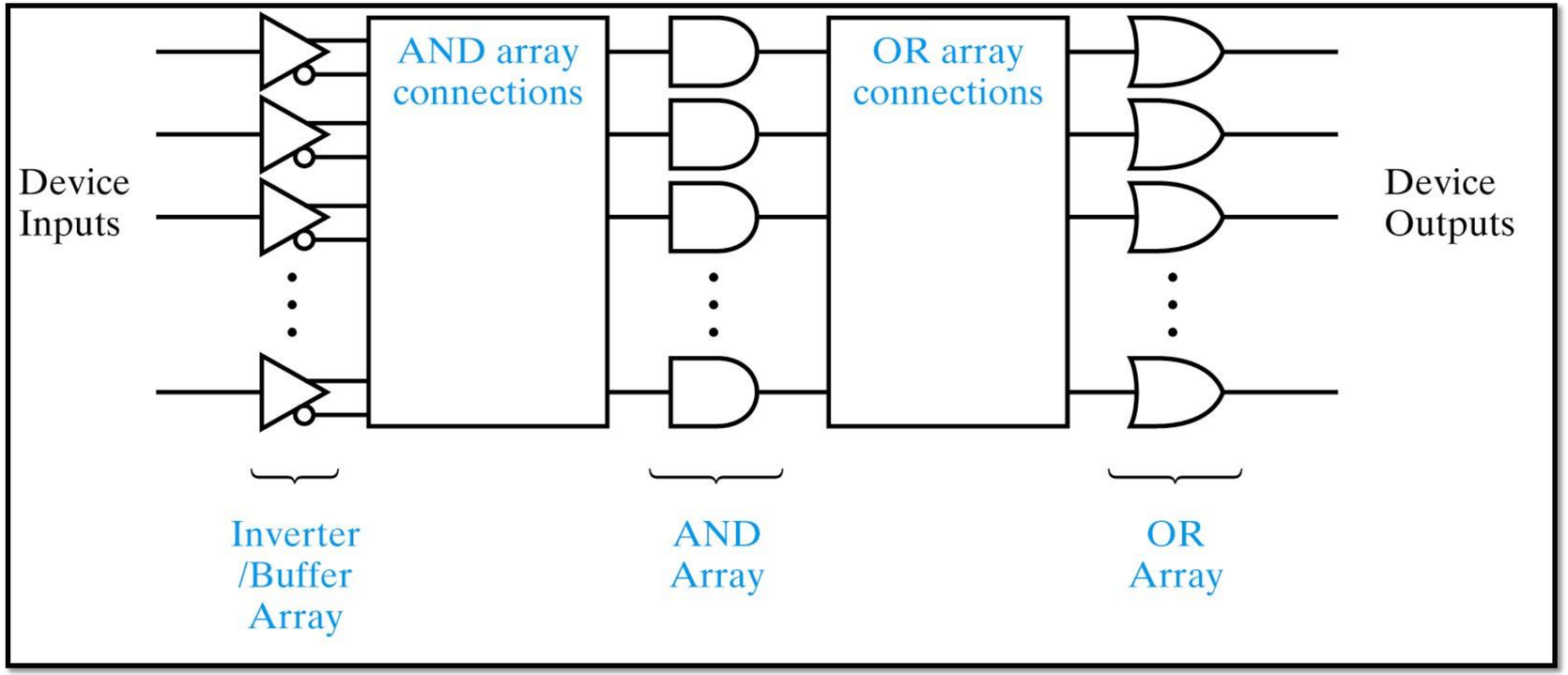
Taxonomies of ICs

- Design Methodology
  - Standard Components (SSI/MSI/LSI)
    - Off-the-shelf Components
    - Basic Universal Building Blocks (AND, OR, NAND, NOR…)
  - Application-Specific Standard Parts (ASSP)
    - Target Specific Application Area, but not Customer
    - e.g. Printer Controller, USB Interface IC, HDD I/F
  - Application-Specific IC (ASIC)
    - Custom Design of IC Targeting Specific Market
    - Full-custom, standard cell, gate-arrays
    - e.g. ATI 3D Graphics Engine
  - Programmable Logic Devices (PLD)
    - Can be used to implement wide variety designs
    - e.g. FPGA (Field-Programmable Gate Arrays)

PLDs

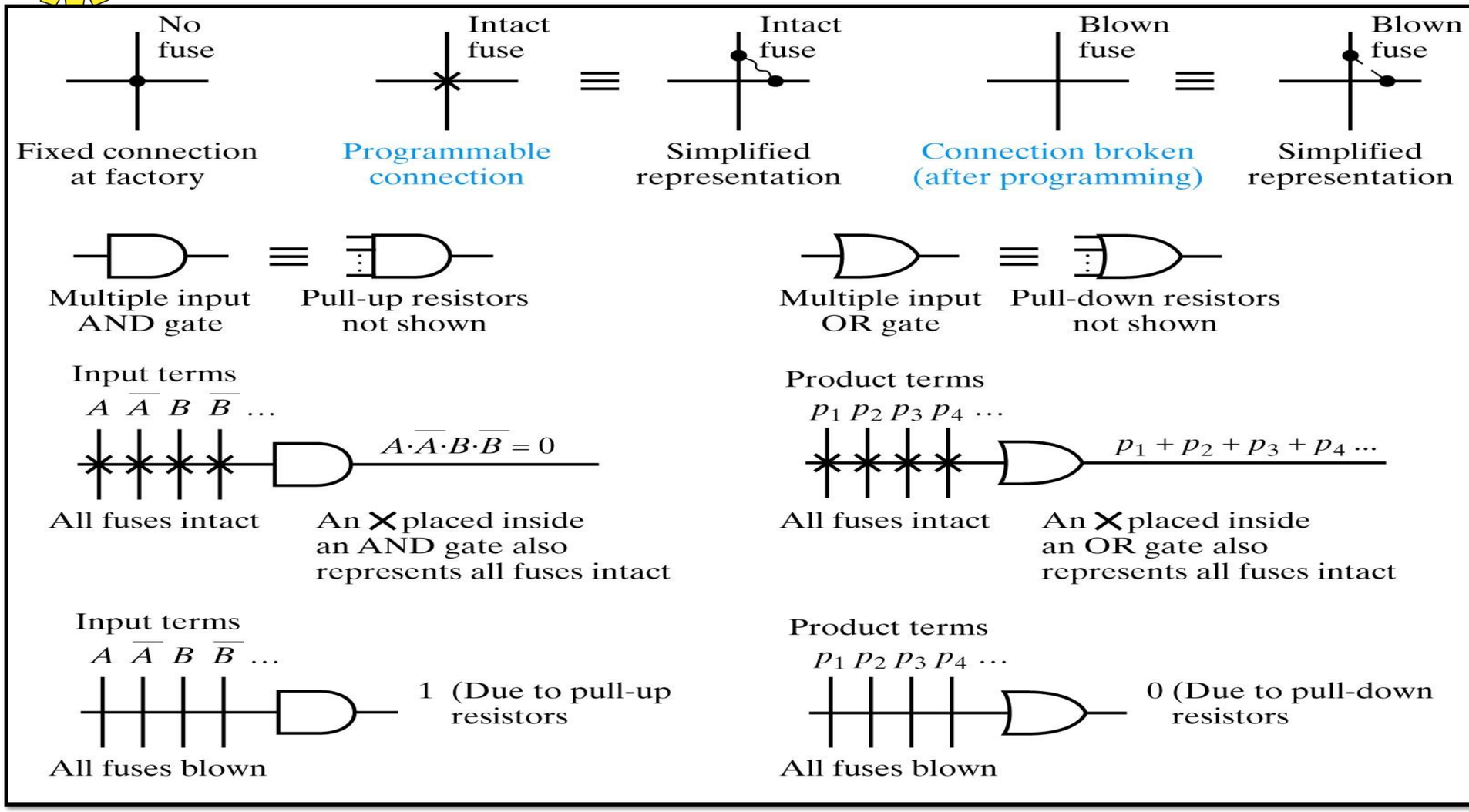
- Programmable Logic Devices (PLDs)
  - **PROM:** Programmable Read Only Memories (1960s)
  - **PLA:** Programmable Logic Arrays [Signetics] (1975)
  - **PALÔ:** Programmable Array Logic [MMI] (1976)
  - **GALÔ:** Generic Array Logic
  - **CPLDs** (Complex PLDs)
  - **FPGA:** Field Programmable Gate Arrays

AND/OR Array Architecture

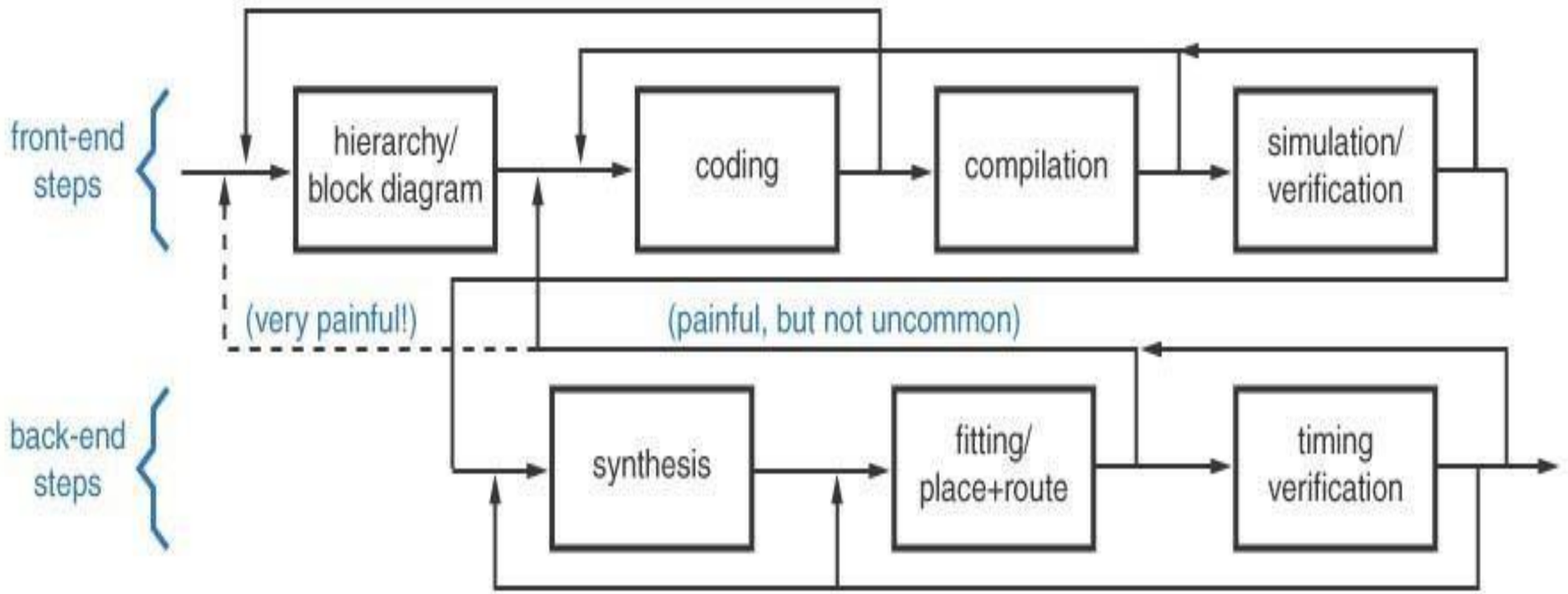


Device type	AND array	OR array	Product term sharing
PROM	Fixed at factory	Programmable	Yes
PLA	Programmable	Programmable	Yes
PAL/GAL	Programmable	Fixed at factory	No

Programmable Symbology

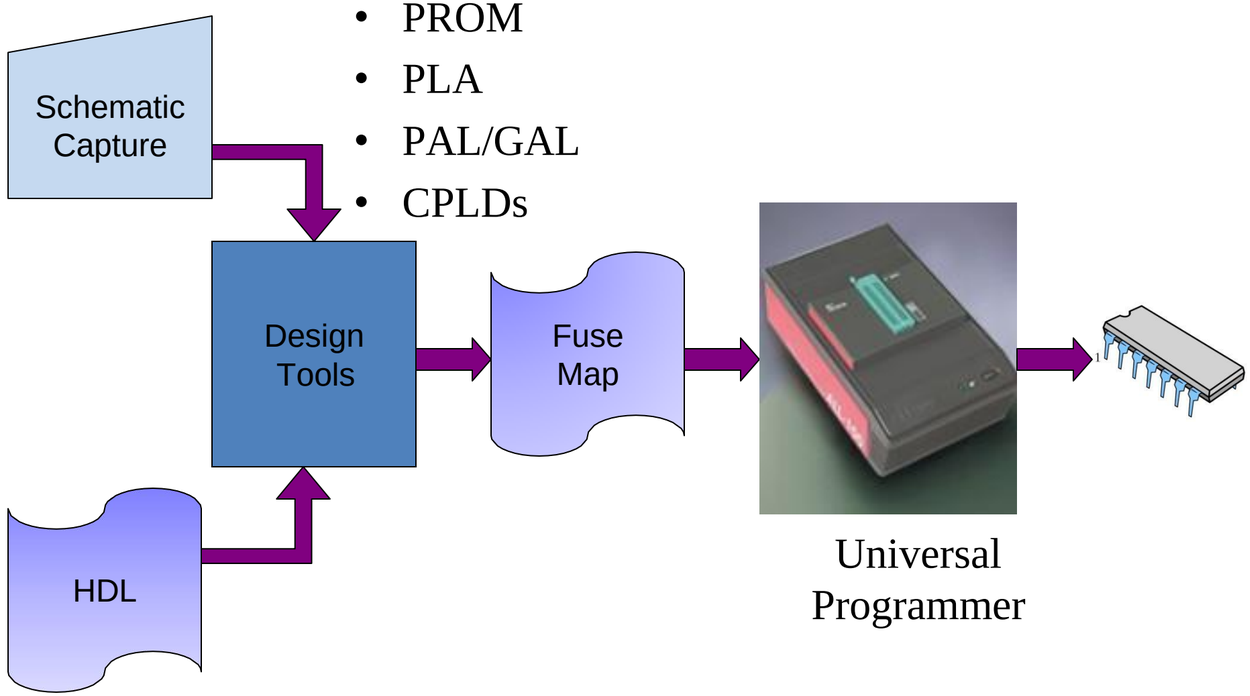


PLD Implementation



PLD Implementation

- PROM
- PLA
- PAL/GAL
- CPLDs



Universal Programmer

Tool and PLD vendors: Xilinx, Altera, Lattice

Advantages to PLDs

- Shorten design time
  - Rapid prototyping!
- Rapid design changes
  - Reprogrammable
    - No masks, jumpers, PCB traces
- Decrease PCB “real estate”
  - Less space than multiple standard logic packages
- Improve reliability
  - Fewer packages, fewer external interconnects

THANK YOU