SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB204 – LINEAR AND DIGITAL CIRCUITS

II YEAR/ III SEMESTER

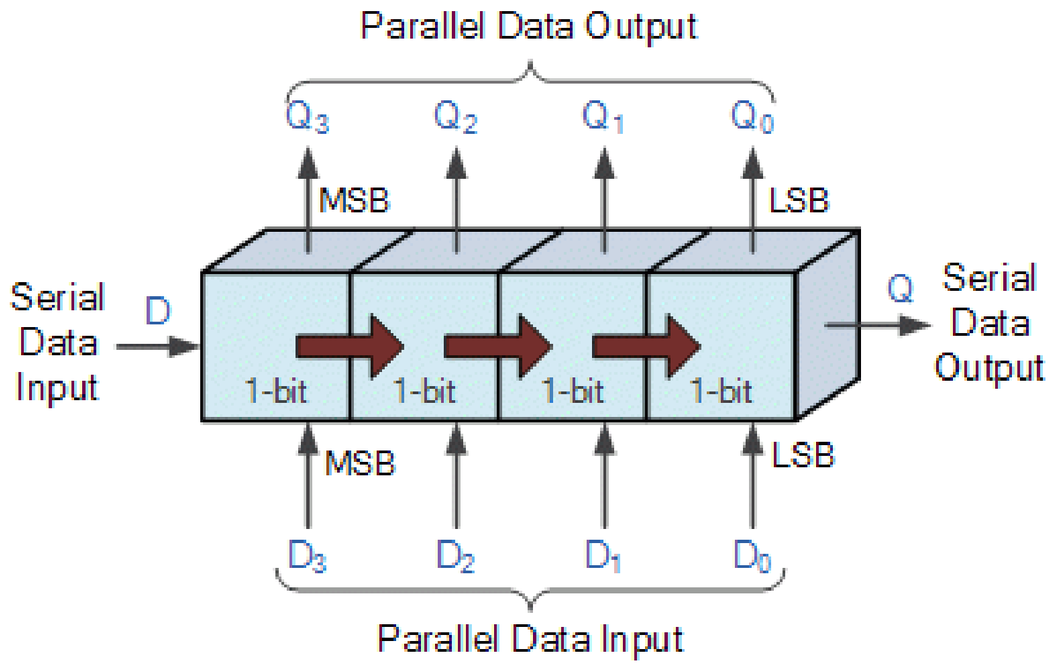
UNIT 3 – COMBINATIONAL and SEQUENTIAL CIRCUITS

TOPIC – Shift registers- SISO,SIPO, PISO,PIPO

Guess the Topic????

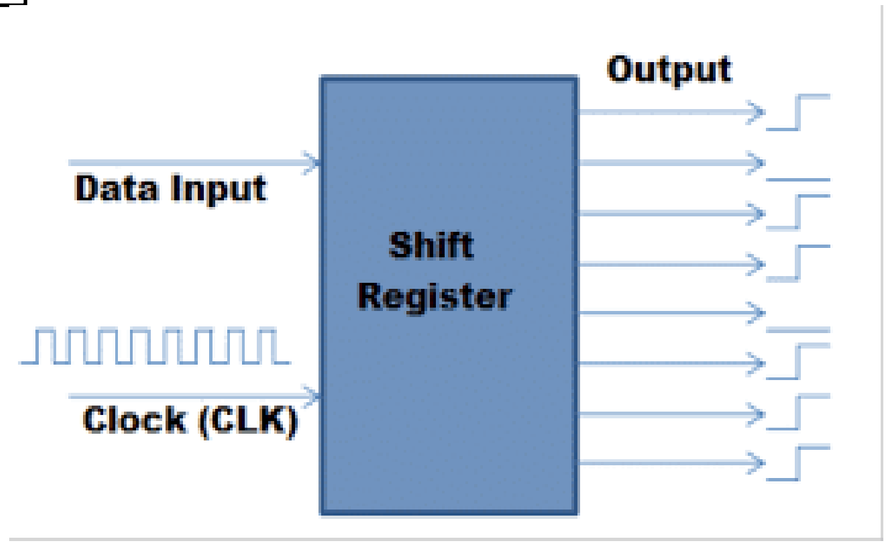
The Shift Register

The Shift Register is another type of sequential logic circuit that can be used for the storage or the transfer of binary data



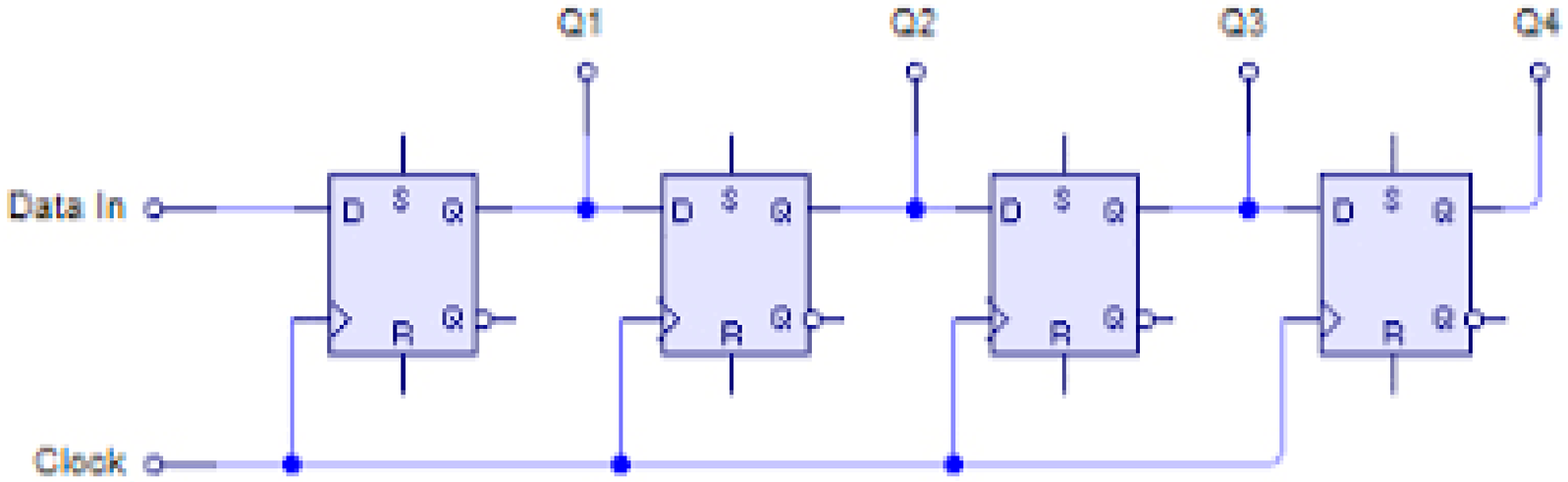
The Shift Register

A shift register basically consists of several single bit “D-Type Data Latches”, one for each data bit, either a logic “0” or a “1”, connected together in a serial type daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on.



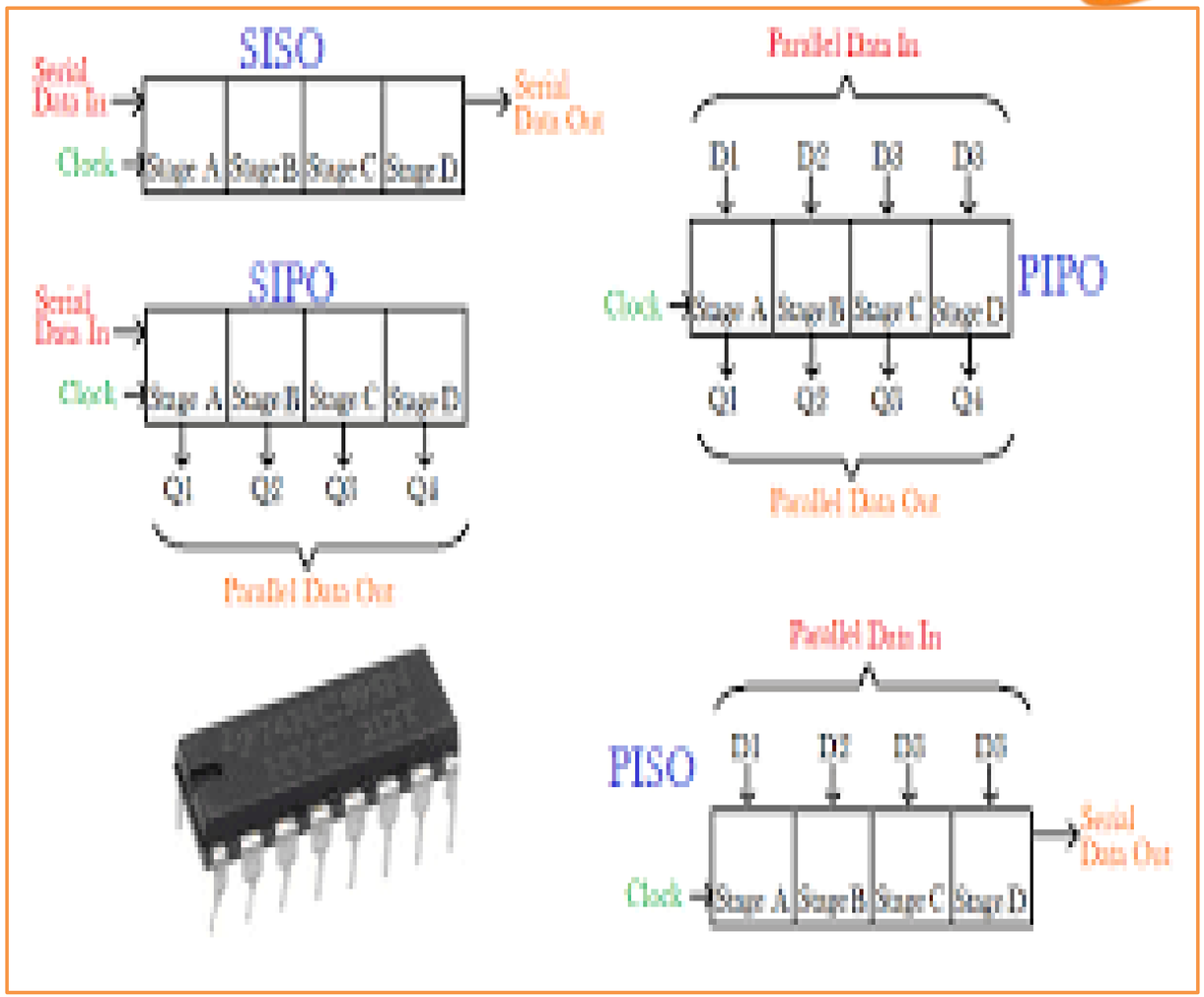
The Shift Register

Data bits may be fed in or out of a shift register serially, that is one after the other from either the left or the right direction, or all together at the same time in a parallel configuration.



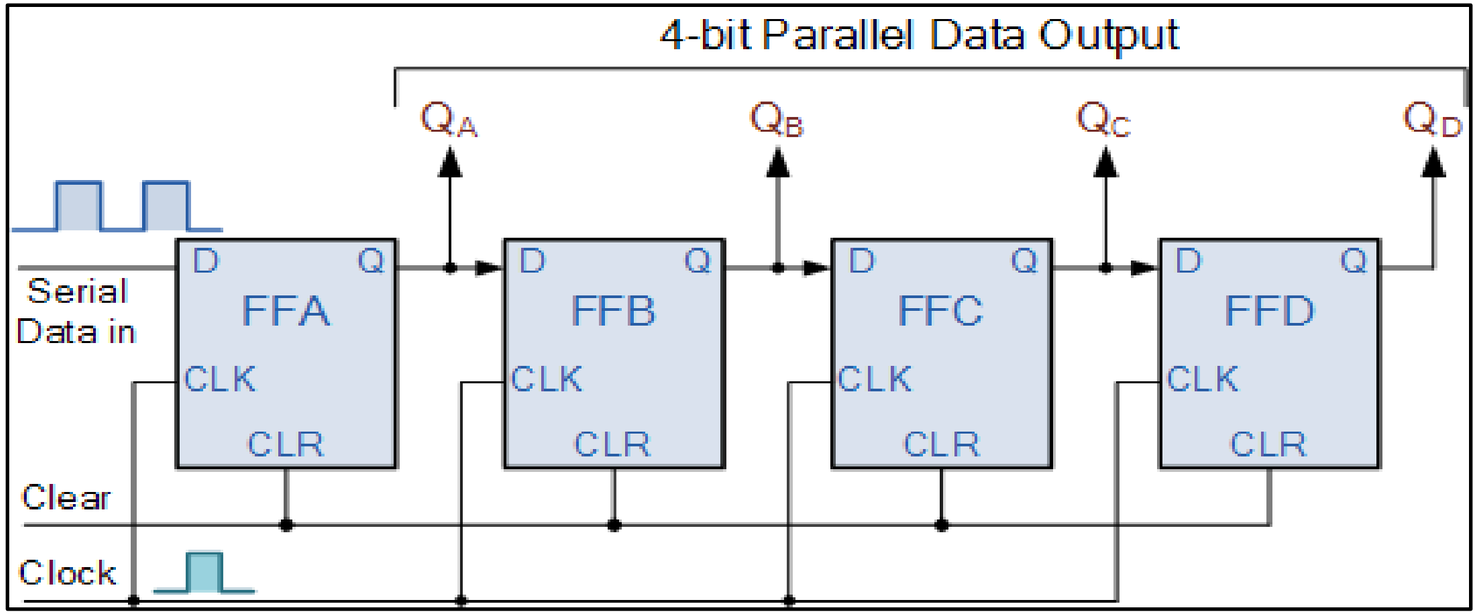
The Shift Register Types

- Serial-in to Parallel-out (SIPO)
- Serial-in to Serial-out (SISO)
- Parallel-in to Serial-out (PISO)
- Parallel-in to Parallel-out (PIPO

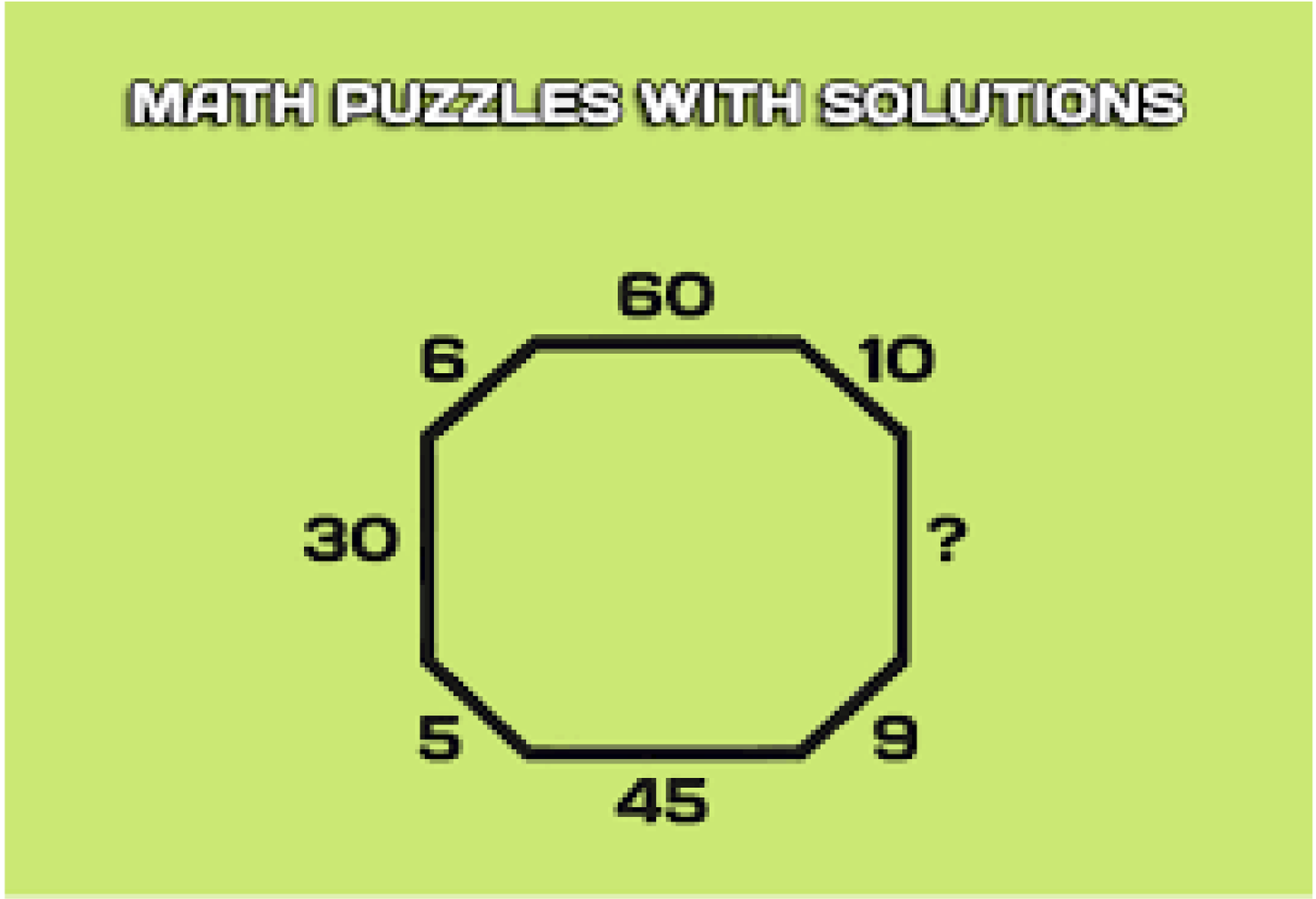


Serial-in to Parallel-out (SIPO)

The register is loaded with serial data, one bit at a time, with the stored data being available at the output in parallel form.

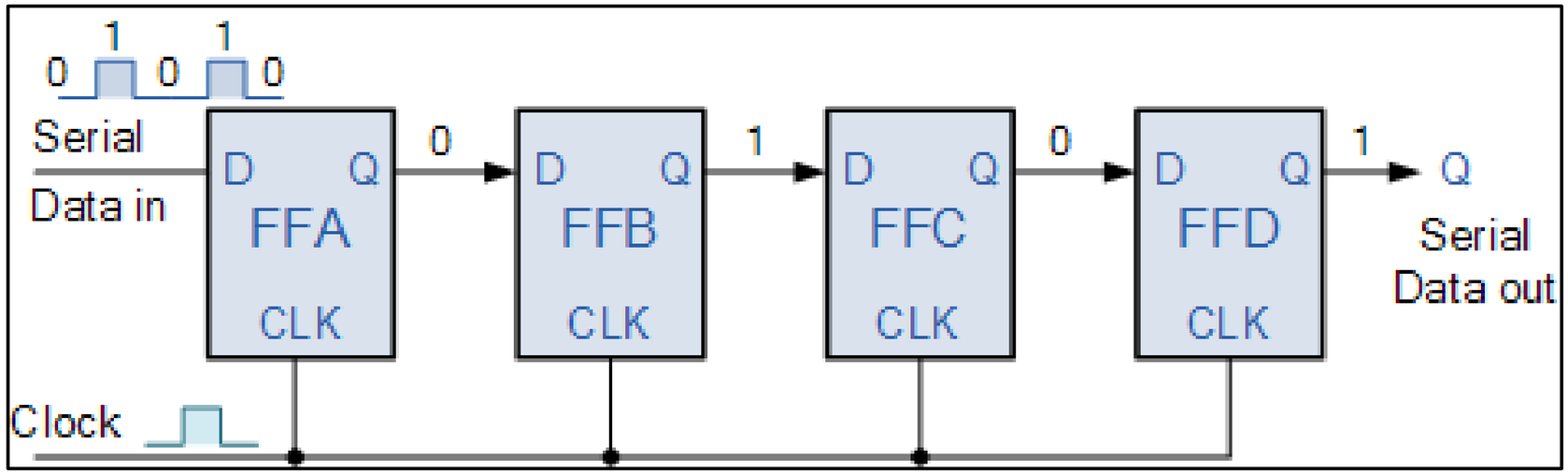


ACTIVITY TIME



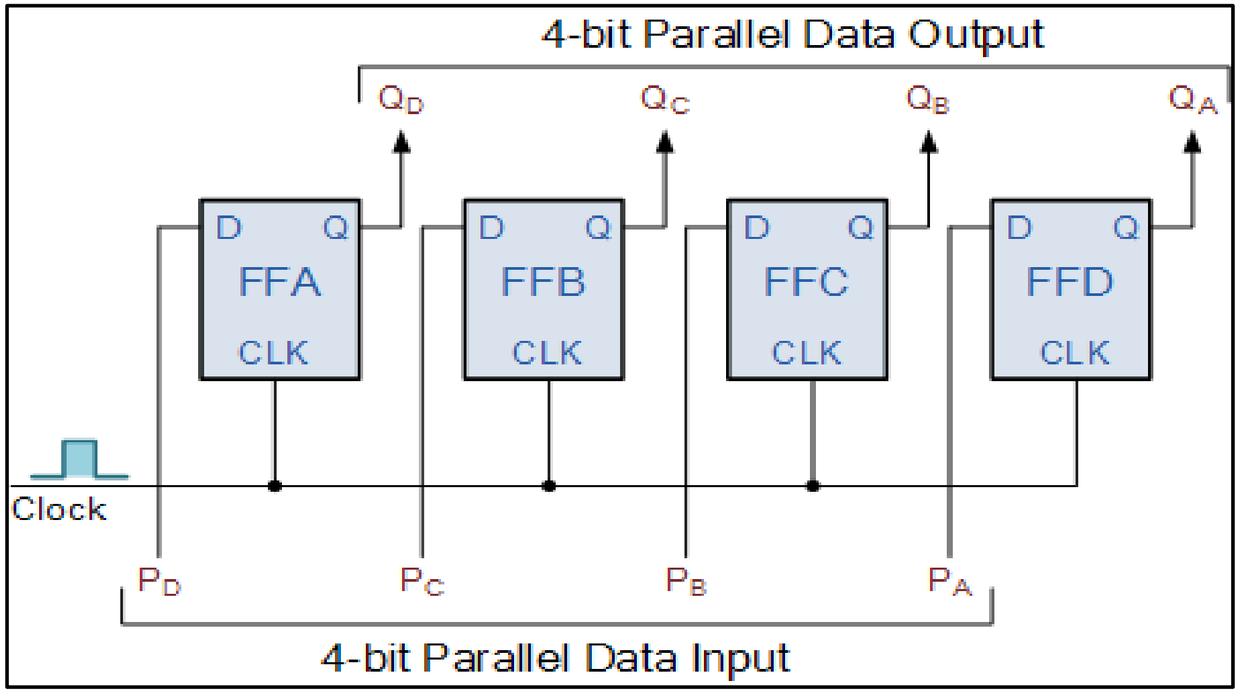
SERIAL-IN TO SERIAL-OUT (SISO) SHIFT REGISTER

The data is shifted serially “IN” and “OUT” of the register, one bit at a time in either a left or right direction under clock control



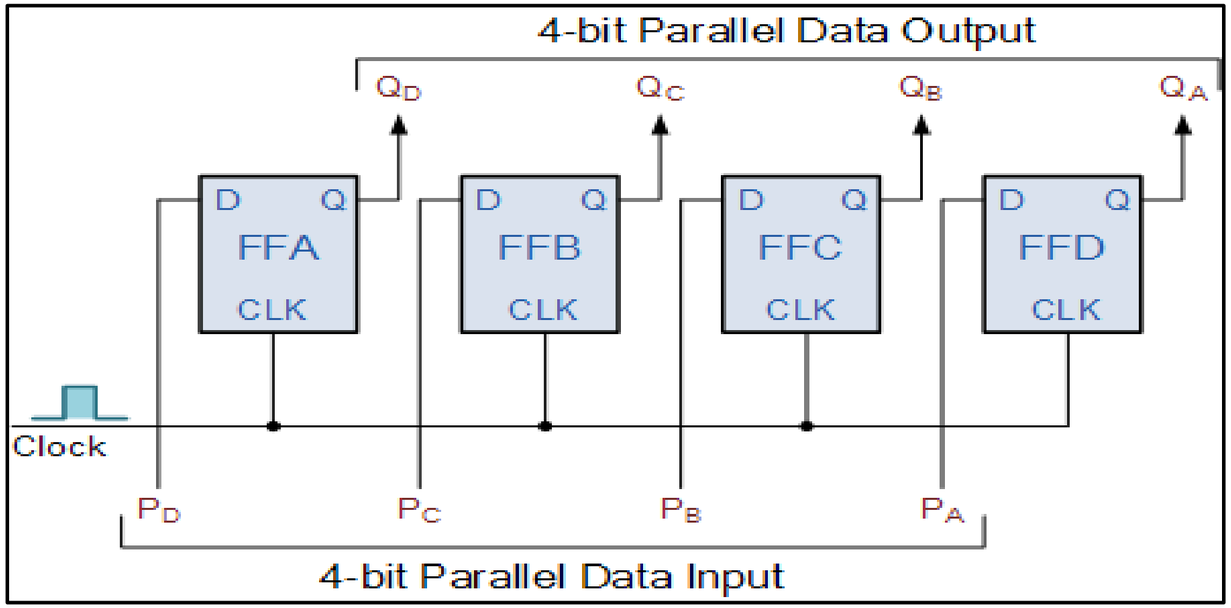
PARALLEL-IN TO SERIAL-OUT (PISO) SHIFT REGISTER

The parallel data is loaded into the register simultaneously and is shifted out of the register serially one bit at a time under clock control.



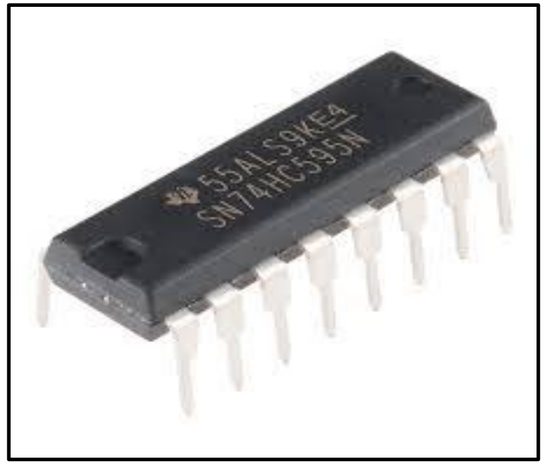
PARALLEL-IN TO PARALLEL-OUT (PIPO)

The parallel data is loaded simultaneously into the register, and transferred together to their respective outputs by the same clock pulse.



SUMMARY

- A simple Shift Register can be made using only D-type flip-Flops, one flip-Flop for each data bit.
- The output from each flip-Flop is connected to the D input of the flip-flop at its right.
- Shift registers hold the data in their memory which is moved or “shifted” to their required positions on each clock pulse.
- Each clock pulse shifts the contents of the register one bit position to either the left or the right.
- The data bits can be loaded one bit at a time in a series input (SI) configuration or be loaded simultaneously in a parallel configuration (PI).



ASSESSMENT TIME

Think, Pair, Share

What's the issue / question / topic?	What do I think about it?	What does my partner think?	What will we share?

THANK YOU