SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

19ECB204 – LINEAR AND DIGITAL CIRCUITS

II YEAR/ III SEMESTER

UNIT 4 – COMBINATIONAL and SEQUENTIAL CIRCUITS

TOPIC - Design of Counters- synchronous up/down counter

What is a Counter?

➢A digital circuit which is used for a counting pulses is known as counter.

➢ Counter is the widest application of flip-flops.

➢ It is a group of flip-flops with a clock signal applied.
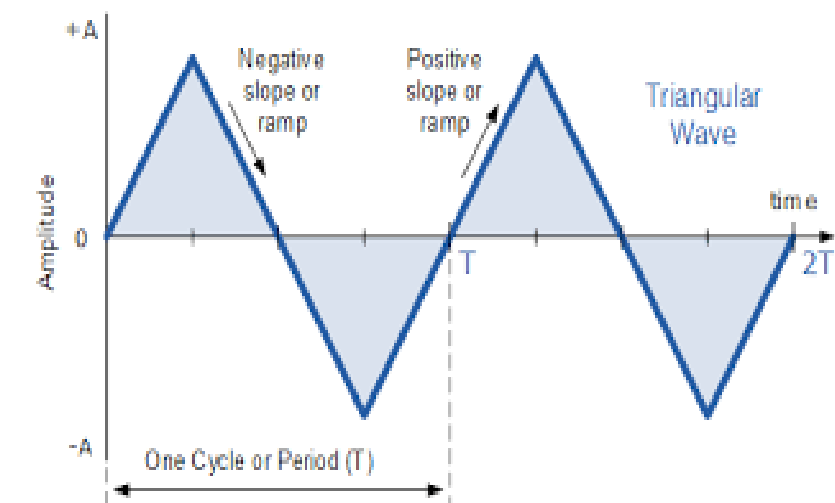
Applications of Counters

Frequency counters

Digital clocks
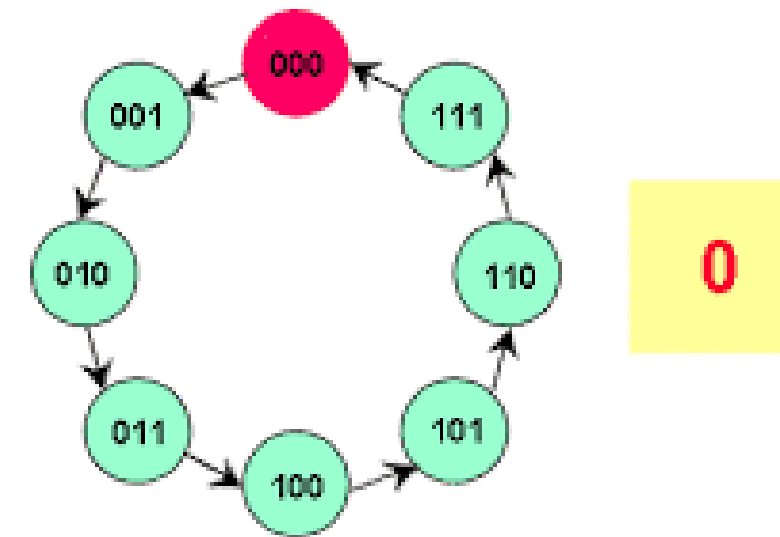
Digital triangular wave generator

Types of Design counters

Two Types
1. Asynchronous Counter or Ripple Counter.
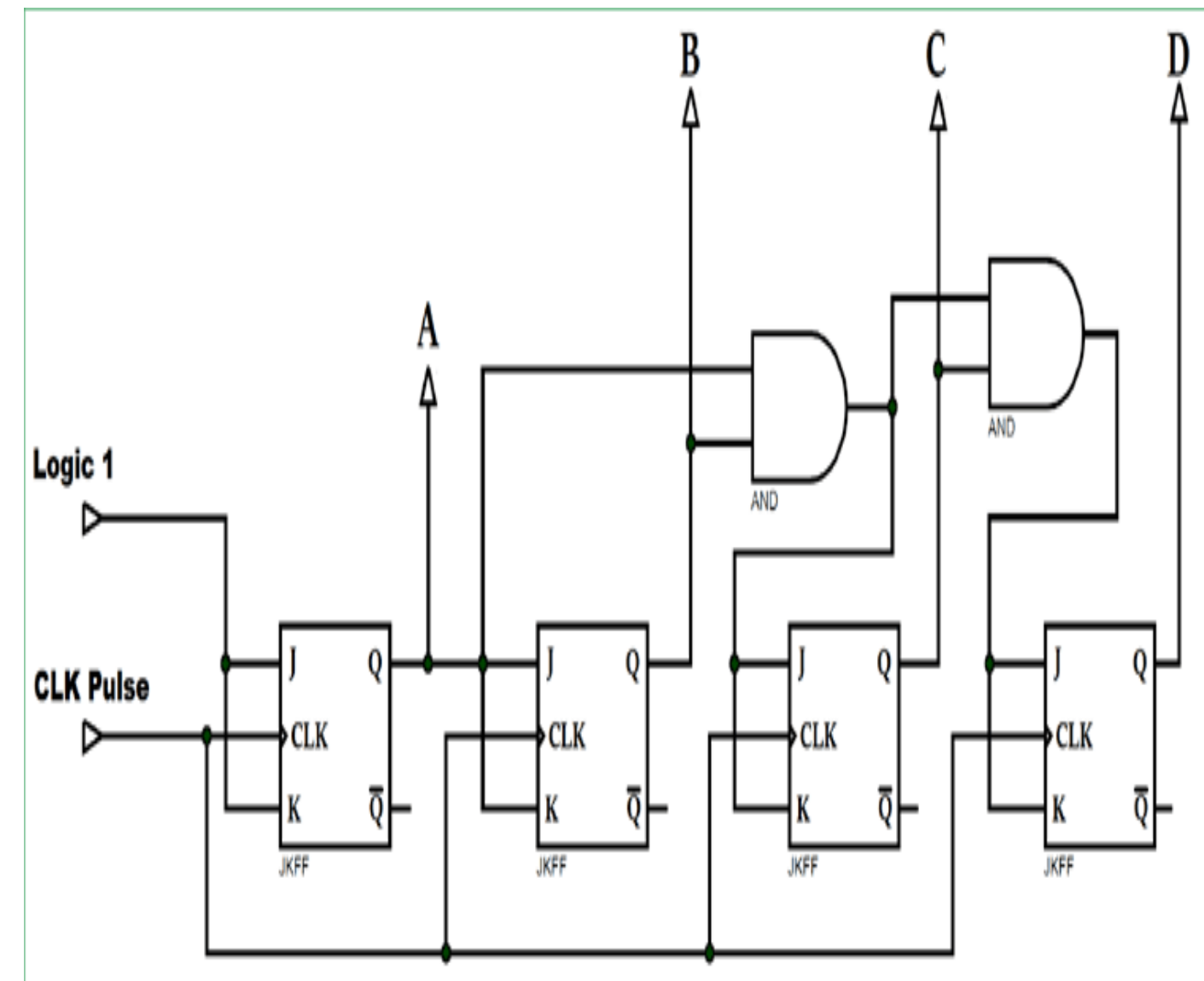2. Synchronous Counter

Synchronous Counter

➢**In synchronous counter**, the clock input across all the flip-flops use the same source and create the same clock signal at the same time.

➢ A counter which is using the same clock signal from the same source at the same time is called **Synchronous counter**.

Activity

Team Building

Design of Counters- synchronous up/down counter/ LINEAR AND DIGITAL CIRCUITS/Mr.N.Arunkumar/AP/ECE/SNSCT
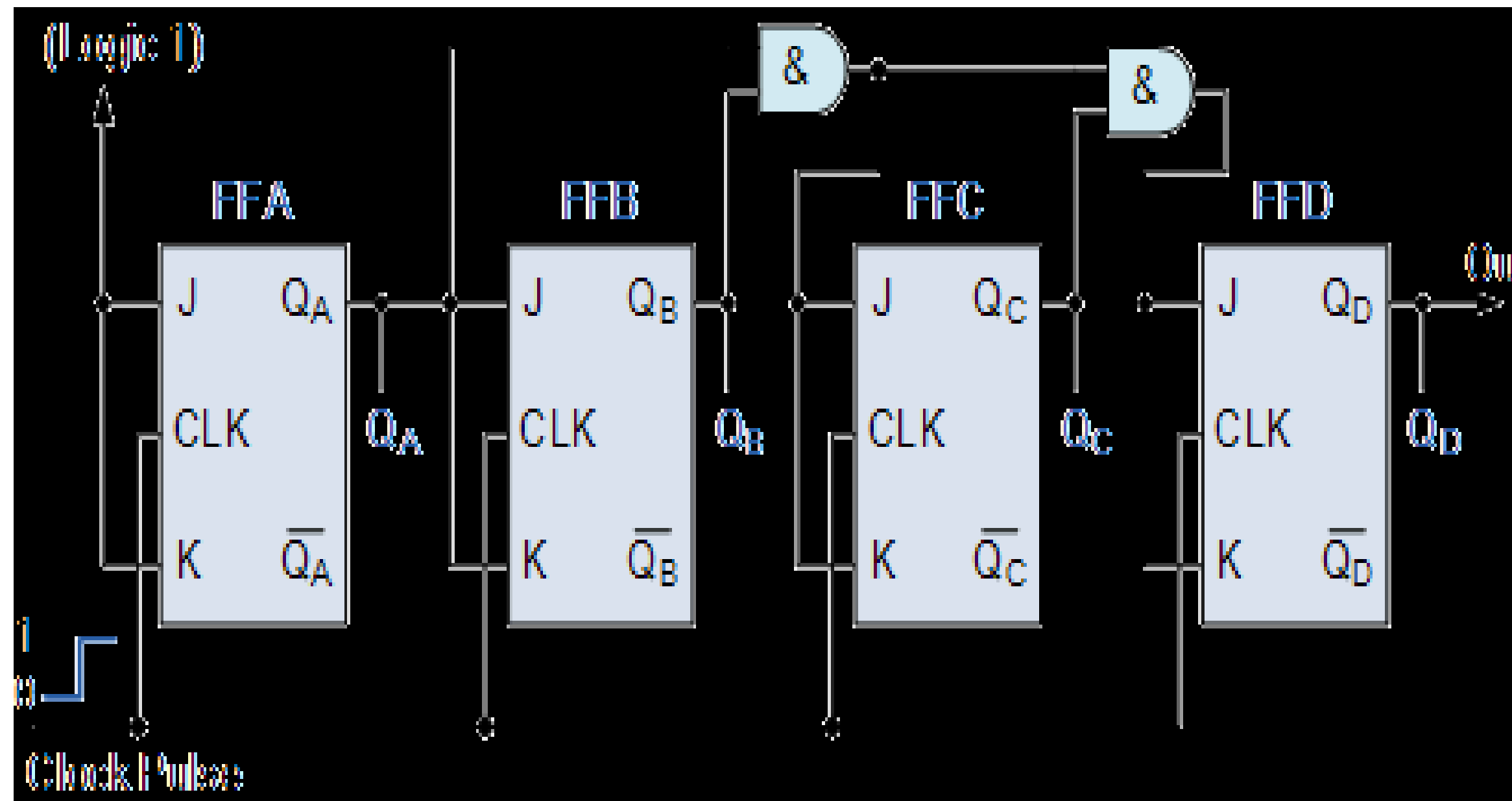
Synchronous Up Counter – 4 bit

➢ A **4-bit Synchronous up counter** start to count from 0 (0000 in binary) and increment or count upwards to 15 (1111 in binary) and then start new counting cycle by getting reset.

➢ Its operating frequency is much higher than the same range Asynchronous counter.

➢ There is **no propagation delay** in the synchronous counter just because all flip-flops or counter stage is in parallel clock source and the clock triggers all counters at the same time.

Binary 4-bit Synchronous Up Counter

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Binary 4-bit Synchronous Up Counter

➢ External clock pulses (pulses to be counted) are fed directly to each of the **J-K flip-flops** in the counter chain and that both the J and K inputs are all tied together in toggle mode.

➢ In the first flip-flop, flip-flop FFA (LSB) are they connected HIGH, logic "1" allowing the flip-flop to toggle on every clock pulse.

➢Then the synchronous counter follows a predetermined sequence of states in response to the common clock signal, advancing one state for each pulse.

➢The J and K inputs of flip-flop FFB are connected directly to the output Q_A of flip-flop FFA, but the J and K inputs of flip-flops FFC and FFD are driven from separate AND gates which are also supplied with signals from the input and output of the previous stage.
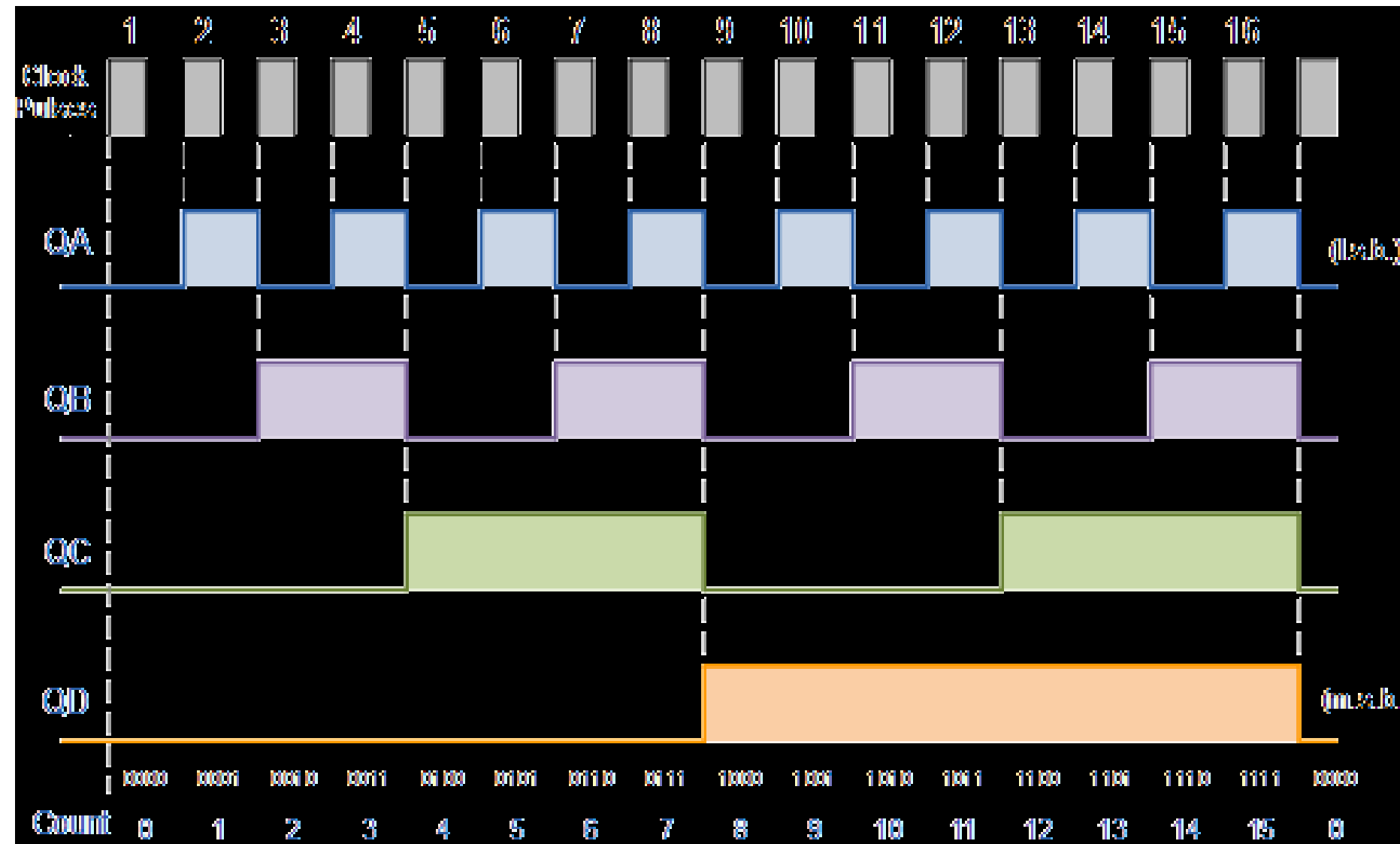
Binary 4-bit Synchronous Up Counter

➢ The additional AND gates generate the required logic for the JK inputs of the next stage.

➢ If we enable each JK flip-flop to toggle based on whether or not all preceding flip-flop outputs (Q) are "HIGH" we can obtain the same counting sequence as with the asynchronous circuit but without the ripple effect, since each flip-flop in this circuit will be clocked at exactly the same time.

➢ There is no inherent propagation delay in synchronous counters, because all the counter stages are triggered in parallel at the same time, the maximum operating frequency of this type of frequency counter is much higher than that for a similar asynchronous counter circuit.

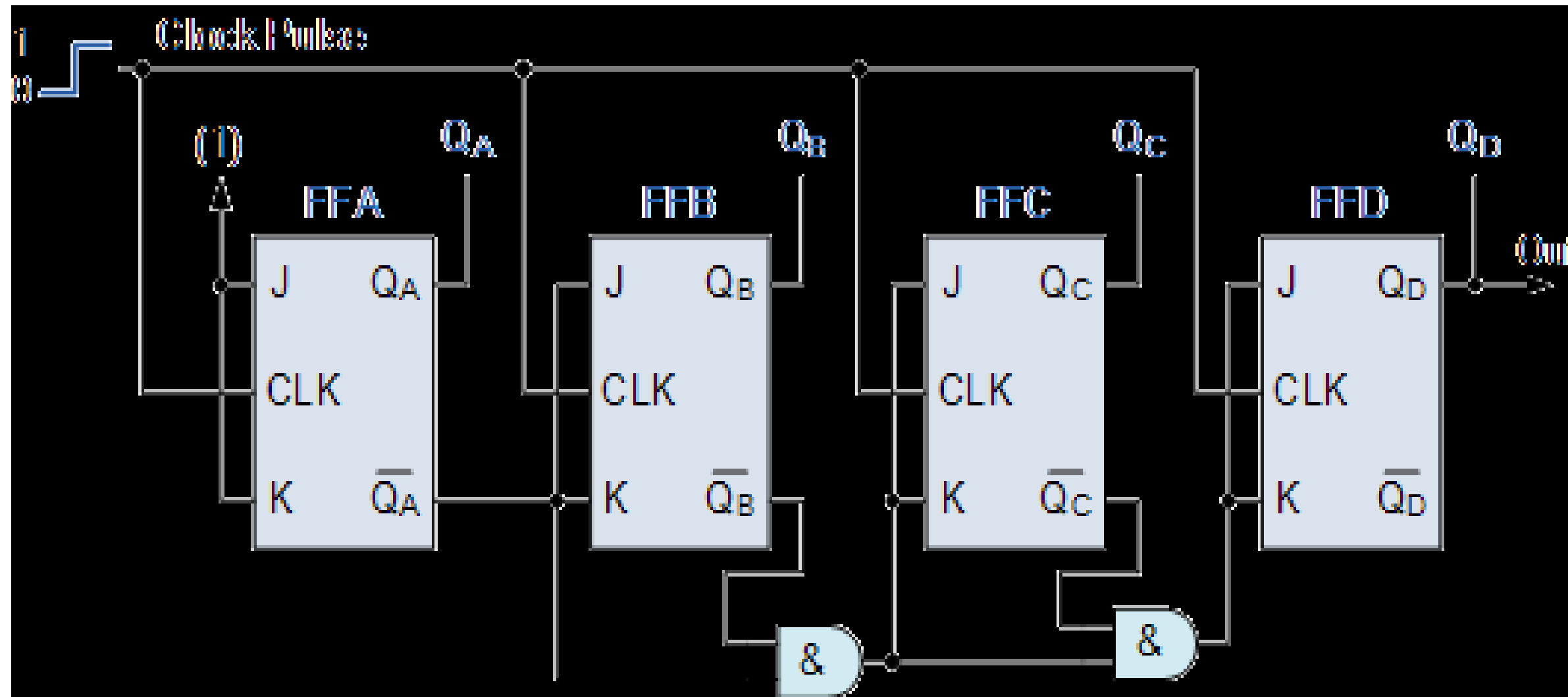# 4-bit Synchronous Counter Waveform Timing Diagram

4-bit Synchronous Up Counter

➢ Since,4-bit synchronous counter counts sequentially on every clock pulse the resulting outputs count upwards from 0 (0000) to 15 (1111) known as a **4-bit Synchronous Up Counter**.

➢A **4-bit Synchronous Down Counter can be designed** by connecting the AND gates to the Q output of the flip-flops as shown to produce a waveform timing diagram the reverse of the above.

4-bit Synchronous Down Counter

4-bit Synchronous Down Counter

➢ An 4-bit Synchronous Down Counter can be constructed by connecting the AND gates to the Q output of the flip-flops as shown to produce a waveform timing diagram the reverse .

➢ Here the counter starts with all of its outputs HIGH (1111) and it counts down on the application of each clock pulse to zero, (0000) before repeating again.

4-bit Synchronous Down Counter

➢As synchronous counters are formed by connecting flip-flops together and any number of flip-flops can be connected or "cascaded" together to form a "divide-by-n" binary counter.

➢The modulo's or "MOD" number still applies as it does for asynchronous counters so a Decade counter or BCD counter with counts from 0 to 2^n-1 can be built along with truncated sequences.

➢ We need to increase the MOD count of an up or down synchronous counter is an additional flip-flop and AND gate across it.

ASSESSMENTS

1. How many natural states will there be in a 4-bit ripple counter?
   a) 4
   b) 8
   c) **16**
   d) 32
2. A ripple counter's speed is limited by the propagation delay of _____
   a) **Each flip-flop**
   b) All flip-flops and gates
   c) The flip-flops only with gates
   d) Only circuit gates.
3. Internal propagation delay of asynchronous counter is removed by _____
   a) Ripple counter
   b) Ring counter
   c) Modulus counter
   d) Synchronous counter
4. An asynchronous 4-bit binary down counter changes from count 2 to count 3. How many transitional states are required?
   a) 1
   b) 2
   c) 8
   d) **15**
5. A ripple counter's speed is limited by the propagation delay of _____
   a) **Each flip-flop**
   b) All flip-flops and gates
   c) The flip-flops only with gates
   d) Only circuit gates

THANK YOU

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