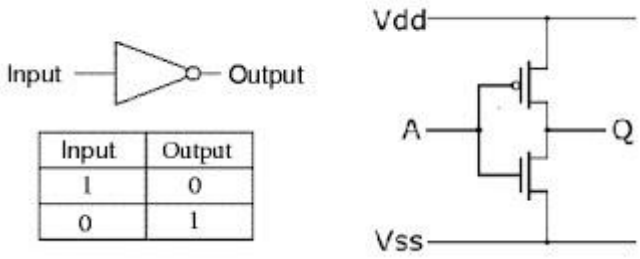
COMPLEMENTARY METAL–OXIDE–SEMICONDUCTOR

The term "CMOS" stands for "complementary metal–oxide–semiconductor". CMOS is a type of MOSFET, where its fabrication process uses complementary & symmetrical P-type & N-type MOSFET pairs for logic functions. The main CMOS devices characteristics are consumption of low static power & high noise immunity.

The inverter is accepted universally as the basic logic gate while performing a Boolean operation on a single i/p variable. A basic inverter circuit is used to accomplish a logic variable by complementing from A to A'. So, a **CMOS inverter** is a very simple circuit, designed with two opposite-polarity MOSFETs within a complementary way.

CMOS Inverter

CMOS inverter definition is a device that is used to generate logic functions is known as CMOS inverter and is the essential component in all integrated circuits. A CMOS inverter is a FET (field effect transistor), composed of a metal gate that lies on top of oxygen's insulating layer on top of a semiconductor. These inverters are used in most electronic devices which are accountable for generating data n small circuits.

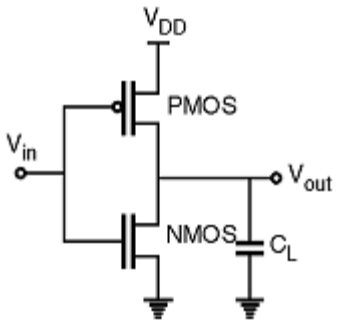


Input	Output
1	0
0	1

CMOS Inverter Symbol & Truth Table

CMOS Inverter Schematic Diagram

The logic element like an inverter reverses the applied input signal. In digital logic circuits, binary arithmetic & switching or logic function's mathematical manipulation are best performed through the symbols 0 & 1. The CMOS inverter truth table is shown above. If the input logic is zero (0) then the output will be high (1) whereas, if the input logic is one (1), then the output will be low (0).



CMOS Inverter Circuit

The general CMOS inverter structure is the combination of both the PMOS & NMOS transistors where the pMOS is arranged at the top & nMOS is arranged at the bottom.

The connection of both the PMOS & NMOS transistors in the CMOS inverter can be done like this. The NMOS transistor is connected at the drain (D) & gate (G) terminals, a voltage supply (VDD) is connected at the source terminal of PMOS & a GND terminal is connected at the source terminal of NMOS. Input voltage (Vin) is connected to both the gate terminals of transistors & output voltage (Vout) is connected to the drain (D) terminals of the transistor.

CMOS Inverter Operation & Working

The working of CMOS inverter is the same as other types of FETs except depends on an oxygen layer to divide electrons within the gate & semiconductor. They are designed with a power supply, input voltage terminal, output voltage, gate, drain, and PMOS & NMOS transistors which are connected to the gate & the drain terminals.

When the low input voltage is given to the CMOS inverter, then the PMOS transistor is switched ON whereas the NMOS transistor will switch OFF by allowing the flow of electrons throughout the gate terminal & generating high logic output voltage.

Similarly, when the high input voltage is given to the CMOS inverter then, the PMOS transistor is switched OFF whereas the NMOS transistor will be switched ON avoiding as many electrons from attaining the output voltage & generating low logic output voltage.

Thus, direct current supplies from the supply voltage (VDD) to the output voltage (Vout) & the load capacitor (CL) can be charged and shows that Vout = VDD. As a result, the above circuit works like an inverter.