16EC303-VLSI DESIGN

2 MARKS

UNIT III SEQUENTIAL LOGIC CIRCUITS

1. What is metastability and list the steps to prevent it?

Metastability is an unknown state it is neither zero nor one. Metastability happens for the design systems violating setup or hold time requirements. Setup time is a requirement that the data has to be stable before the clock edge and hold time is a requirement that the data has to be stable after the clock edge. The potential violation of the setup and hold violation can happen when the data is purely asynchronous and clocked synchronously.

Steps to prevent metastability:

1. Using proper synchronizers (two stage or three stage), as soon as the data is coming from the asynchronous domain. Using synchronizers, recovers from the metastable event.
2. Use synchronizers between cross-clocking domains to reduce the possibility from metastability.
3. Using faster flip flops (which has narrower metastable window).

2. Define local-skew, global-skew, and useful-skew.

Local skew:

The difference between the clock reaching at the launching flip-flop vs the clock reaching the destination flip-flop of a timing-path.

Global skew:

The difference between the earliest reaching flip-flop and latest reaching flip-flop for a same clock-domain.

Useful skew:

Useful skew is a concept of delaying the capturing flip-flop clock path, this approach helps in meeting setup requirement within the launch and capture timing path. But the hold requirement has to be met for the design.

3. What is meant by virtual clock definition and why it is needed?

Virtual clock is mainly used to model the I/O timing specification. Based on what clock the output/input pads are passing the data.

4. What is the difference between mealy and moore state machines?

In the mealy state machine we can calculate the next state and output both from the input and state. But in the moore state machine we can calculate only next state but not output from the input and state and the output is issued according to next state.

5. What is the difference between latches and flip-flops based designs?

Latches are level-sensitive and flip-flops are edge sensitive. Latch based design and flop based design is that latch allows time borrowing which a tradition flip-flop does not: That makes latch based design more efficient. But at the same time, latch based design is more complicated and has more issues in min timing (races).

6. What are the classifications of CMOS circuit families?
   Static CMOS circuits.
   Dynamic CMOS circuits.
   Ratioed circuits. Pass-
   transistor circuits.

7. What are the characteristics of Static CMOS design?

   A static CMOS circuit is a combination of two networks, one is pull-up network (PUN) and the other is pull-down network (PDN) in which at every point in time, each gate output is connected to either VDD or VSS via pull-up or pull down network.

8. List the important properties of Static CMOS design.
   1. At any instant of time, the output of the gate is directly connected to VDD and VSS.
   2. The function of the PUN is providing a connection between the output and VDD.
   3. The function of the PDN is providing a connection between the output and VSS.
   4. Both PDN and PUN are constructed in mutually exclusive way such that one and only one of the networks is conduct in steady state. That is, the output node is always a low-impedance node in steady state.

9. What is Dynamic CMOS logic?

   Dynamic circuits rely on the temporary storage of signal values on the capacitance of high impedance node. It requires only N+2 transistors. It takes a sequence of precharge and conditional evaluation phases to realize the logic functions.

10. What are the properties of dynamic logic?
    1. Logic function is implemented by pull-down network only.
    2. Full swing outputs (V_{OL}= GND and V_{OH} = VDD).
    3. Non-ratioed.
    4. Faster switching speeds.
    5. Needs a precharge clock.

11. What are the disadvantages of dynamic CMOS technology?

    A fundamental difficulty with dynamic circuits is a loss of noise immunity and a serious timing restriction on the inputs of the gate. Violate monotonicity during evaluation phase.

12. What is CMOS Domino logic?

    A static CMOS inverter placed between dynamic gates which eliminate the monotonicity problem in dynamic circuits are called CMOS Domino logic.

13. What is called static and dynamic sequencing element?

    A sequencing element with static storage employs some sort of feedback to retain its output value indefinitely. A sequencing element with dynamic storage generally maintains its value as charge on a capacitor that will leak away if not refreshed for a long period of time.

14. What is clock skew?

    In reality clocks have some uncertainty in their arrival times that can cut into the time available for useful computation. It is called clock skew.

15. What are synchronizers?

Synchronizers are used to reduce metastability. The synchronizers ensure synchronization between asynchronous input and synchronous system.

16. Difference between latches and Flip-Flop.

S.No	Latch	Flip-Flop
1.	A Latch is Level Sensitive	A flip-flop is edge triggered.
2.	A latch stores when the clock level is low and is transparent when the level is high.	A flip-flop stores when the clock rises and is mostly never transparent.

17. Define Pipelining.

Pipelining is a popular design technique often used to accelerate the operation of the data path in digital processors. The major advantages of pipelining are to reduce glitch in complex logic networks and getting lower energy due to operand isolation.

18. How the limitations of a ROM based realization is overcome in a PLA based realization. In a ROM, the encoder part is only programmable and use of ROMs to realize Boolean functions is wasteful in many situations because there is no cross-connect for a significant part. This wastage can be overcome by using Programmable Logic Array (PLA), which requires much lesser chip area.

19. Define Latch/flip-flop clock-to-Q propagation delay.

t_{PLH}: 50% triggering edge point of the clock pulse to 50% transition of the output from low to high.

t_{PHL}: 50% triggering edge of the clock pulse to the high to low transition of the output.

20. Define Latch/flip-flop clock-to-Q contamination delay.

Output signal start to change after its input change and settles to the final value within propagation delay.

21. What is static 0 hazard?

Output goes momentarily 1 when it should remain at 0 is called static 0 hazard.

22. What is dynamic hazard?

Output changes 3 or more times when it changes from 1 to 0 or 0 to 1

23. What is non critical race?

Final stable state does not depend on the order in which the state variable changes then that race is called non critical race and it is not harmful

24. What is critical race?

Final stable state depends on the order in which the state variable changes then that race condition is called critical race and it is harmful.

25. Define propagation delay and contamination delay?

Propagation delay: The amount of time needed for a change in a logic input to result in a

permanent change at an output that is the combinational logic will not show any further output changes in response to an input change.
Contamination delay: The amount of time needed for a change in a logic input to result in an initial change at an output, that is the combinational logic is guaranteed not to show any output change in response to an input change before fed time units have passed.

26. Define Setup time and Hold time.

Setup time (t_{setup}): The amount of time before the clock edge that data input D must be stable the rising clock edge arrives.

Hold time (t_{hold}): This indicates the amount of time after the clock edge, the data input D must be held stable in order for Flip Flop to latch the correct value. Hold time is always measured from the rising clock edge to a point after the clock edge.

27. Differentiate DRAMs from SRAMs.

Both SRAMs and DRAMs are volatile in nature, ie. Information is lost if power line is removed. However SRAMs provide high switching speed, good noise margin but require large chip area than DRAMs.

28. Explain the read and write operations for a one transistor DRAM cell.

A significant improvement in the DRAM evolution was to realize 1-T DRAM cell. One additional capacitor is explicitly fabricated for storage purpose. To store '1', it is charged and to store '0' it is discharged to '0' volt. Read operation is destructive. Sense amplifier is needed for reading. Read operation is followed by restoration operation.