Reg.No:							

SNS College of Technology, Coimbatore-35.
(Autonomous)
B.E/B.Tech- Internal Assessment -I
Academic Year 2022-2023(Odd)
Fifth Semester
Electronics and Communication Engineering
19ECB302 – VLSI Design

B

Time: $1^{1/2}$ Hours **Maximum Marks: 50**

Answer All Questions

				CO	Blooms
	PART - A (5 x 2 = 10 Marks)			**CO**	**Blooms**
1	List the steps involved in manufacturing of CMOS IC fabrication.			CO1	REM
2	What are the two types of CMOS layout design rules?			CO1	UND
3	Differentiate between Threshold Voltage and Body Effect.			CO1	ANA
4	Define Drain punch through condition in CMOS circuits.			CO2	REM
5	Recall the advantages of Transmission Gate logic			CO2	REM
	PART – B (2*13 = 26 Marks)				
				CO	**Blooms**
6.	(a)	Describe mask levels for the CMOS Fabrication P-well process with necessary diagrams.	14	CO1	UND
		(or)			
	(b)	Build the MOS C-V Characteristics with its neat diagrams and explanation.	14	CO1	APP
7	(a)	Analyze pass transistor and Transmission gates with neat sketches.	14	CO2	ANA
		(or)			
	(b)	Develop any two examples of combinational logic with its circuit diagrams	14	CO2	APP
		PART – C (1*14 = 14 Marks)		**CO**	**Blooms**
8	(a)	Survey the concept of Twin Tub process Logic with relevant diagrams	14	CO1	ANA
		(or)			
	(b)	Apply the different mask levels for drawing stick diagram of **CMOS NAND** gate and **a.b +c** with its circuit diagram.	14	CO1	APP

CO-Course Outcomes, **REM**-Remembering**, UND**-Understanding, **APP-**Applying, **ANA**-Analyzing

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