SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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DEPARTMENT OF MECHATRONICS ENGINEERING

19MCT201 - DESIGN OF DIGITAL CIRCUITS

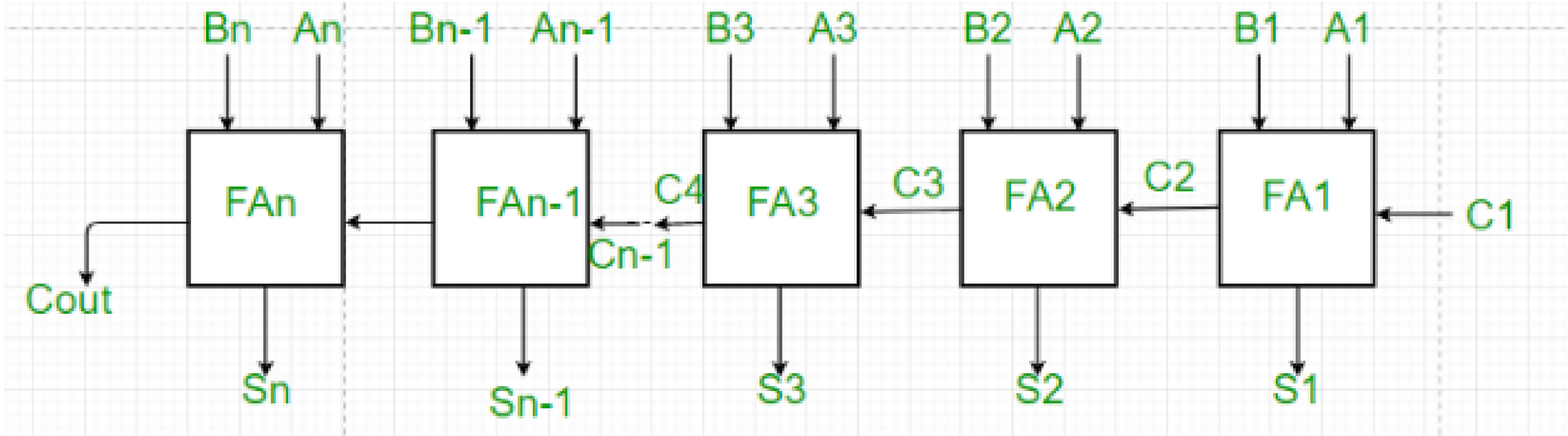
II YEAR - III SEM

UNIT 2 – COMBINATIONAL CIRCUITS

TOPIC 2 –Parallel Adder

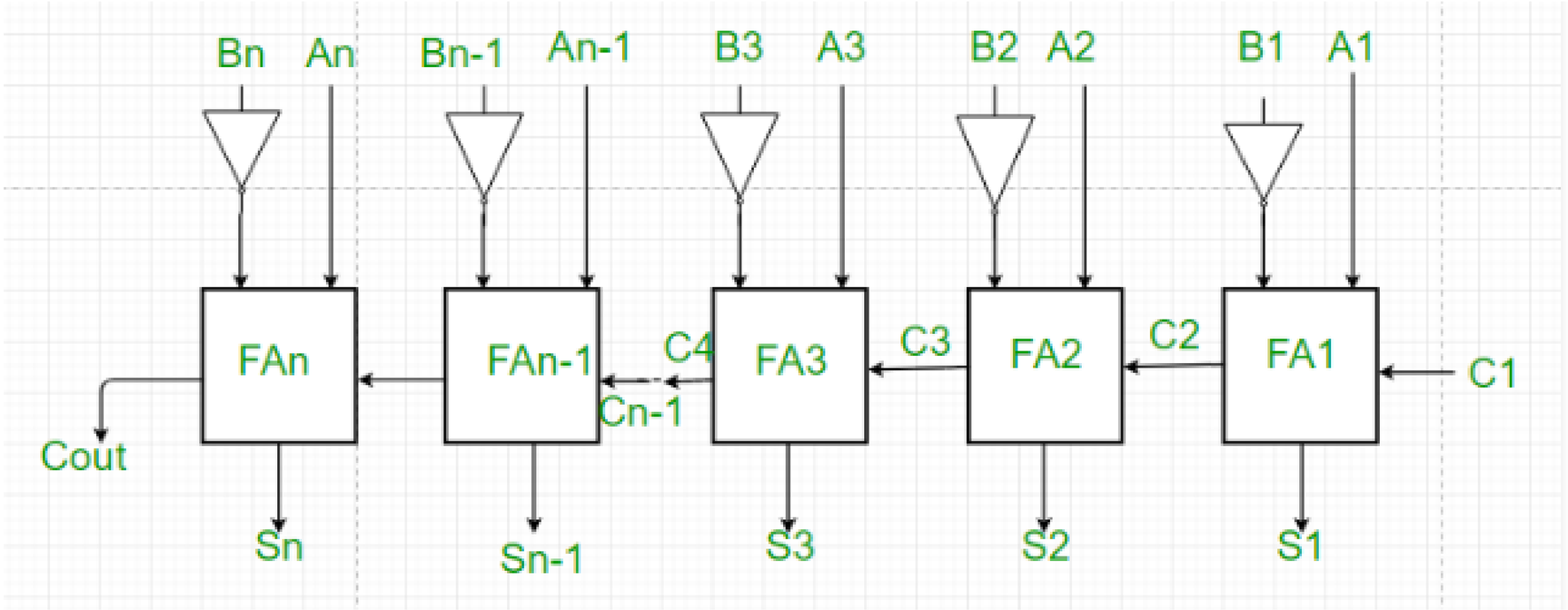
Parallel binary adder

- ✓A single full adder performs the addition of two one bit numbers and an input carry.
- ✓Parallel Adder for sum of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel.
- ✓It consists of full adders connected in a chain where the output carry from each full adder is connected to the carry input of the next higher order full adder in the chain.
- ✓ A n bit parallel adder requires n full adders to perform the operation.
- ✓So for the two-bit number, two adders are needed while for four bit number, four adders are needed and so on.

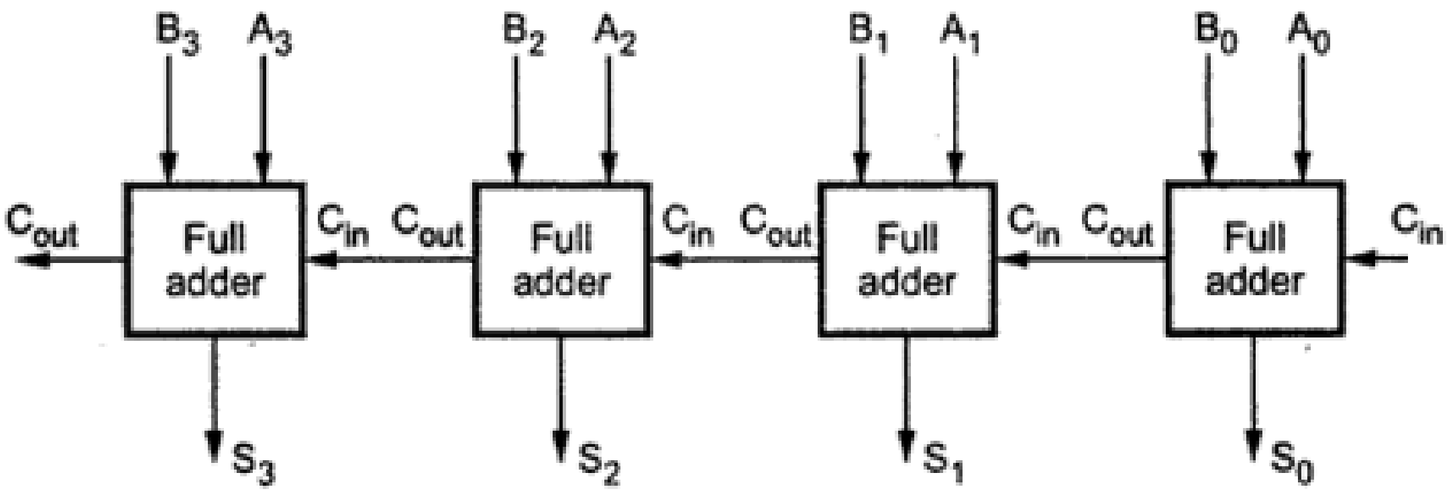


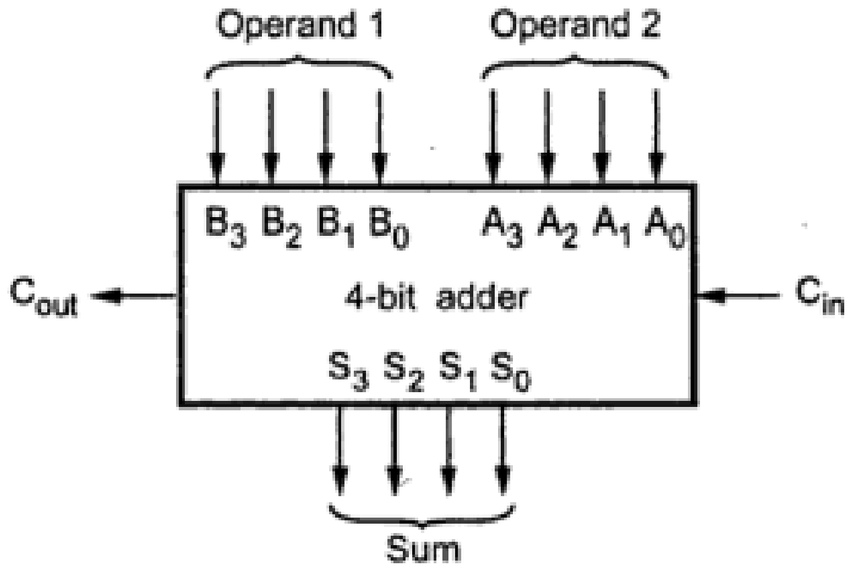
Parallel binary Subtractor

- ✓A Parallel Subtractor is a digital circuit capable of finding the arithmetic difference of two binary numbers that is greater than one bit in length by operating on corresponding pairs of bits in parallel.
- ✓The parallel subtractor can be designed in several ways including combination of half and full subtractors, all full subtractors or all full adders with subtrahend complement input.

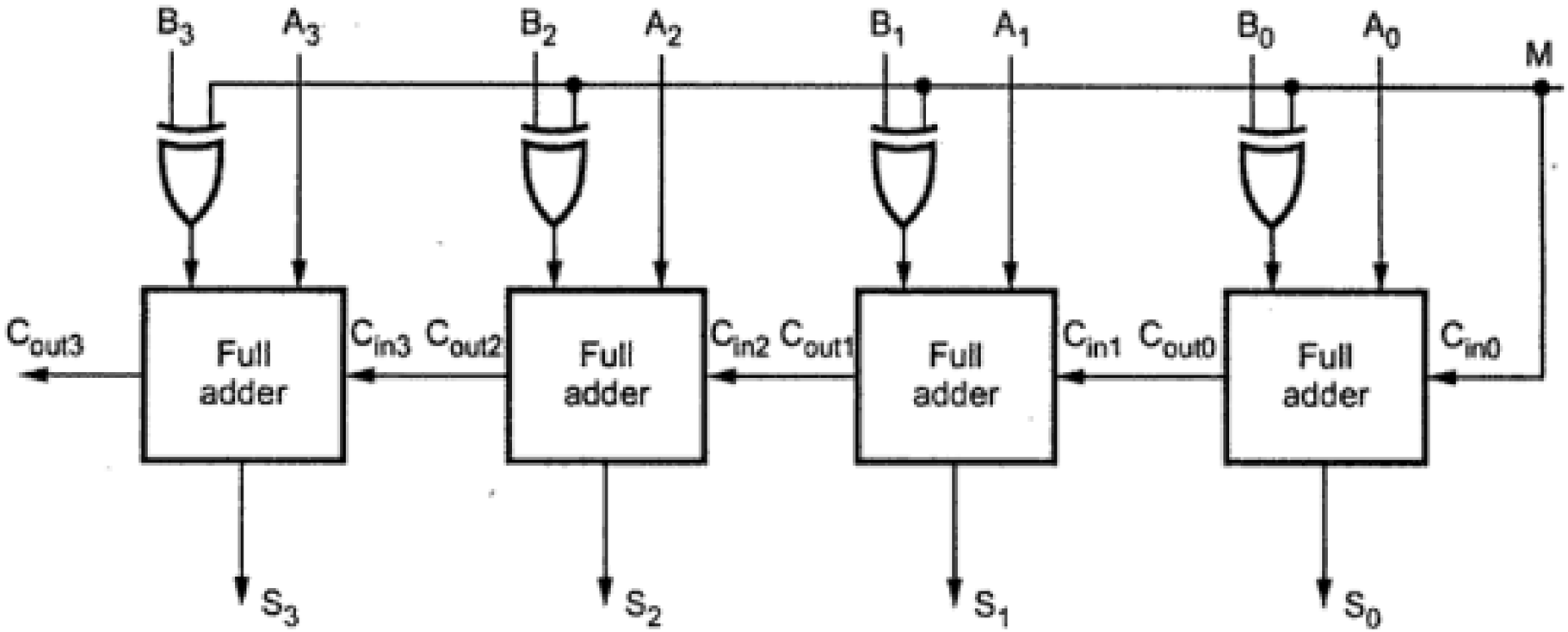


Design a 4-bit Parallel adder





Adder / Subtractor

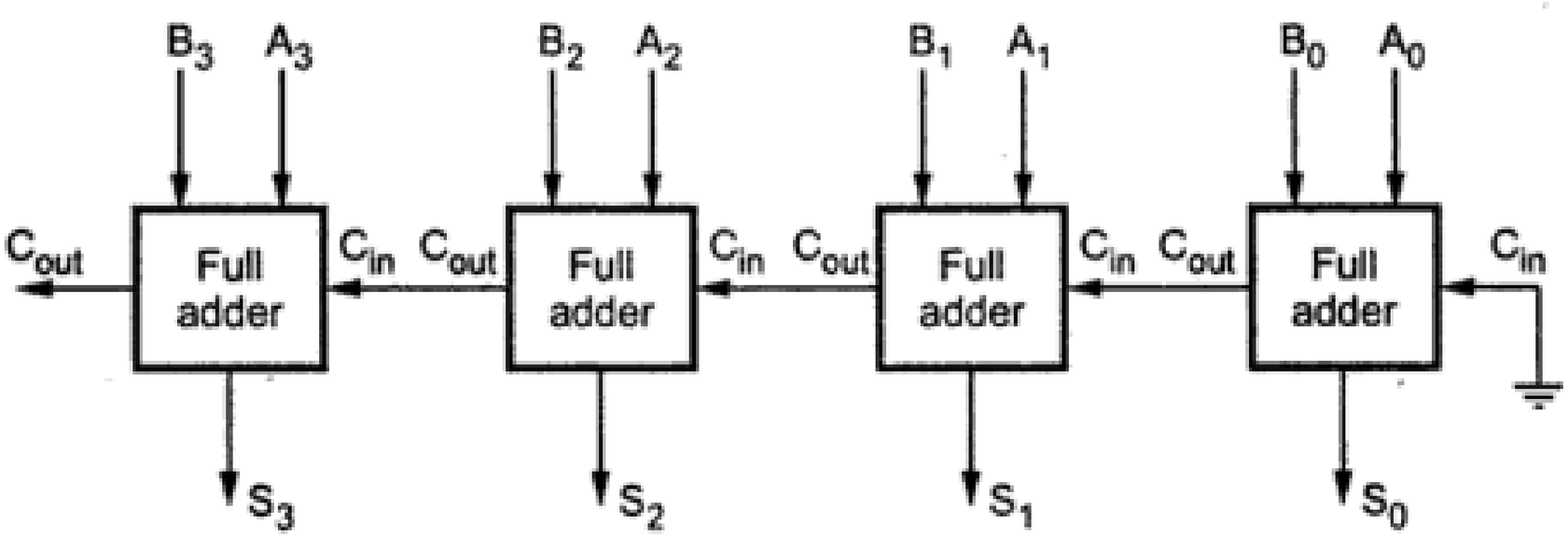


4-bit adder/subtractor

Carry Look Ahead Adder

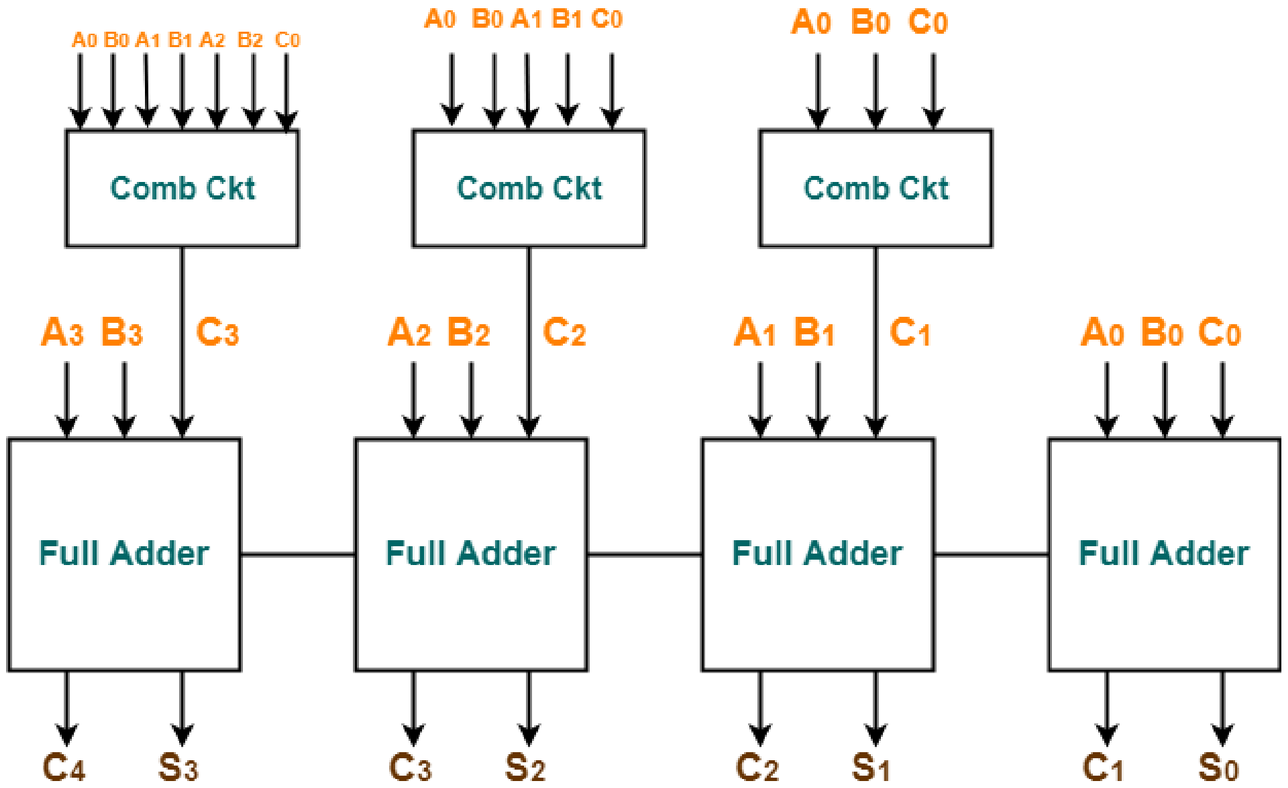
In a parallel adder circuit, the carry output of each full adder stage is connected to the carry input of the next higher-order stage, hence it is also called as **ripple carry type adder.**

In such adder circuits, it is not possible to produce the sum and carry outputs of any stage until the input carry occurs. So there will be a considerable time delay in the addition process , which is known as **, carry propagation delay**.



$$\begin{array}{r} 0\,1\,0\,1 \\ +\ 0\,0\,1\,1 \\ \hline 1\,0\,0\,0 \end{array}$$

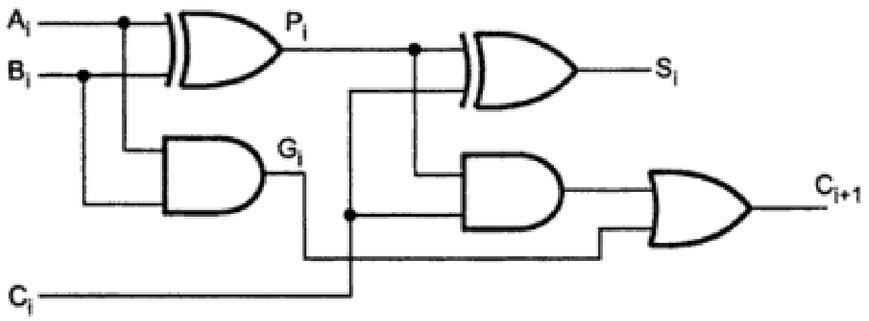
Carry Look Ahead Adder



Carry Look Ahead Adder Logic Diagram

$$\begin{array}{r} 0\,1\,0\,1 \\ +\;\; 0\,0\,1\,1 \\ \hline 1\,0\,0\,0 \end{array}$$

Look Ahead Adder



carry propagate. $P_i = A_i \oplus B_i$

carry generate $G_i = A_i B_i$

The output sum and carry can be expressed as

$$S_i = P_i \oplus C_i$$

$$C_{i+1} = G_i + P_i C_i$$

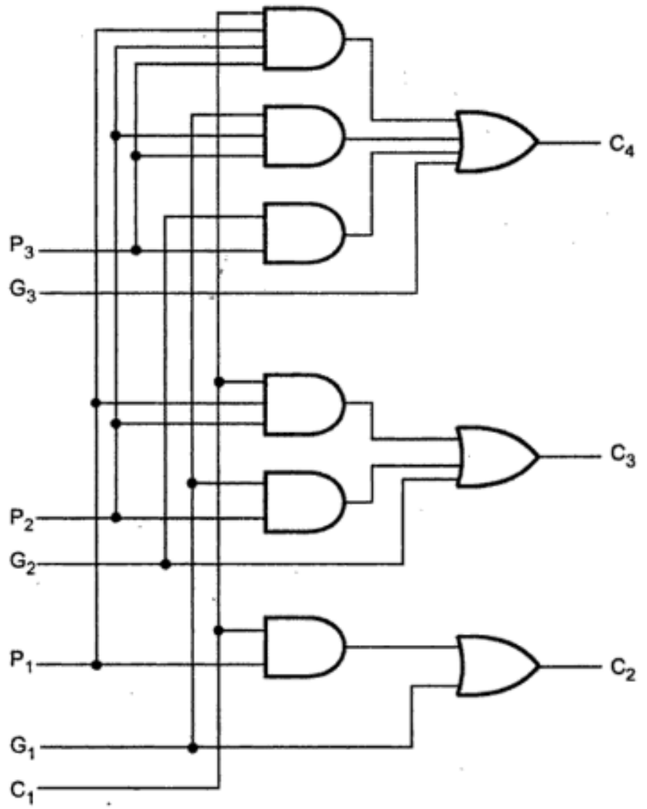
$$C_2 = G_1 + P_1 C_1$$

$$C_3 = G_2 + P_2 C_2 = G_2 + P_2 (G_1 + P_1 C_1)$$

$$= G_2 + P_2 G_1 + P_2 P_1 C_1$$

$$C_4 = G_3 + P_3 C_3 = G_3 + P_3 (G_2 + P_2 G_1 + P_2 P_1 C_1)$$

$$= G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 C_1$$



BCD adder

each BCD digit is represented as a 4-bit binary number.

5	2	6
↓	↓	↓
0 1 0 1	0 0 1 0	0 1 1 0

The addition of two BCD numbers can be best understood by considering the three cases that occur when two BCD digits are added.

1. Add two BCD numbers using ordinary binary addition.
2. If four-bit sum is equal to or less than 9, no correction is needed. The sum is in proper BCD form.
3. If the four-bit sum is greater than 9 or if a carry is generated from the four-bit sum, the sum is invalid.
4. To correct the invalid sum, add 0110_2 to the four-bit sum. If a carry results from this addition, add it to the next higher-order BCD digit.

Inputs				Output
S_3	S_2	S_1	S_0	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

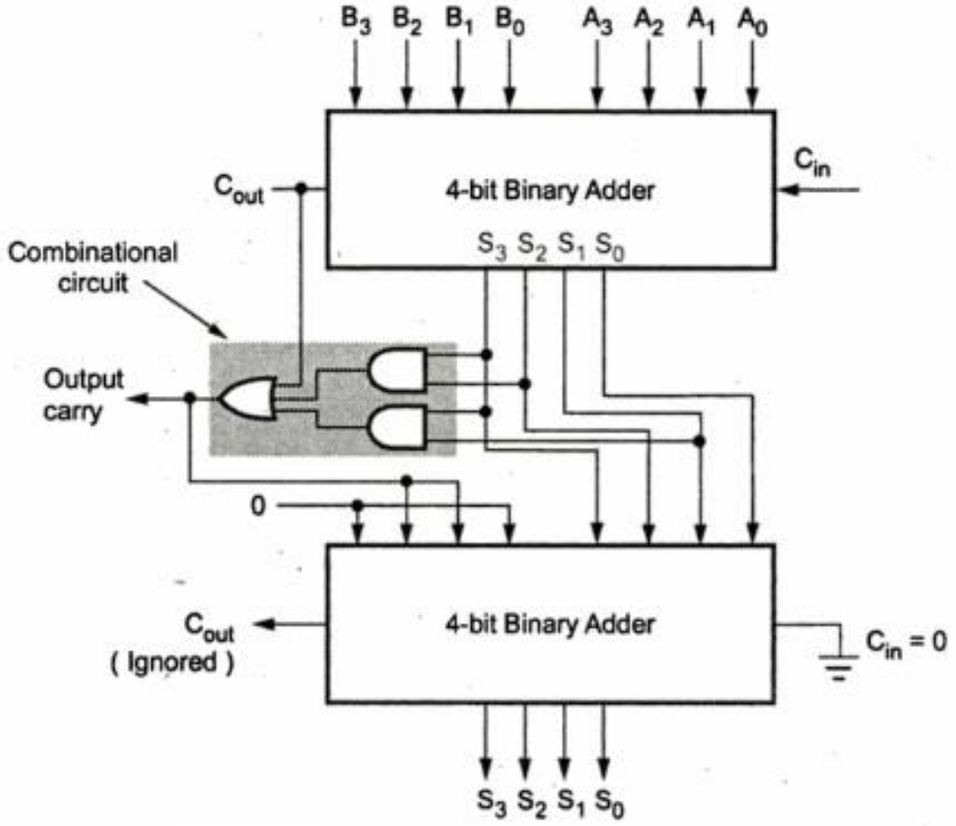
BCD adder

Thus to implement BCD adder we require :

- 4-bit binary adder for initial addition.
- Logic circuit to detect sum greater than 9 and
- One more 4-bit adder to add 0110_2 in the sum if sum is greater than 9 o is 1.

S_3S_2 \ S_1S_0	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	0	0	1	1

$$Y = S_3S_2 + S_3S_1$$



Block diagram of BCD adder

Binary Multiplier

A binary multiplier is a combinational logic circuit used **in digital systems to perform the multiplication of two binary numbers**. In multiplication process, the number which is to be multiplied by the other number is called as multiplicand and the number multiplied is called as multiplier.

Types:

1. Partial product addition and shifting
2. Parallel multipliers

$0 \times 0 = 0$

$0 \times 1 = 0$

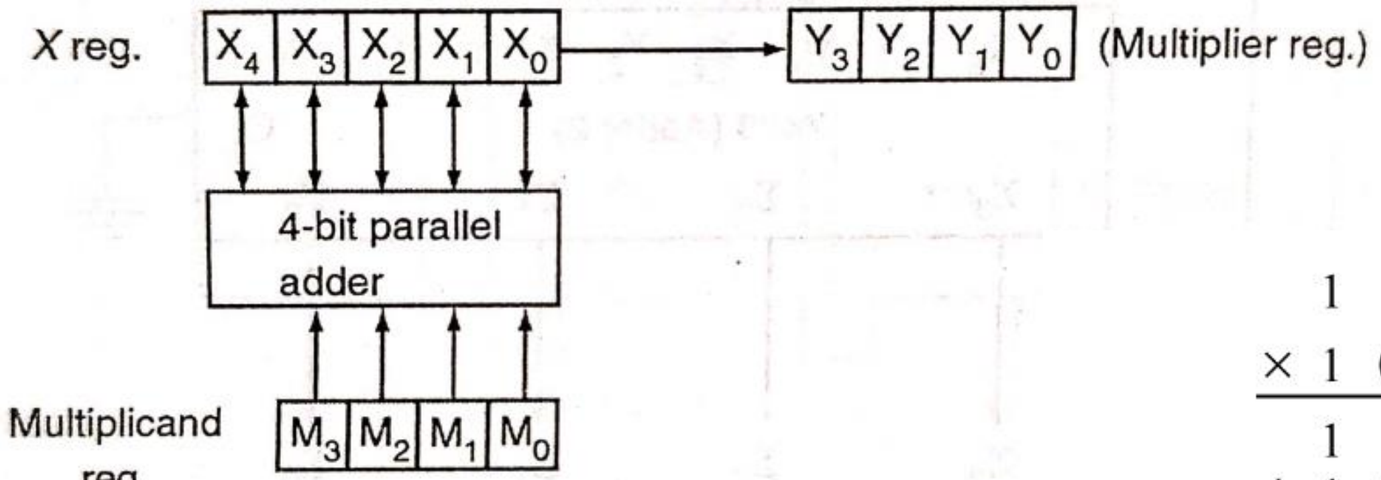
$1 \times 0 = 0$

$1 \times 1 = 1$

```
      2   8          1 1 0          6
*     1   3    *     1 1 0 1   *    1 3
-------------    -----------    -------
      6+2 4          1 1 0        1 8
2     8            0 0 0          6
-------------    1 1 0          -------
3     6   4      1 1 0            7 8
               -----------
               1 0 0 1 1 1 0
```

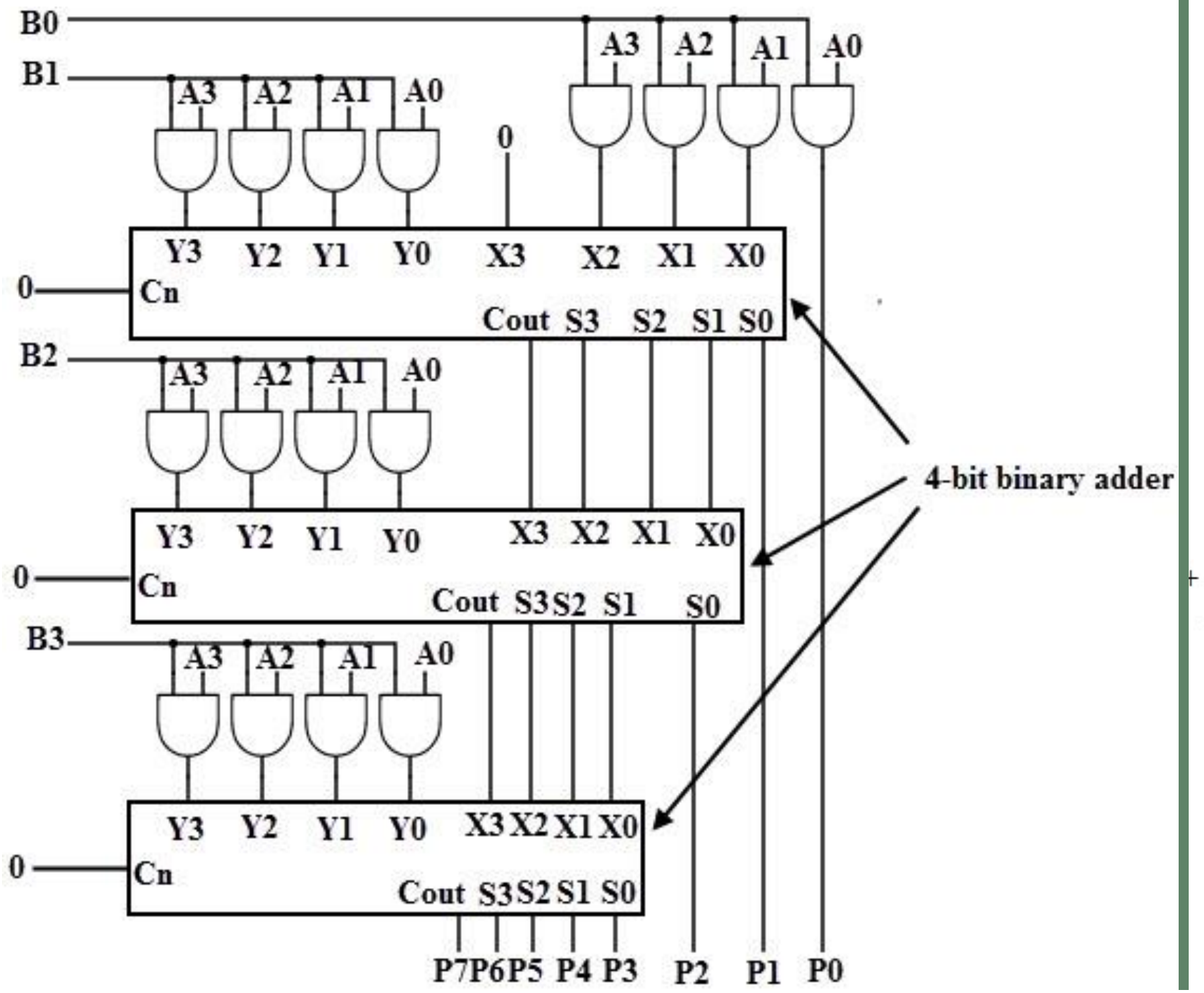
Partial Product and Shifting

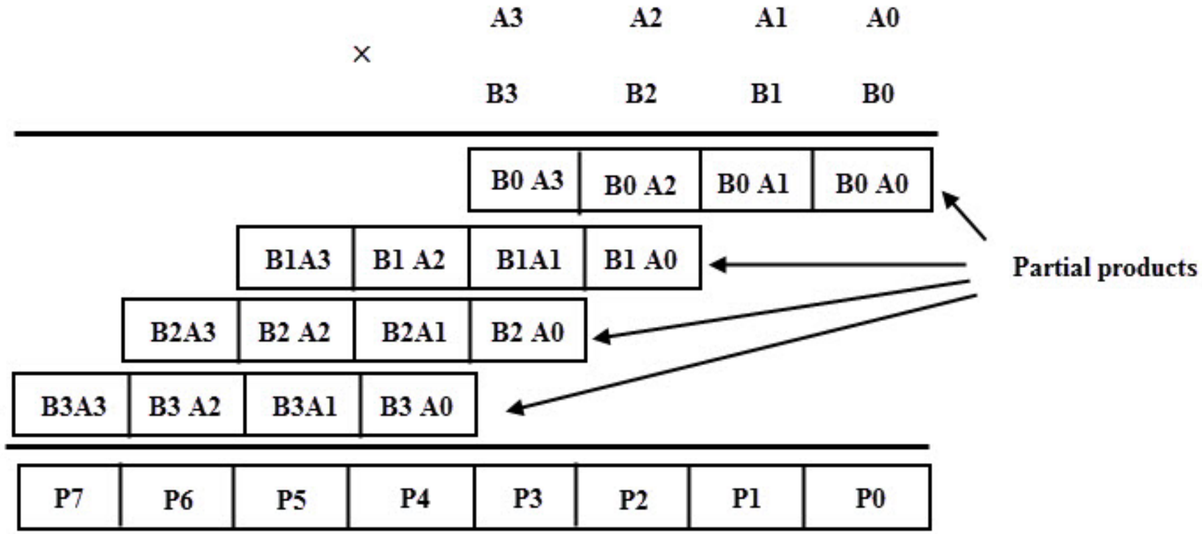
This manual multiplication approach can be implemented by using 4-bit adder, four registers (X, Y, C and M) and shift and control logic.



1 1 0 1	$(13)_{10}$	Multiplicand M
× 1 0 1 1	$(11)_{10}$	Multiplier Q
1 1 0 1		Partial products
1 1 0 1		
0 0 0 0		
1 1 0 1		
1 0 0 0 1 1 1 1	$(143)_{10}$	Product P

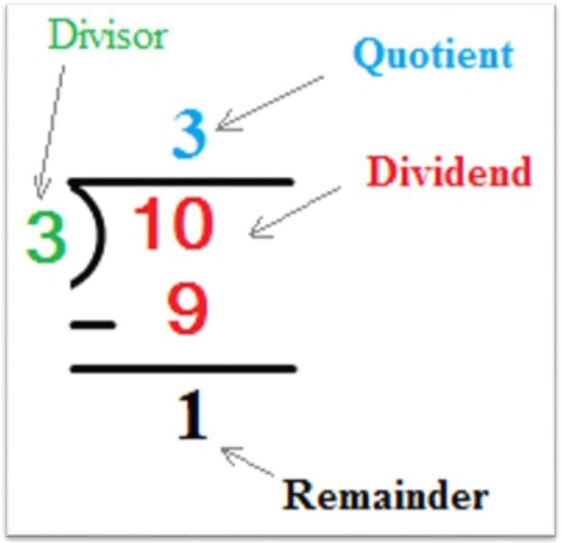
Parallel Multiplier





Binary Divider

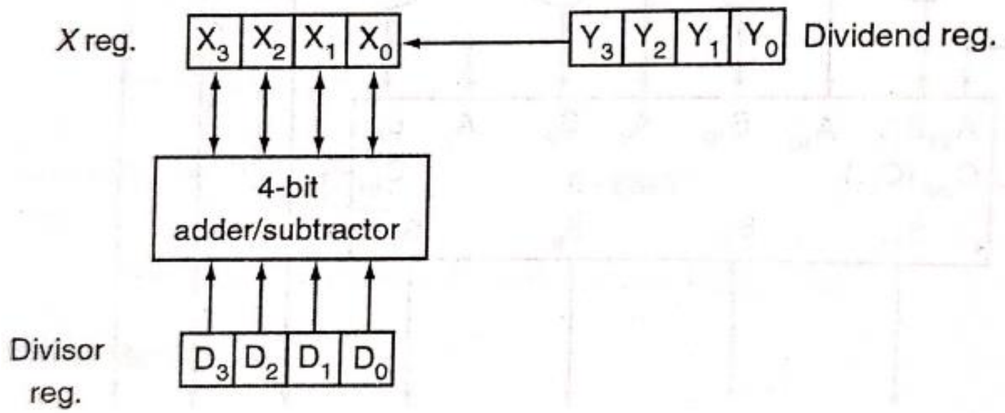
The binary division is one of the important operations of binary arithmetic. A binary number system or base-two is a counting technique that uses two digits: 0 and 1, and represents the number with the base 2.



Quotient		111	
Divisor	110	101010	Dividend
		-110	
		1001	
		-110	
		110	
		-110	
Remainder		0	

0 - 0 = 0
1 - 0 = 1
1 - 1 = 0
10 - 1 = 1

Binary Divider



		10011	Quotient (q=19)
Divisor (d=10)	1010	1100 0101	Dividend (z=197)
		1010	
The 1st subtraction			
$s^{(0)}$		0 0100 101	
The 2nd subtraction		0000	
$s^{(1)}$		0 01001 01	
The 3rd subtraction		0000	
$s^{(2)}$		00 10010 1	
The 4th subtraction		1010	
$s^{(3)}$		000 10001	
The 5th subtraction		1010	
$s^{(4)}$		0000 0111	Remainder (s=7)

References

- https://brilliant.org/wiki/de-morgans-laws/
- https://circuitglobe.com/demorgans-theorem.html
- https://www.electrical4u.com/