SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF MECHATRONICS ENGINEERING

19MCT201 - DESIGN OF DIGITAL CIRCUITS

II YEAR - III SEM

UNIT 1 – MINIMIZATION TECHNIQUES AND LOGIC GATES

TOPIC 1 –BOOLEAN POSTULATES AND LAWS

Meaning of this Symbol ?

UNIT I MINIMIZATION TECHNIQUES AND LOGIC GATES 9

Minimization Techniques: Boolean postulates and laws – De-Morgan‟s Theorem - Principle of Duality - Boolean expression - Minimization of Boolean expressions –- Minterm – Maxterm - Sum of Products (SOP) – Product of Sums (POS) – Karnaugh map Minimization – Don't care conditions – Quine - McCluskey method of minimization

Logic Gates: AND, OR, NOT, NAND, NOR, XOR and XNOR Implementations of Logic Functions using NAND–NOR . Simulation for Minimization & Logic Diagram

UNIT II COMBINATIONAL CIRCUITS 9

Design procedure – Half adder – Full Adder – Half subtractor – Full subtractor – Parallel binary adder, parallel binary Subtractor – Fast Adder - Carry Look Ahead adder – Serial Adder/Subtractor - BCD adder - Multiplexer/ Demultiplexer – decoder - encoder – parity checker – parity generators – code converters - Magnitude Comparator. Design of Combination circuits using simulation.

UNIT III SEQUENTIAL CIRCUITS 9

Latches, Edge triggered Flip flops SR, JK, T, D and Master slave – Characteristic table and equation, Application table, Synchronous counters, Design of synchronous counters, up/down counter, Modulo–n counter, Decade counters. Design of Sequential circuits using simulation

UNIT IV DESIGN OF SEQUENTIAL CIRCUITS 9

Register, shift registers, Universal shift register, Ring counters, Classification of sequential circuits: Moore and Mealy, Design of synchronous sequential circuits, state diagram, State table, State minimization, State assignment, Introduction to Hazards: Static, Dynamic

UNIT V DIGITAL LOGIC FAMILIES AND PLD 9

Memories: ROM, PROM, EEPROM, RAM, Programmable Logic Devices: Programmable Logic Array (PLA), Programmable Array Logic (PAL), Implementation of combinational logic using PROM, PLA and PAL, Digital logic families: TTL, ECL and CMOS. Design of Memory elements using simulation

Meaning of this Symbol ?

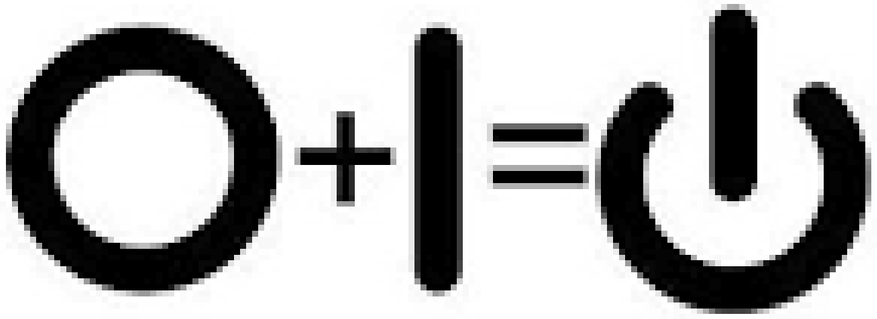
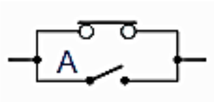
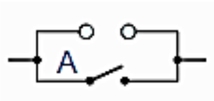
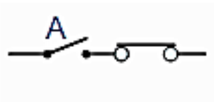
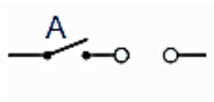
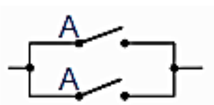
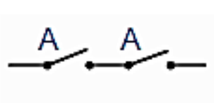


Image Courtesy: singularityhub.com

A switch contains 2 differenc symbols on it, do you noticed it ?

Rules of Boolean Algebra

Boolean Expression	Description	Equivalent Switching Circuit	Boolean Algebra Law or Rule
A + 1 = 1	A in parallel with closed = "CLOSED"		Annulment
A + 0 = A	A in parallel with open = "A"		Identity
A . 1 = A	A in series with closed = "A"		Identity
A . 0 = 0	A in series with open = "OPEN"		Annulment
A + A = A	A in parallel with A = "A"		Idempotent
A . A = A	A in series with A = "A"		Idempotent

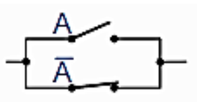
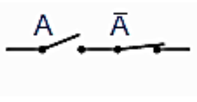
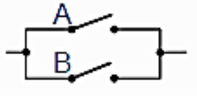
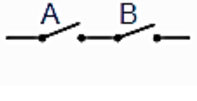
NOT $\overline{A}$ = A	NOT NOT A (double negative) = "A"		Double Negation
A + $\overline{A}$ = 1	A in parallel with NOT A = "CLOSED"		Complement
A . $\overline{A}$ = 0	A in series with NOT A = "OPEN"		Complement
A+B = B+A	A in parallel with B = B in parallel with A		Commutative
A.B = B.A	A in series with B = B in series with A		Commutative
$\overline{A+B}$ = $\overline{A}$.$\overline{B}$	invert and replace OR with AND		de Morgan's Theorem
$\overline{A.B}$ = $\overline{A}$+$\overline{B}$	invert and replace AND with OR		de Morgan's Theorem

Image Courtesy: softbankrobotics.com

Laws of Boolean Algebra

T1 : Commutative Law

(a) $A + B = B + A$

(b) $A\,B = B\,A$

T2 : Associate Law

(a) $(A + B) + C = A + (B + C)$

(b) $(A\,B)\,C = A\,(B\,C)$

T3 : Distributive Law

(a) $A\,(B + C) = A\,B + A\,C$

(b) $A + (B\,C) = (A + B)\,(A + C)$

T4 : Identity Law

(a) $A + A = A$

(b) $A\,A = A$

T5 :

(a) $AB + A\overline{B} = A$

(b) $(A+B)(A+\overline{B}) = A$

T6 : Redundance Law

(a) $A + A\,B = A$

(b) $A\,(A + B) = A$

T7 :

(a) $0 + A = A$

(b) $0\,A = 0$

T8 :

(a) $1 + A = 1$

(b) $1\,A = A$

T9 :

(a) $\overline{A} + A = 1$

(b) $\overline{A}\,A = 0$

T10 :

(a) $A + \overline{A}\,B = A + B$

(b) $A\,(\overline{A} + B) = A\,B$

T11 : De Morgan's Theorem

(a) $\overline{(A + B)} = \overline{A}\ \overline{B}$

(b) $\overline{(A\,B)} = \overline{A} + \overline{B}$

Advantage of Minimized Boolean Expression

Where
A = 1
A’ = 0

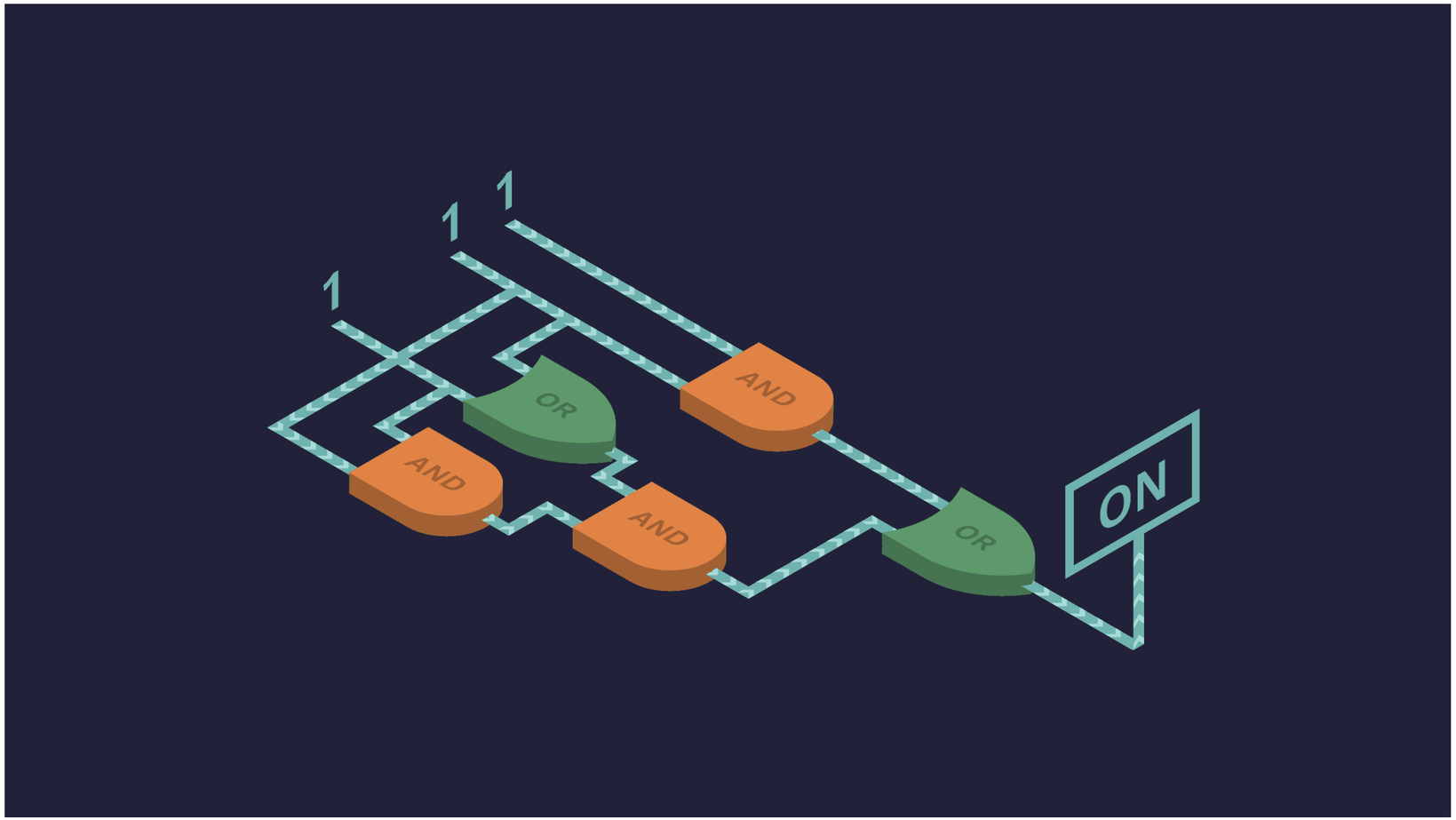


Image Courtesy: www.electrical4u.com

De Morgan's Law

$$(A+B)' = A'.B'$$

$$(A+B)' = A'.B'$$

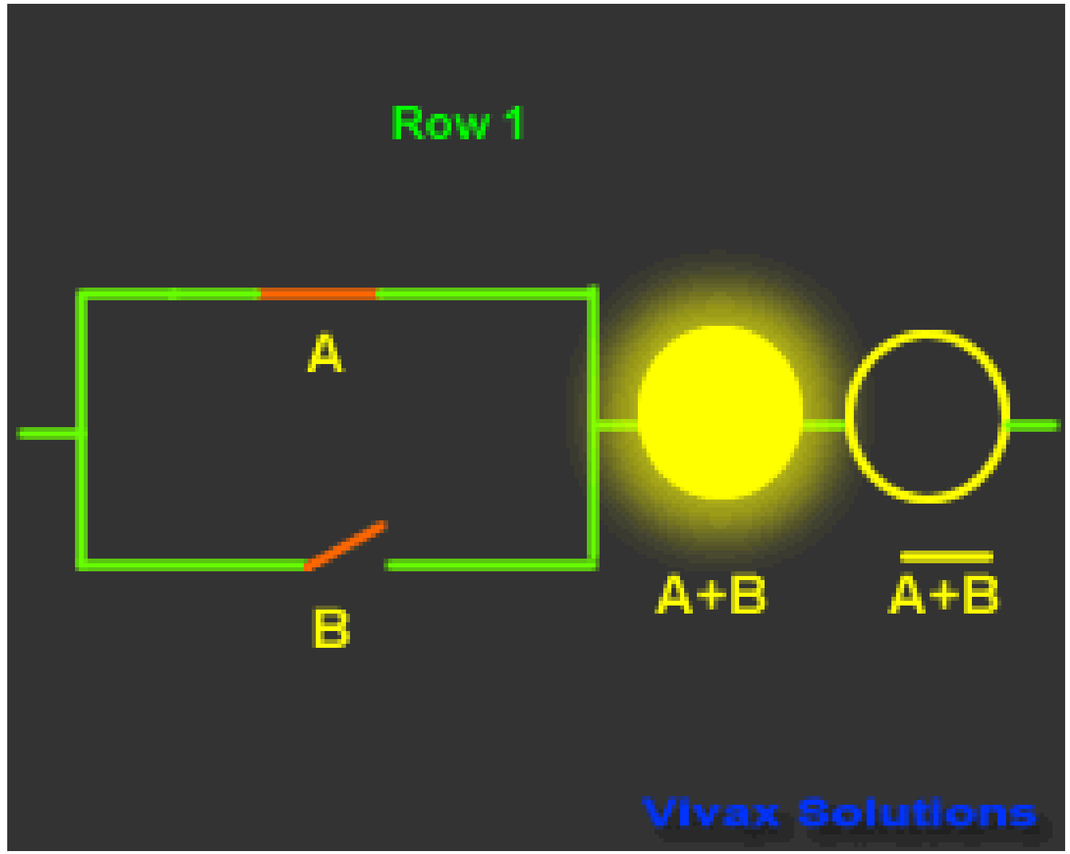


Image Courtesy: www.vivaxsolutions.com

ASSESSMENT - 1

How Laws relates with us….

Question 1

Complement of function (A+B+C)' using theorem and laws is

- a. (A')+B+C
- b. (A+B)'+C
- c. A+B+C
- d. A'B'C'

Question 2

X+X'=? Is equal to

- a. 0
- b. 1
- c. X
- d. X’

References

- https://brilliant.org/wiki/de-morgans-laws/
- https://circuitglobe.com/demorgans-theorem.html
- https://www.electrical4u.com/