Substitute the value of V_{GS} in eqn ①

① $\Rightarrow$ $I_D = I_{DSS}\left(1 - \frac{(-I_D R_S)}{V_P}\right)^2$ → for n-channel

$= I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2$

Apply KVL to the Drain to source junction

$V_S + V_{DS} + I_D R_D - V_{DD} = 0$

$\therefore V_{DS} = V_{DD} - V_S - I_D R_D$

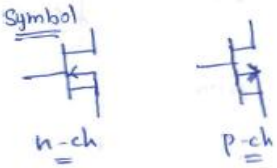
$= V_{DD} - I_D R_S - I_D R_D$

$\therefore V_{DS} = V_{DD} - I_D(R_S + R_D)$

Design of Biasing for MOSFET

* MOSFET – Metal Oxide Semiconductor Field Effect Transistor
* It has a Gate, Source & Drain like the JFET.
* The Drain current (I_D) in the MOSFET is controlled by the Gate-Source Voltage V_{GS}.
* There are 2 types of MOSFETS

Symbol



- Enhancement type (E-MOSFET)
- Depletion type (D-MOSFET)

* MOSFET is also referred to as an IGFET because the gate is isolated from the channel.

1. DMOSFET

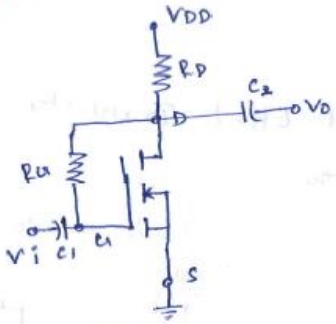
* It is similar to the circuit used for JFET biasing
* The primary difference b/w the two is the fact that depletion type MOSFETs also permits operating points with positive value of V_{GS} for n-channel & negative values of V_{GS} for p-channel.
* To have positive values of V_{GS} for n-channel & negative value of V_{GS} for p-channel self bias circuit is unsuitable.

[Use only
1. Fixed bias
2. Voltage divider bias]

2. EMOSFET

* It's similar to the circuit used for JFET biasing.
* The primary difference b/w the two is the fact that Enhancement type MOSFETS also permits operating points with positive value of V_{GS} for n-channel & negative values of V_{GS} for p-channel.
* To have positive values of V_{GS} the n-channel & negative value of V_{GS} for p-channel self bias circuit is unsuitable.
* Here, we will discuss only feedback bias & voltage divider bias circuit.

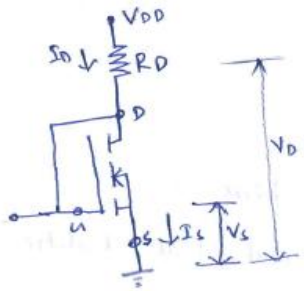
1. Feed Back Bias



Dc Analysis :

* For dc Analysis we can replace coupling capacitors by open circuit & replace the R_G by a short circuit equivalent. Since $I_G = 0$.
* The Drain & Gate Terminals are shorted.

$$V_D = V_D \quad \& \quad V_{DS} = V_{GS} \quad \because V_S = 0$$



* Apply KVL to the Drain - source junction

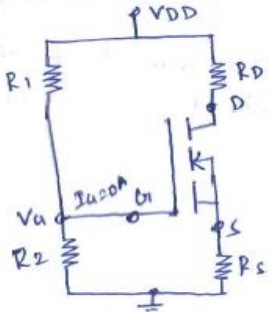
$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D$$

(or)

$$V_{GS} = V_{DD} - I_D R_D$$

2. Voltage Divider Bias



* The biasing resistors R_1 & R_2 are designed to provide positive gate to source voltage.
* Apply KVL to the Gate - source junction

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S$$