19ECB302-VLSI DESIGN

2 MARKS

UNIT II COMBINATIONAL LOGIC CIRCUITS

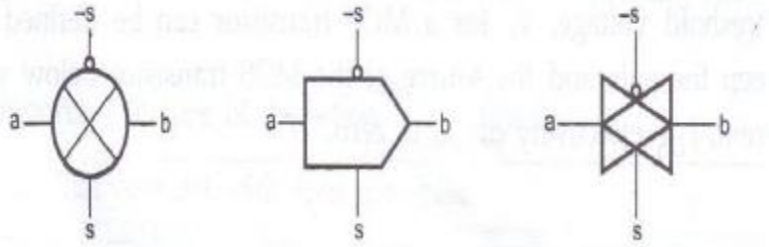
1. What is a pull down device?

A device connected so as to pull the output voltage to the lower supply voltage usually 0 V is called pull down device.

2. What is pull up device?

A device connected so as to pull the output voltage to the upper supply voltage usually VDD is called pull up device.

3. Give the different symbols for transmission gate.



4. What is mean by power and power dissipation?

Power is the rate at which energy is delivered or exchanged; power dissipation is the rate at which energy is taken from the source (VDD) and converted into heat (electrical energy is converted into heat energy during operation).

5. What is mean by PDP?

Power delay product (PDP) = $P_{av} * t_p = (C_L V_{DD})/2^2$
PDP is the average energy consumed per switching event (watts * sec = joule).

6. What is EDP?

Energy delay product (EDP) = PDP* $t_p = P_{av} * t_p^2$
EDP is the average energy consumed multiplied by the computation time required.

7. What are two types of power dissipation?

i) Static dissipation due to leakage current or other current drawn continuously from the power supply.
ii) Dynamic dissipation due to
a) Switching transient current.
b) Charging and discharging of load capacitances.

8. Define elmore delay model.

It is an analytical method used to estimate the RC delay in a network. Elmore delay model

estimates the delay of a RC ladder as the sum over each node in the ladder of the resistance R_{n-1} between that node and a supply multiplied by the capacitor on the nodes.

9. What are the general properties of elmore delay model?

General property of Elmore delay model network has

Single input node

All the capacitors are between a node and ground

Network does not contain any resistive loop

10. What is static power dissipation?

The power dissipation due to leakage current when the MOS transistor is in idle state is called the static power dissipation. Static power due to

Sub threshold conduction through OFF transistors

Tunneling current through gate oxide

Leakage through reverse biased diodes

Contention current in radioed circuits.

11. What is dynamic power dissipation?

Power dissipation is due to circuit switching to charge and discharge the output load capacitance at a particular node at operating frequency is called dynamic power dissipation. The Dynamic power dissipation at a particular output node is given by

$P_d = C_L V_{dd}^2 F_{clk} . A$

Where, C_L = Load capacitance A = Activity factor

V_{dd} = Power supply F_{clk}= Operating frequency

12. What are the methods available to reduce dynamic power dissipation?

1. Reducing the product of capacitance and its switching frequency.
2. Eliminate logic switching that is not necessary for computation.
3. Reduce activity factor Reduce supply voltage

13. What are the methods to reduce static power dissipation?

1. By selecting multi threshold voltages on circuit paths with low-V_t transistors while leakage on other paths with high-V_t transistors.
2. By using two operating modes, active and standby for each function blocks.
3. By adjusting the body bias (i.e) adjusting FBB (Forward Body Bias) in active mode to increase performance and RBB (Reverse Body Bias) in standby mode to reduce leakage.
4. By using sleep transistors to isolate the supply from the block to achieve significant leakage power savings.

14. What is short circuit power dissipation?

During switching, both NMOS and PMOS transistors will conduct simultaneously and provide a direct path between VDD to ground resulting in short circuit power dissipation.

15. Define design margin.

The additional performance capability above required standard basic system parameters that may be specified by a system designer to compensate for uncertainties is called design margin. Design margin required as there are three sources of variation two environmental and one manufacturing.

16. Write the applications of transmission gate?
Multiplexing element of path selector
A latch element an unlock switch
Act as a voltage controlled resistor connecting the input and output.

17. What is pass transistor?

It is a MOS transistor, in which gate is driven by a control signal, when the control signal is high, input is passed to the output and when the control signal is low, the output is floating topology such topology circuits is called pass transistor.

18. List the advantages of pass transistor logic.

Pass transistor logic circuits are often superior to standard CMOS circuits in terms of layout density, circuit delay and power consumption.

They do not have path VDD to GND and do not dissipate standby power (static power dissipation).

19. What is transmission gate?

The circuit constructed with the parallel connection of PMOS and NMOS with shorted drain and source terminals. The gate terminal uses two select signals s and , when s is high than the transmission gate passes the signal on the input. The main advantage of transmission gate is that it eliminates the threshold voltage drop.

20. Why low power has become an important issue in the VLSI circuit realization?

Increasing transistor count:

The number of transistor is getting doubled in every 18 months based on moore's law

Higher speed of operation:

The power dissipation is proportional to clock frequency

Greater device leakage current:

In nanometer technology the leakage component become a significant percentage of the total power and the leakage current increases at a faster rate than dynamic power in technology generations.

21. What are the various ways to reduce the delay time of a CMOS inverter?

1. The width of the MOS transistor can be increased to reduce delay this is known as gate sizing, which will be discussed later in more details.
2. The load capacitance can be reduced to reduce delay this is achieved by using transistor of smaller and smaller dimension by feature generation technology.
3. Delay can also be reduced by increasing the supply voltage VDD and reducing the threshold voltage V_t of the MOS transistors

22. Explain the basic operation of a 2- phase dynamic circuit.

The operation of the circuit can be explained using pre-charge logic in which the output is pre-charged to HIGH level during Φ_2 clock and the output is evaluated during Φ_1 clock.

23. What makes dynamic CMOS circuits faster than static CMOS circuits?

As MOS dynamic circuits require lesser number of transistors and capacitance is to be driven by it. This makes MOS dynamic circuits faster.

24. What is glitch power dissipation?

Because of finite delay of the gates used to realize the Boolean functions, different signals cannot reach the inputs of a gate simultaneously this leads to spurious transition at the output before it settles down to its final value, the spurious transitions leads to charging and discharging of the outputs causing glitch power dissipation.