SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

16EC303–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 1 –MOS TRANSISTOR PRINCIPLE

TOPIC 9 –LAYOUT DIAGRAM

OUTLINE

- LAYOUT DIAGRAMS-INTRODUCTION
- DETAILED MASK VIEWS
- CMOS INVERTER LAYOUT DIAGRAM
- DESIGN STEPS & MICROWIND TOOL
- MOS DEVICE :PERFORMANCE STEPS
- LAYOUT DESIGN RULES NEEDS –STEPS 1 to 4
- ACTIVITY
- STEP 5 TO 8
- FINAL CONNECTIONS
- CHECK DESIGN RULE CHECK (DRC) & ASSIGN SOURCE
- SIMULATION & VOTAGE TRANSFER CHARECTERISTICS
- 1. SCALABLE DESIGN RULES
  (E.G. SCMOS, Λ-BASED DESIGN RULES):
- 2. ABSOLUTE DESIGN RULES (E.G. M-BASED DESIGN RULES
- CMOS DESIGNS ENTITIES & CMOS INVERTER LAYOUT
- ASSESSMENT
- SUMMARY & THANK YOU

LAYOUT DIAGRAMS-INTRODUCTION

-Chips are specified with set of masks

-Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)

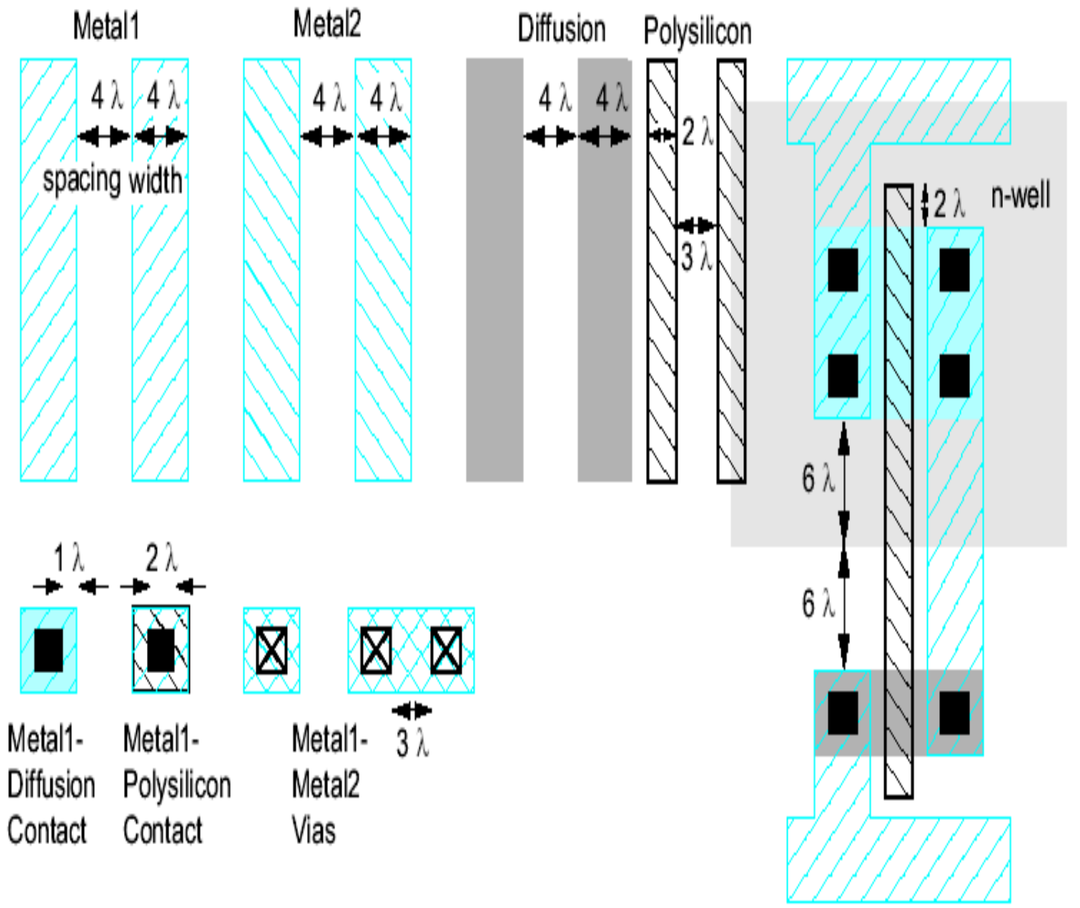
-Feature size f = distance between source and drain

-Set by minimum width of polysilicon

-Feature size improves 30% every 3 years or so Normalize for feature size when describing design rules

Express rules in terms of $\lambda = f/2$

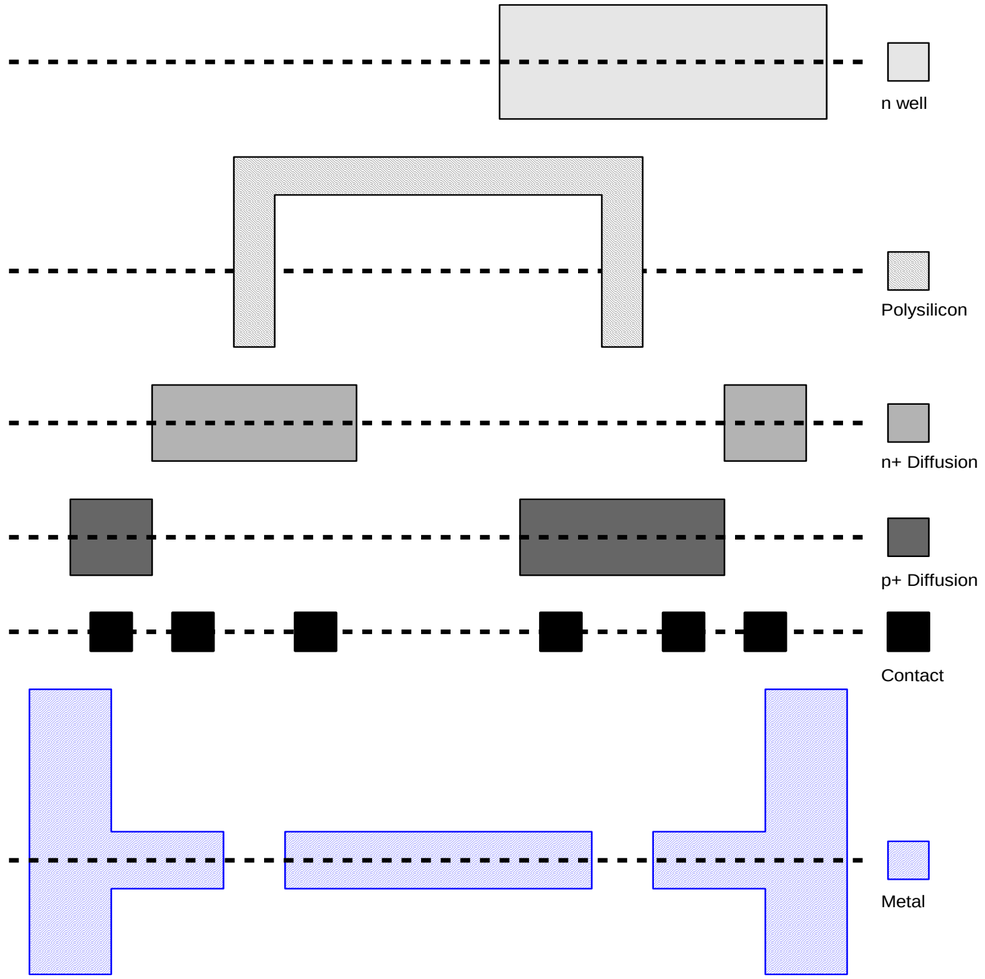
E.g. λ = 0.3 mm in 0.6 mm process



DETAILED MASK VIEWS

Six masks

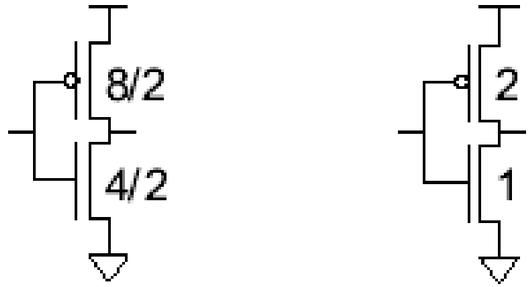
- n-well
- Polysilicon
- n+ diffusion
- p+ diffusion
- Contact
- Metal

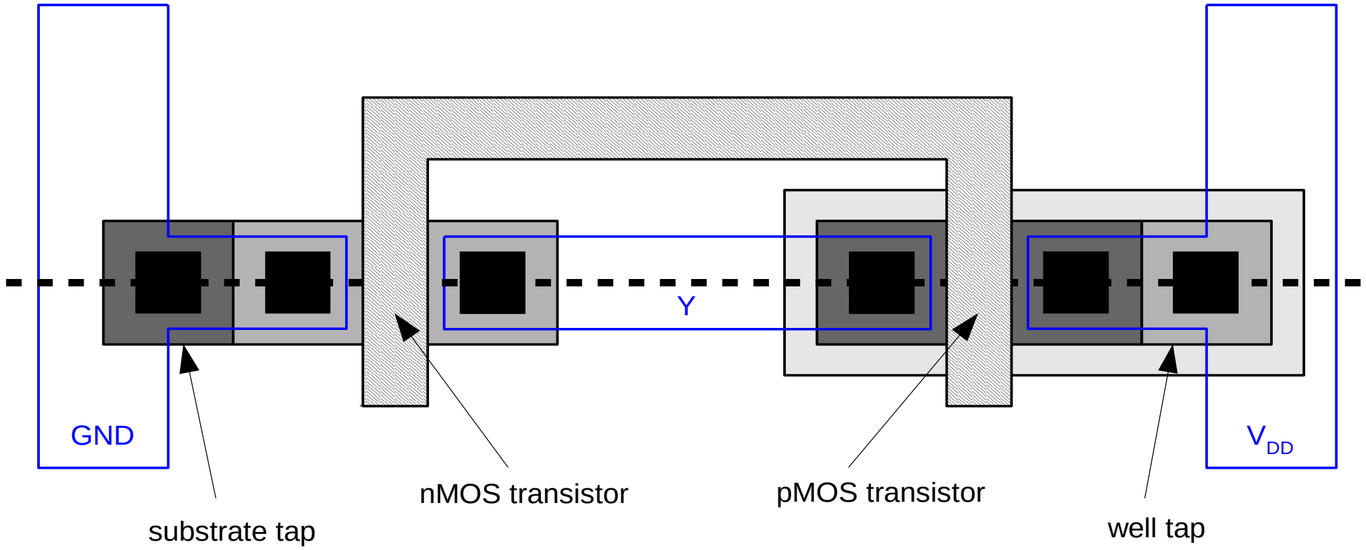


CMOS INVERTER LAYOUT DIAGRAM

Transistor dimensions specified as Width / Length

- Minimum size is 4l / 2l, sometimes called 1 unit
- In f = 0.6 mm process, this is 1.2 mm wide, 0.6 mm long

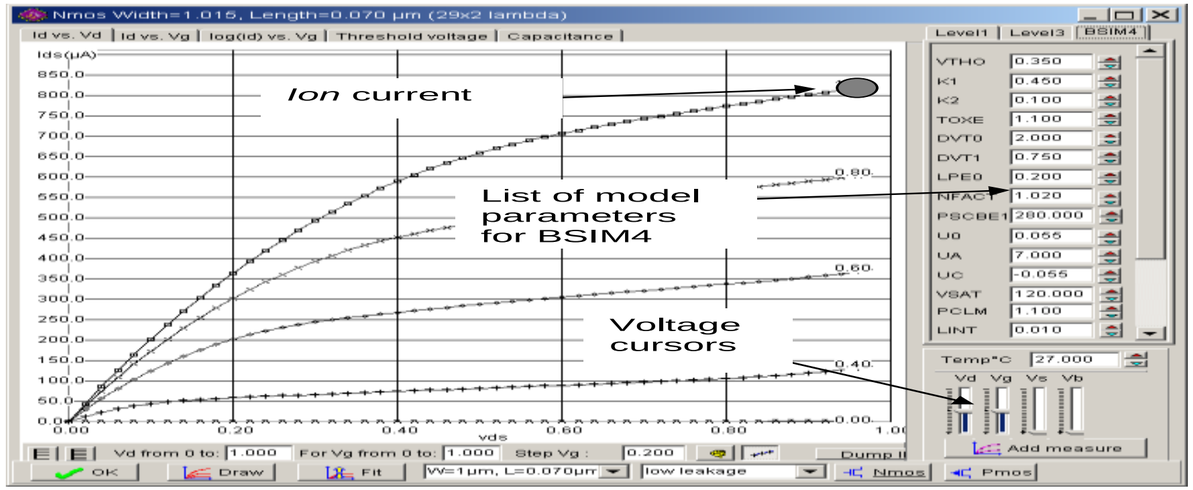




DESIGN STEPS & MICROWIND TOOL

- SCHEMATIC
- LAYOUT DESIGN
- DRC
- LAYOUT Vs SCHEMATIC
- PARASITIC EXTRACTION
- POST LAYOUT SIMULTION

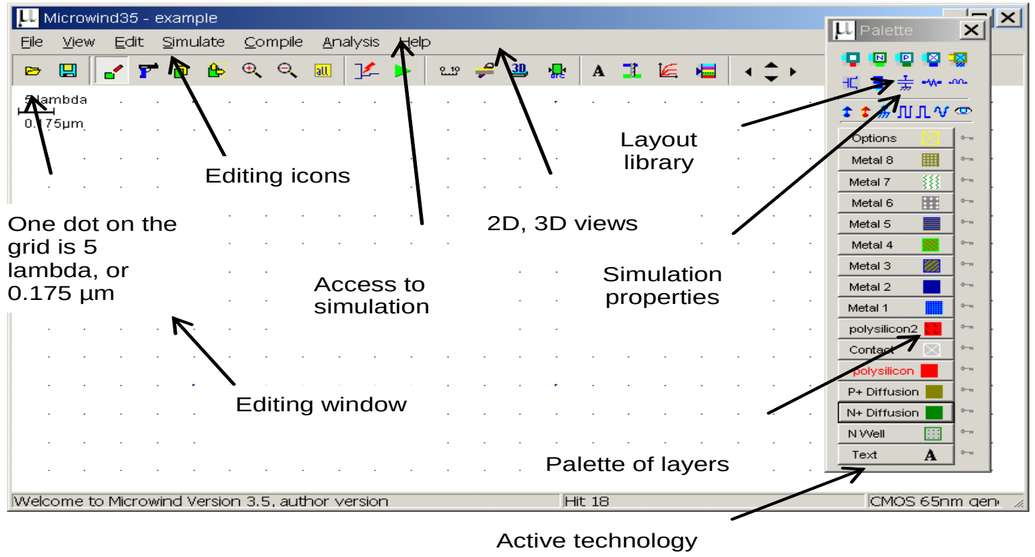
Microwind is a tool for designing and simulating circuits at layout level.
The tool features full editing facilities (copy, cut, past, duplicate, move), various views (MOS characteristics, 2D cross section, 3D process viewer), and an analog simulator



MICROWIND :TOOLS & HOW TO GET TOOL

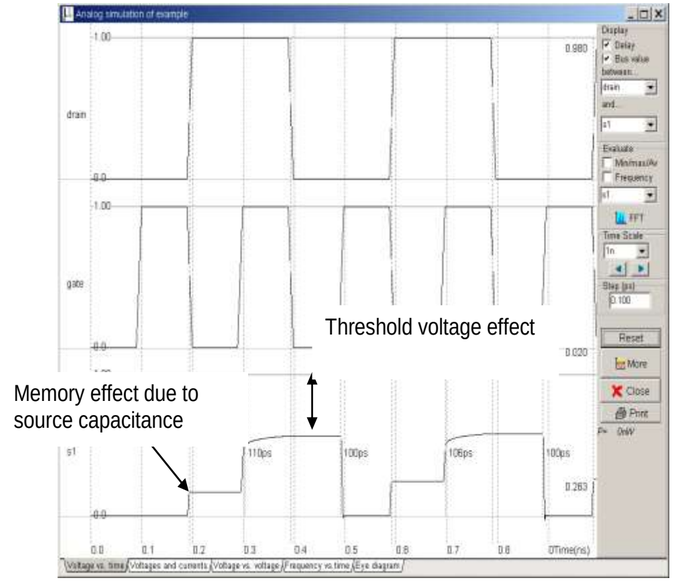
- Microwind
- DSCH
- Microwind3 Editor
- Microwind 2D viewer
- Microwind 3D viewer
- Microwind analog simulator
- Microwind tutorial on MOS devices
- View of Silicon Atoms

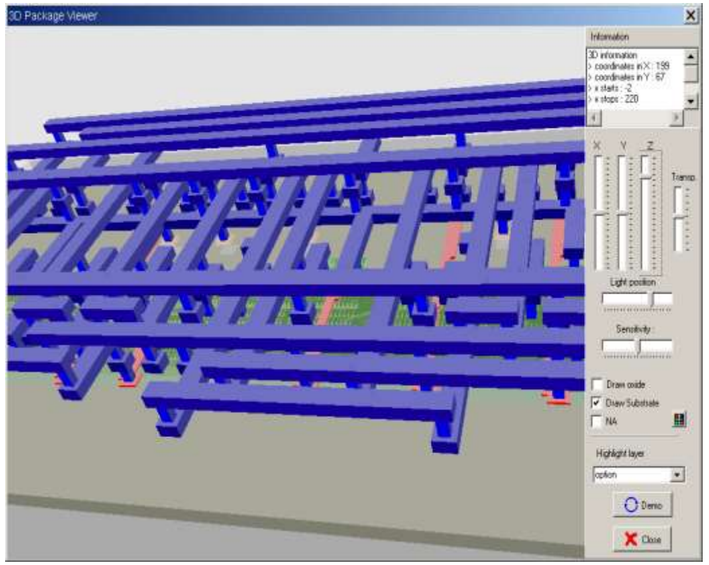
- Go to the website
- http://www.microwind.net/document
- Download the freeware version of the micro wind
- Unzip the files in a Folder



INTRODUCTION THE TOOL

- User-friendly and intuitive design tool for educational use.
- The student draws the masks of the circuit layout and performs analog simulation
- The tool displays the layout in 2D, static 3D and animated 3D



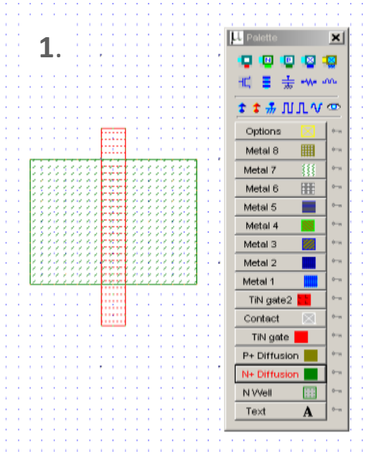


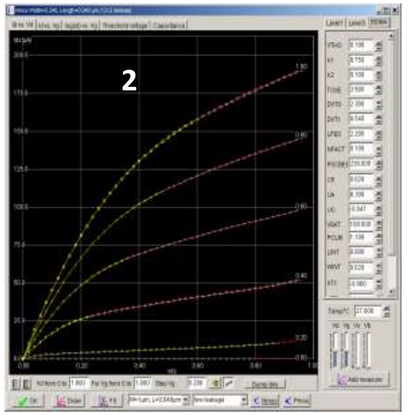
MOS DEVICE :PERFORMANCE STEPS

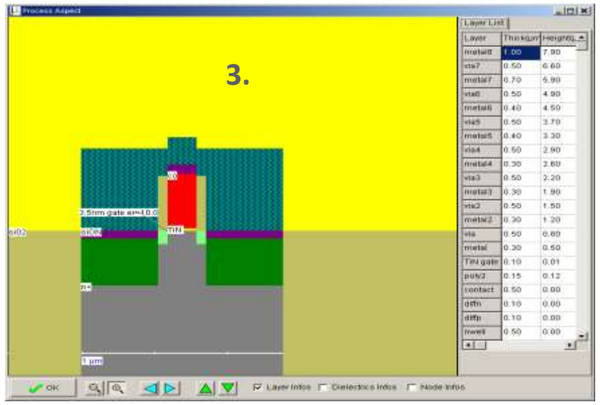
Traditional teaching : in-depth explanation of the potentials, fields, threshold voltage, and eventually the expression of the current *Ids*

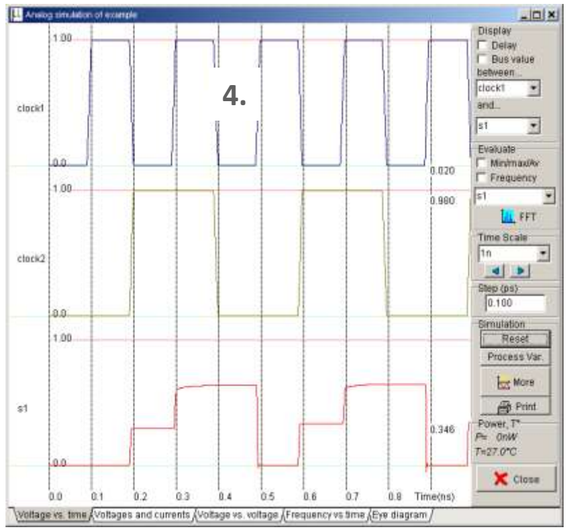
Our approach : step-by-step illustration of the most important relationships between layout and performance.

1. **Design of the MOS**
2. **I/V Simulation**
3. **2D view**
4. **Time domain analysis**





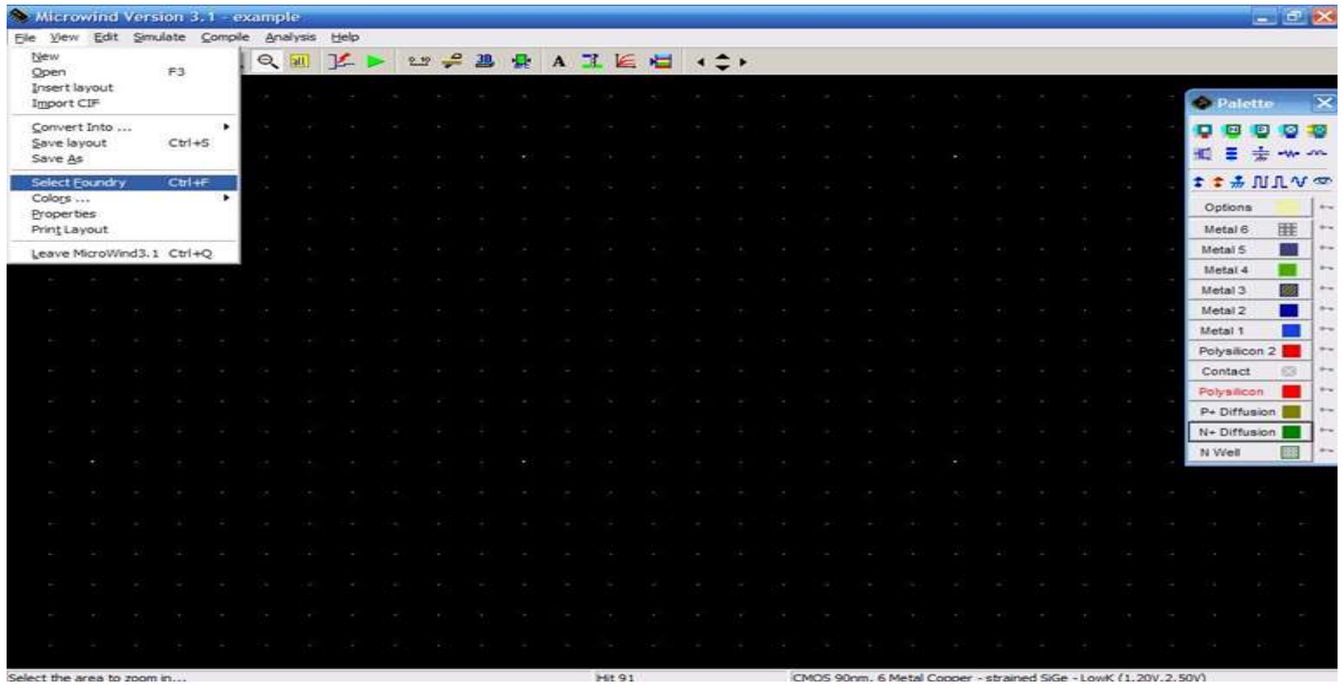




LAYOUT DESIGN RULES NEEDS

•Interface or communication link between the circuit designer and the process engineer during the manufacturing phase.

- Photo resist shrinkage, tearing.
- Variations in material deposition, temperature and oxide thickness.
- Impurities.
- Variations across a wafer.

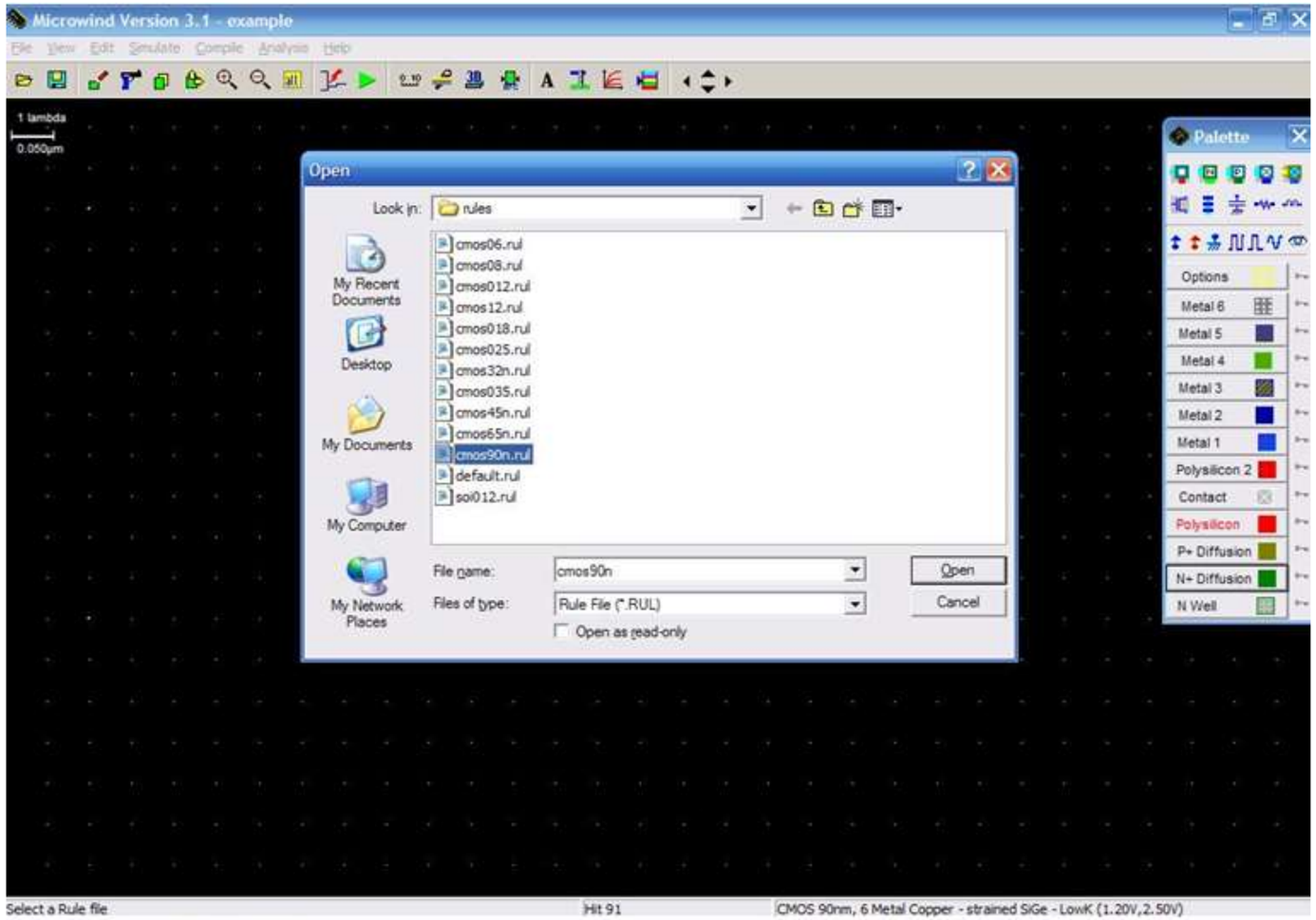


Step 1: Select Foundry

LAYOUT DIAGRAMS NEEDS

To avoid

- **Transistor problems**
- **Wiring problems**
- **Oxide problems**
- **Via problems**

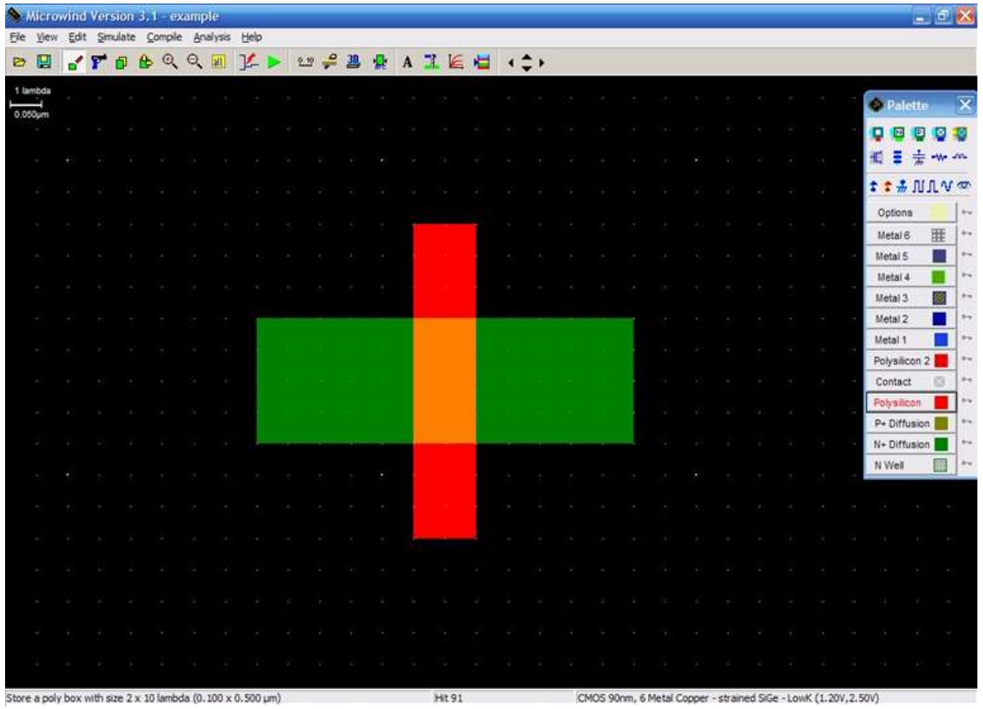


Step 2: Select Technology

TWO ISSUES & TYPES OF DESIGN RULES

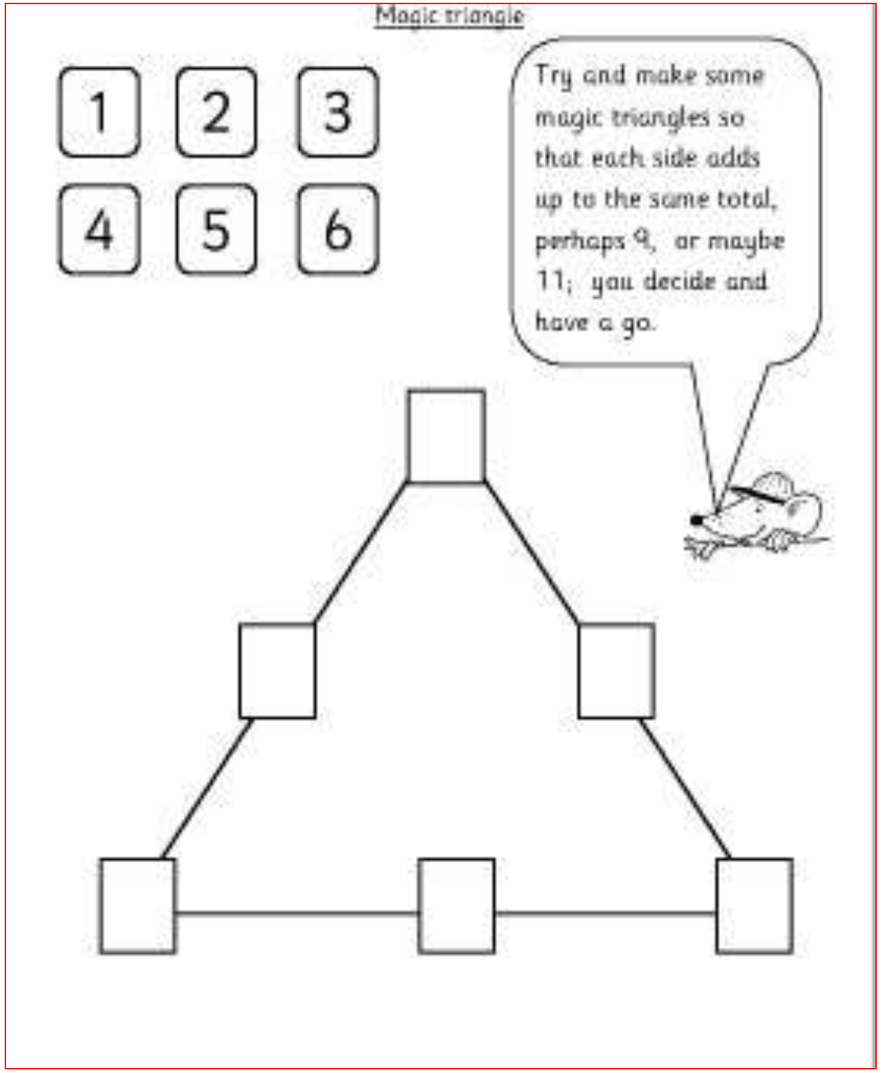
1. The geometrical reproduction of features that can be reproduced by the mask making and lithographical process.
2. The interaction between different layers.

1. Linear scaling is possible only over a limited range of dimensions.
2. Scalable design rules are conservative .This results in over dimensioned and less dense design.
3. This rule is not used in real life.

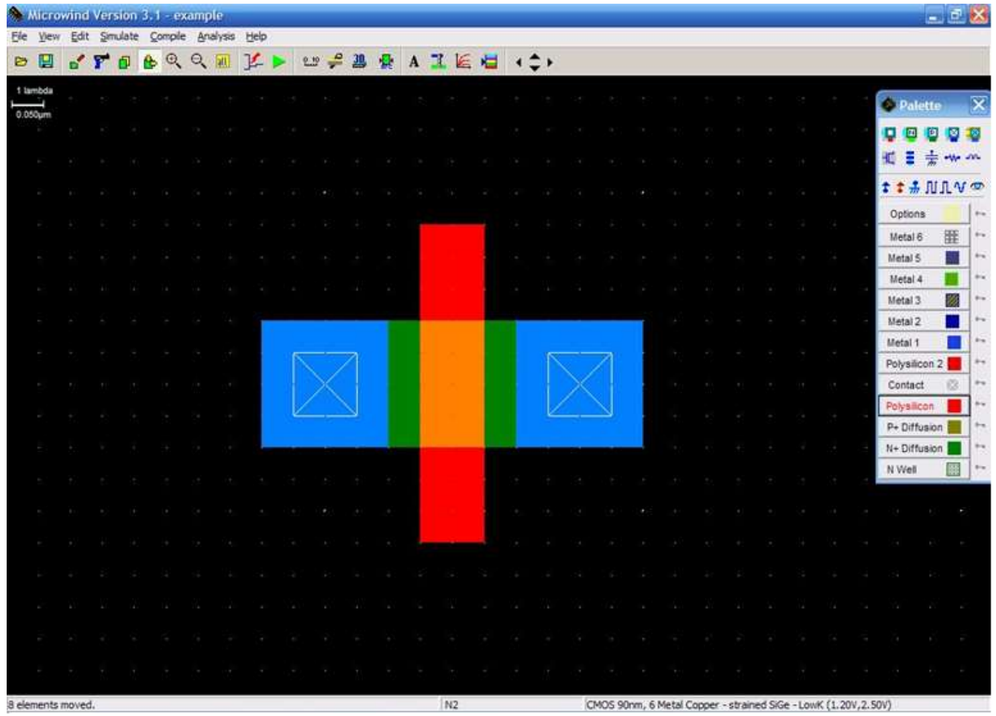


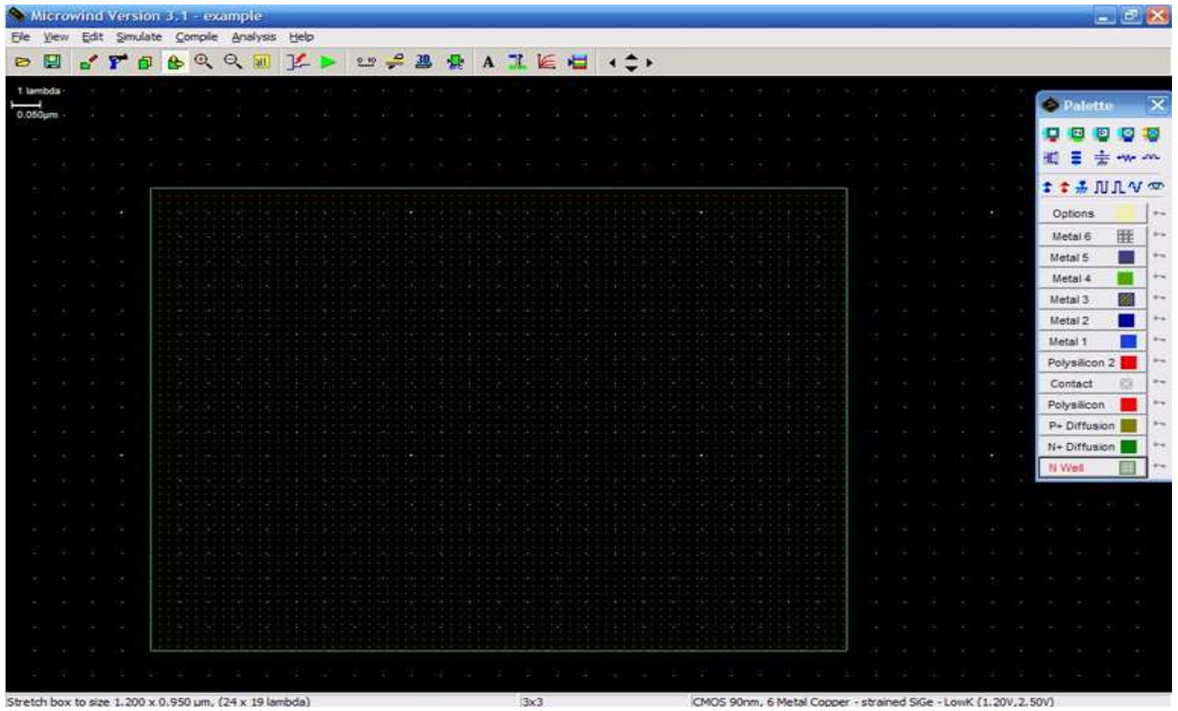
Step 3& 4: n+ Diffusion& Poly silicon

CLASS ROOM ACTIVITY



STEP 5 &6

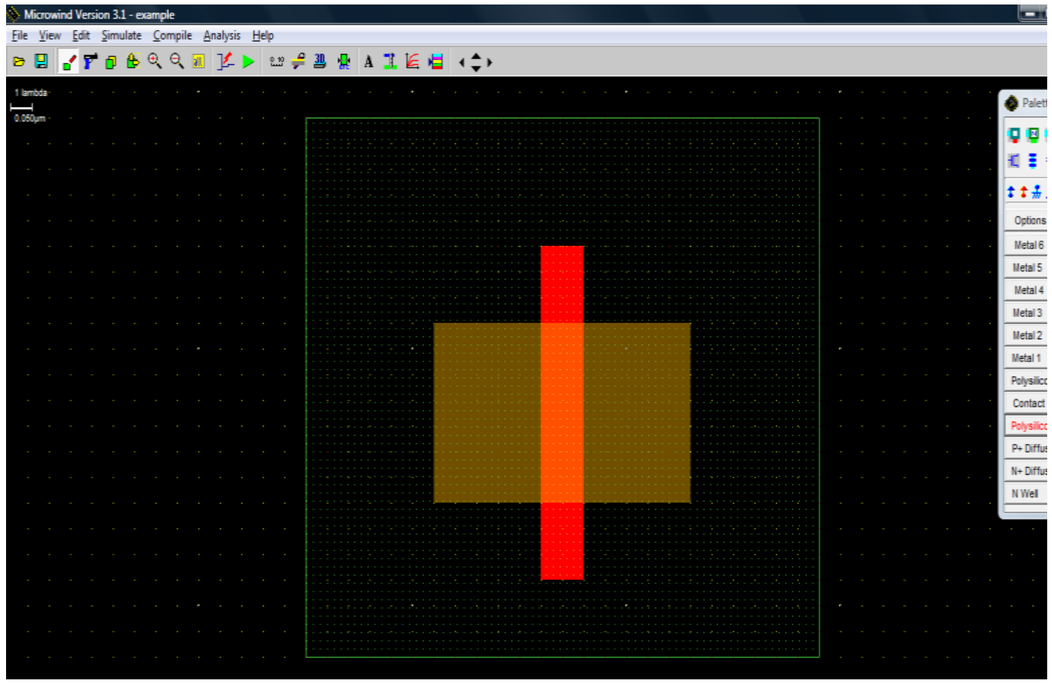




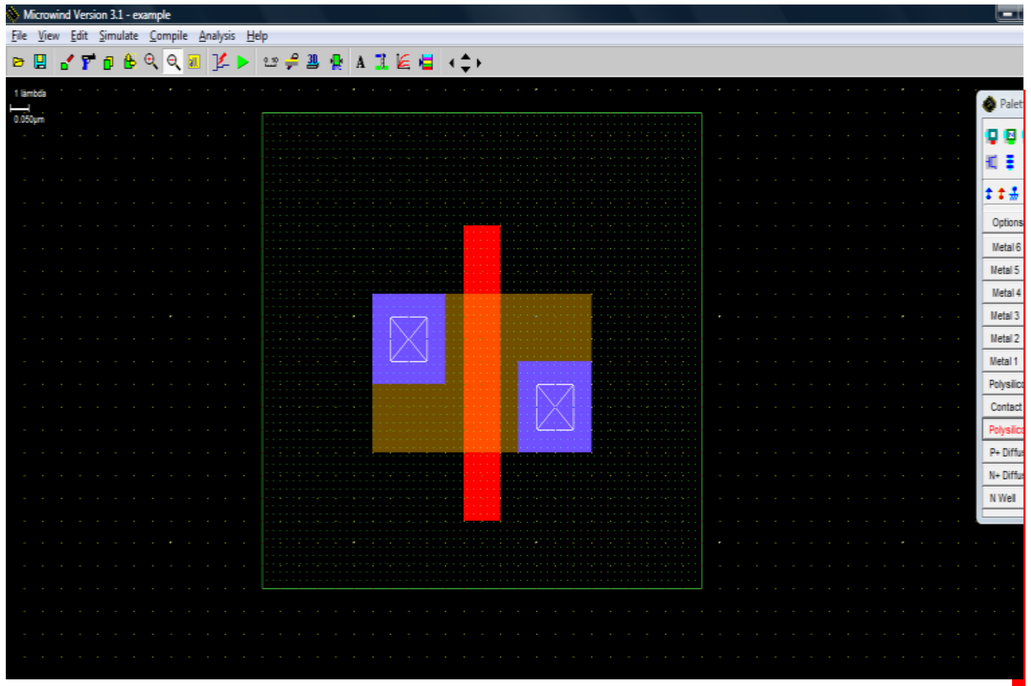
Step 5: n+diff and Metal Contact

Step 6: Create N Well

STEP 7&8



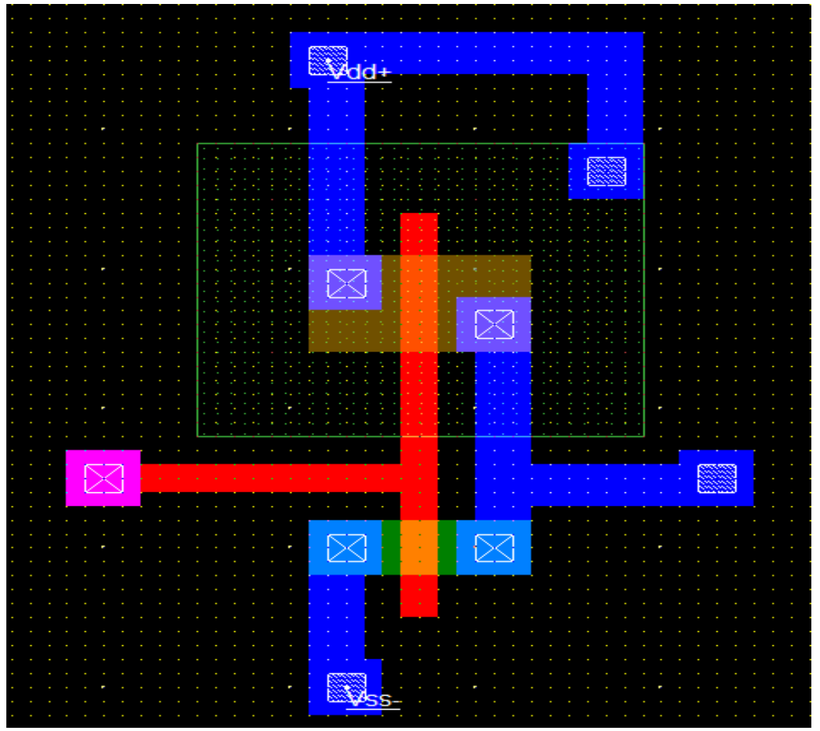
Step 7: Polysilicon



Step 8: Contacts

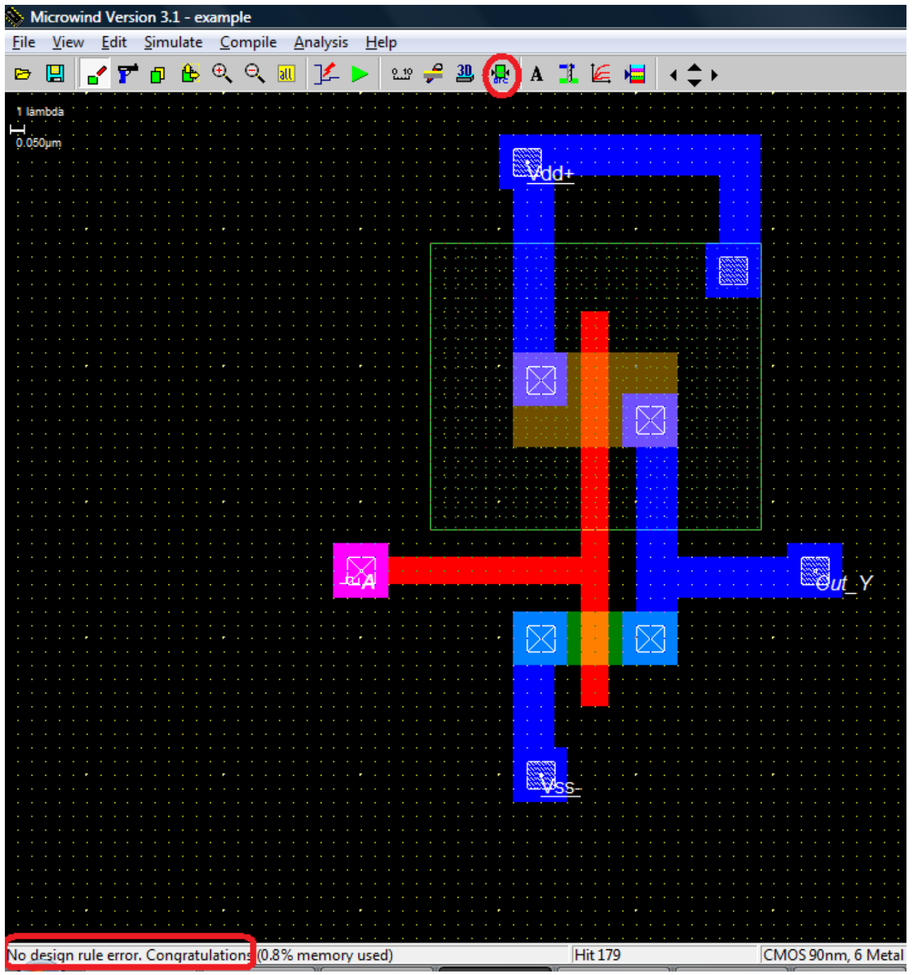
FINAL CONNECTIONS

- pMOS Completed
- Now Interconnection of pMOS and nMOS to complete inverter
- Connect Source of pMOS to VDD and Source of nMOS to VSS.
- Short the Drain of both pMOS and nMOS.



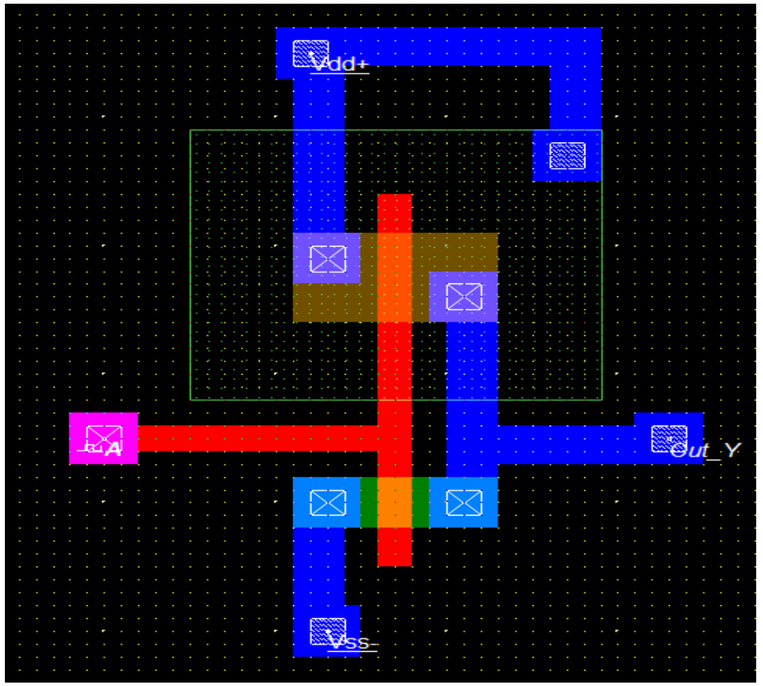
INVERTER: Complete Design

CHECK DESIGN RULE CHECK (DRC) & ASSIGN SOURCE

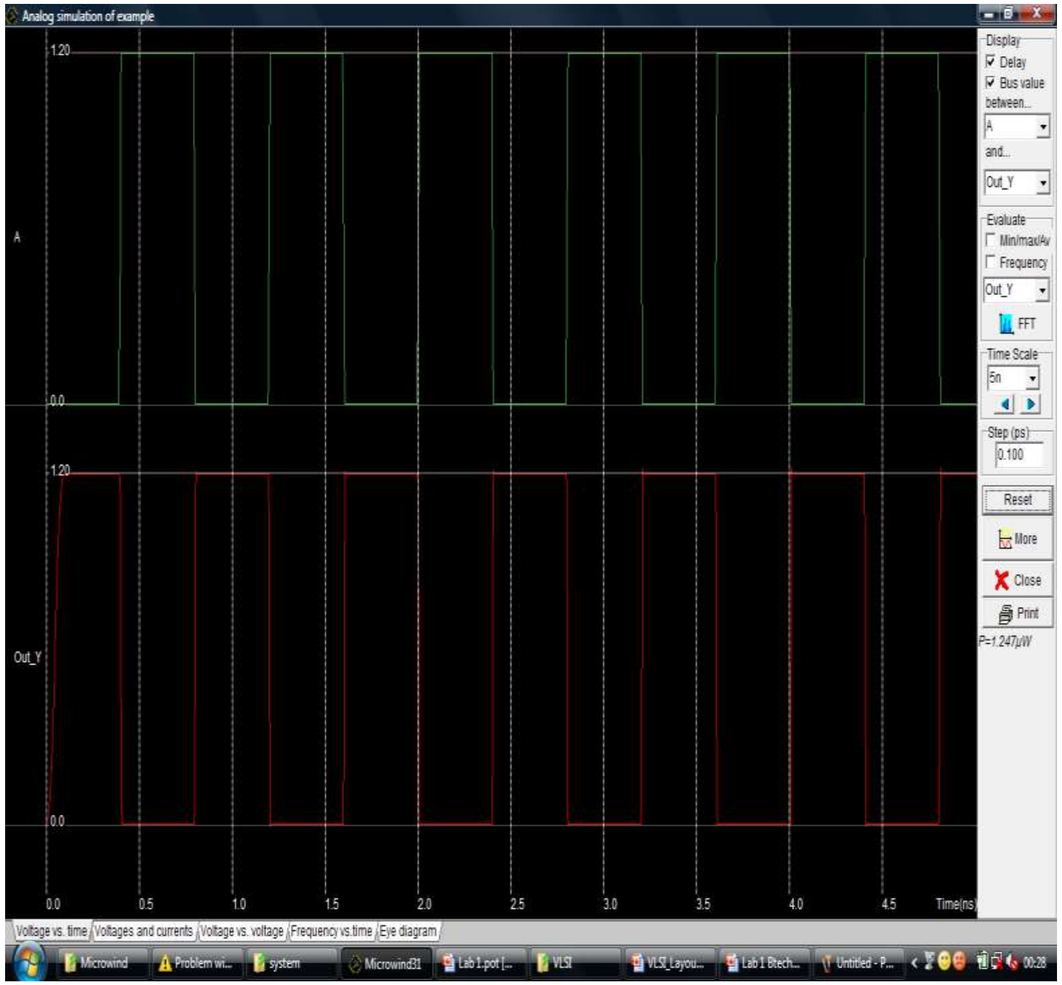


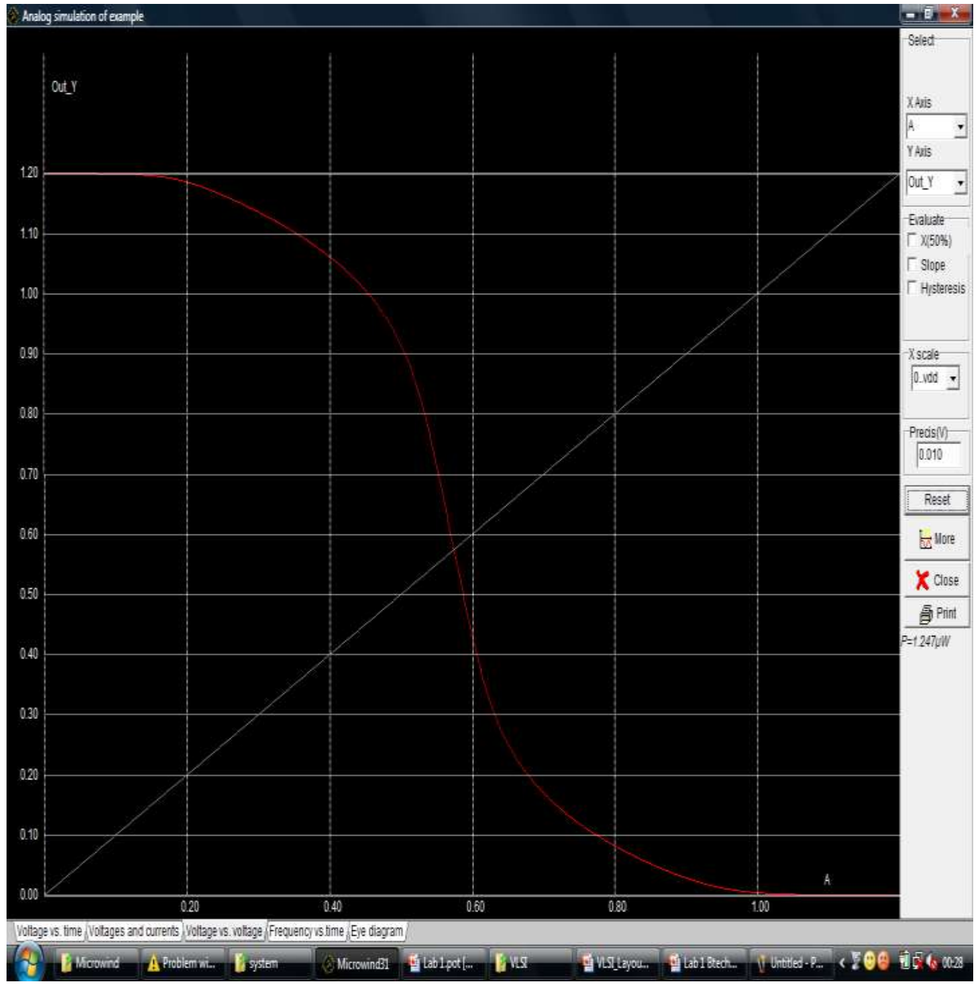
Assign Signal (Clock) to Gate Terminal

Add Visible node at Output



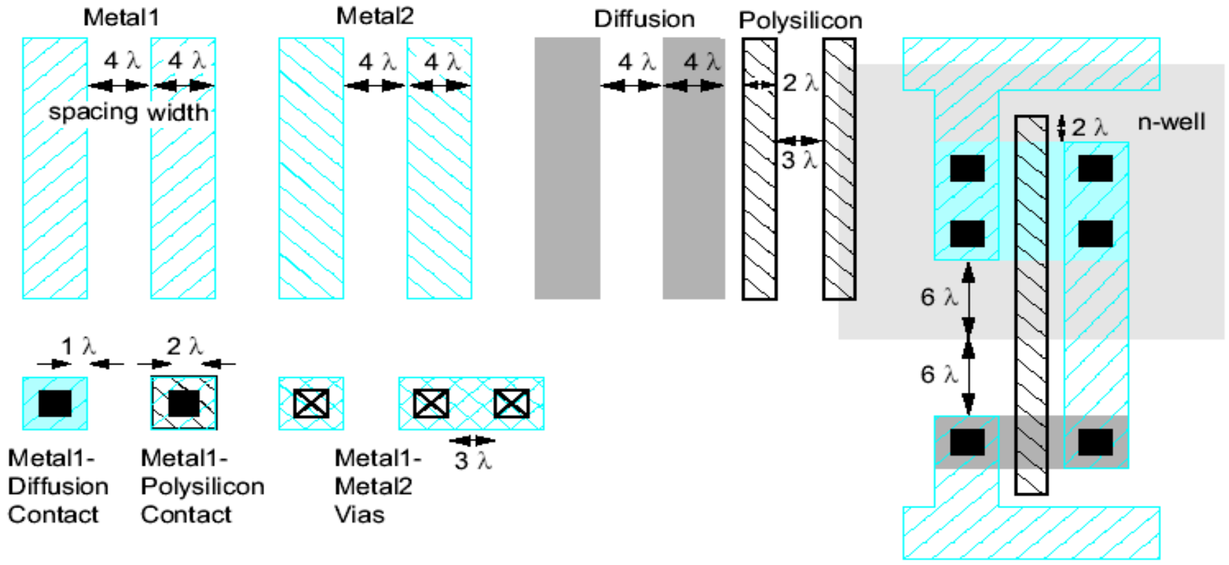
RUN SIMULATION & VOTAGE TRANSFER CHARECTERISTICS (VTC) CHARACTERISTICS





1. SCALABLE DESIGN RULES (E.G. SCMOS, Λ-BASED DESIGN RULES):

- Rules are defined in terms of a single parameter λ.
- design can be easily ported over a cross section of industrial process ,making the layout portable .
- Scaling can be easily done by simply changing the value

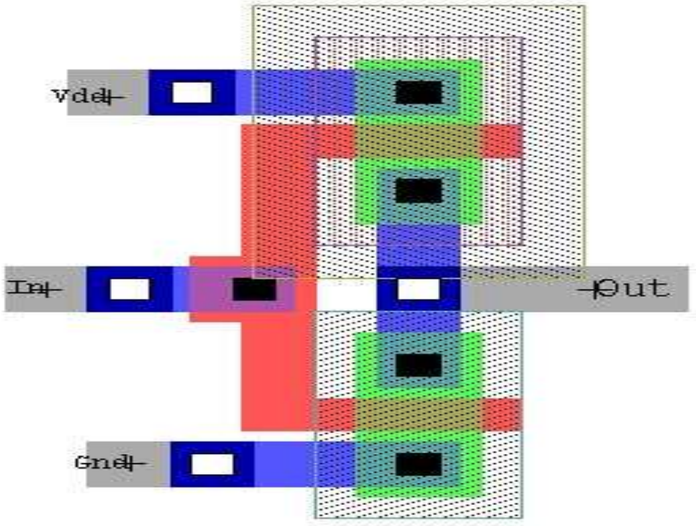


2. **ABSOLUTE DESIGN RULES (E.G. M-BASED DESIGN RULES)**

•Design rules are expressed in absolute dimensions (e.g. 0.75µm) and therefore can exploit the features of a given process to a maximum degree.
•Here, scaling and porting is more demanding, and has to be performed either manually or using CAD tools .
•more complex for deep submicron.
•set of design rules is the minimum line width .
•It stands for the minimum mask dimension that can be safely transferred to the semiconductor material .
•Even for the same minimum dimension, design rules tend to differ from company to company, and from process to process.

CMOS DESIGNS ENTITIES & CMOS INVERTER LAYOUT

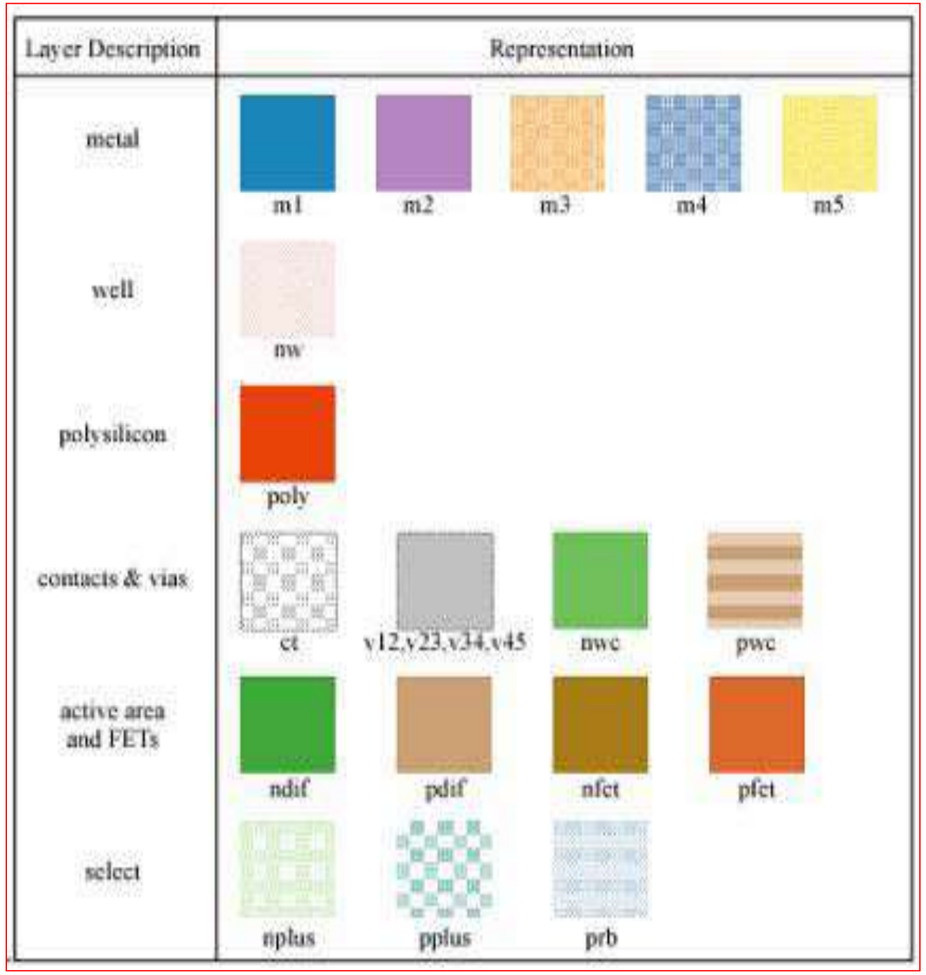
- Two different substrates and/or wells: which are p-type for NMOS and n-type for PMOS.
- Diffusion regions (p+ and n+): which defines the area where transistors can be formed. These regions are also called active areas. Diffusion of an inverse type is needed to implement contacts to the well or to substrate. These are called select regions
- Transistor gate electrodes : Polysilicon layer
- Metal interconnect layers
- Interlayer contacts and via layers.



CMOS LAYOUT DIAGRAM

The layers for typical CMOS processes are represented in various figures in terms of:

- A colour scheme (**Mead-Conway colours**).
- Other colour schemes designed to differentiate CMOS structures.
- Varying stipple patterns
- Varying line styles



ASSESSMENT

1.Six masks

- n-well
- ----------
- n+ diffusion
- p+ diffusion
- ----------
- ----------

2.List out two issues without layout diagrams(needs of layout diagrams)

3.Compare two layout design rules.

4.List out the micro wind layout design steps

SUMMARY & THANK YOU