UNIT-III

JFET and MOSFET Amplifiers

JFET Amplifiers

* It provide an excellent voltage gain (A_v) with the added advantage of a high input impedance (Z_i).
* For this reason JFETs are often preferred over BJTs for certain types of applications.
* There are 3 basic configurations ** 2 Mark
  1. Common Source
  2. Common Drain (source follower)
  3. Common Gate
* The difference between BJT & JFET configurations:

BJT	JFET
It controls large output current (I_c) by means of a relative small input current (I_b).	It controls large output current (I_D) by means of a small input voltage (V_g)

Small Signal Analysis of JFET Amplifiers

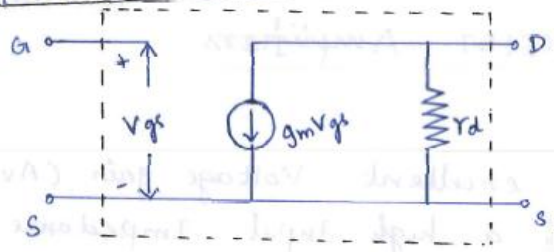
* The Drain to source current of JFET is controlled by gate to source voltage.
* The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor g_m.

$$g_m = \frac{\Delta I_d}{\Delta V_{GS}}$$

* Another important parameter is drain resistance r_d.

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Big|_{V_{GS} = \text{constant}}$$

AC Equivalent Circuit :-



∴ 2 Mark

Fig: N-channel JFET - CS

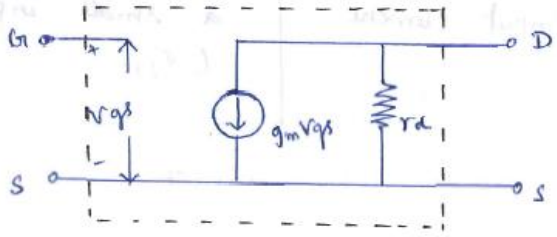
* The relation of $\frac{Id}{Vgs}$ is included as current source $g_m V_{gs}$ connected from drain to source.

* The input impedance is represented by the open circuit at it's input terminal, since I_G is zero.

* The Output impedance is represented by rd from drain to source.

Approximate AC Equivalent circuit :-

* When the value of external drain resistance R_D is very small as compared to the value of output impedance represented by rd, it's possible to replace rd by open circuit.



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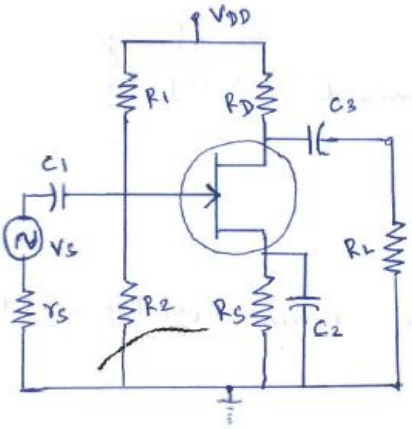
1. Common Source Circuit Analysis



=> * The input terminals are the Gate & Source, & the Output terminals are the Drain & the Source.

* So the Source terminal is common to both input & output, & the circuit configuration is known as common Source (CS

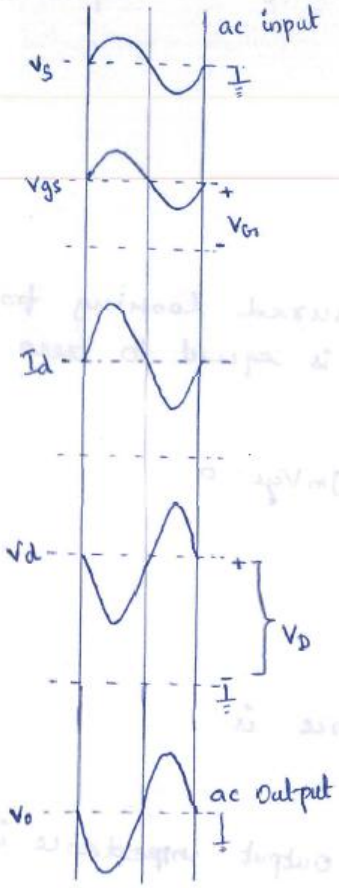


Fig: Voltage & current Waveforms

* For positive-going input signal (V_s) There is a 180° phase shift between the input & the Output.

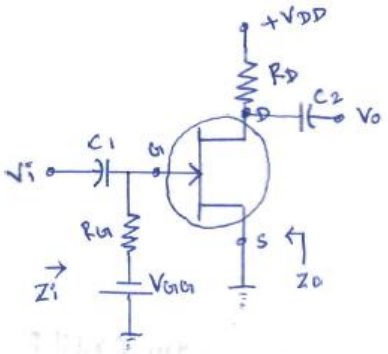
* An increase in V_s increasing the V_{GS} Thus raising the level of I_D & increasing the voltage drop across R_D.

* This produces a decreases in the level of V_D, which is capacitor coupled to the circuit Output as a negative going ac output voltage (V_o)

* Consequently, as V_s increase in a positive direction, V_o changes in negative direction.

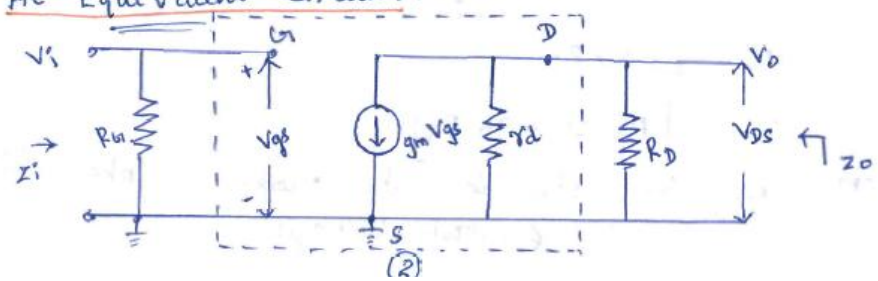
* Consequently, when V_s changes in negative direction, the resultant decrease in V_{GS} reduces I_D & produces a positive-going Output.

1. JFET with Fixed Bias ⁂ 2 Mark



* The coupling capacitors C_1 & C_2 which are used to isolate the d.c biasing from the applied a.c signal act as short circuits for the ac analysis.

Ac Equivalent Circuit:



* The circuit is drawn by replacing all capacitors & d.c supply voltage with short circuits.

1. Input Impedance (Z_i)

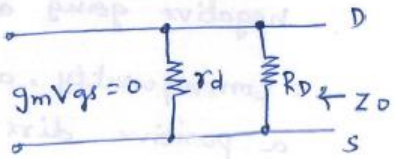
$$\boxed{Z_i = R_G}$$

2. Output Impedance (Z_o)

* It's the impedance measured looking from the output side with input voltage (V_i) is equal to zero.

* As $V_i = 0$

$V_{gs} = 0$ & hence $g_m V_{gs} = 0$



So the Output Impedance is

$$\boxed{Z_o = R_D \| r_d}$$

* if $r_d >> R_D$ Then the output impedance is

$$\boxed{Z_o \simeq R_D}$$

3. Voltage Gain (A_V)

$$A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_o}{V_i}$$

$$V_o = -g_m V_{gs} (r_d \| R_D)$$

* W.K.T $V_i = V_{gs}$ Then

$$V_o = -g_m V_i (r_d \| R_D)$$

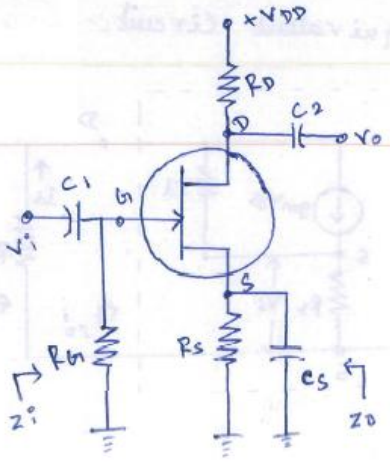
So $$A_V = \frac{-g_m V_i (r_d \| R_D)}{V_i} = \boxed{-g_m (r_d \| R_D)}$$

* if $r_d >> R_D$

$$\boxed{A_V \simeq -g_m R_D}$$

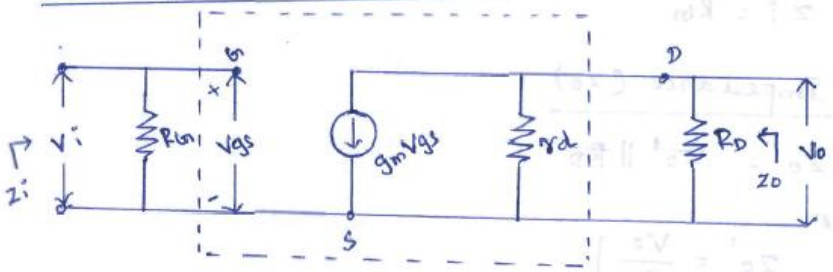
* The negative sign indicate there is a phase shift of 180° between the input & output voltages.

2. JFET with Self Bias (Bypassed R_s)



* The coupling capacitors C_1 & C_2 which are used to isolate the dc biasing from applied ac signal act as short circuits, for ac analysis
* The Bypass capacitor C_s also act as a short circuit for ac analysis.

Ac Equivalent circuit:



* It's drawn by replacing all capacitors & dc supply V_{DD} with short circuits.
* This circuit is similar to ac equivalent circuit of Fixed bias.

1. Input Impedance (Z_i)

$$Z_i = R_G$$

2. Output Impedance (Z_o)

$$Z_o = r_d \,||\, R_D$$

if $r_d >> R_D$

$$Z_o \cong R_D$$

3. Voltage gain (A_v)

∴ 2 Marks

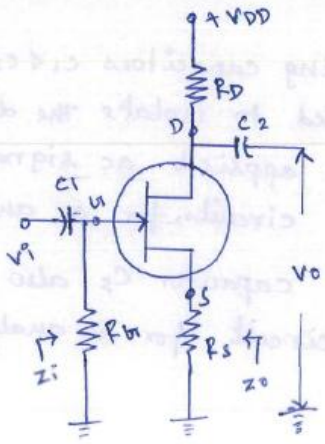
$$A_v = -g_m (r_d \,||\, R_D)$$

if $r_d >> R_D$

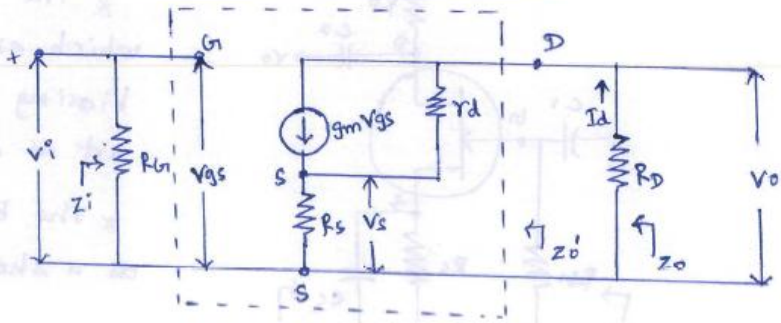
$$A_v \cong -g_m R_D$$

* The negative sign indicate there is a 180° phase shift between input & Output voltages.

3. JFET with Self Bias (Unbypassed R_S)



Ac Equivalent circuit:



1. Input Impedance (Z_i)

$$Z_i = R_G$$

2. Output Impedance (Z_o)

$$Z_o = Z_o' \parallel R_D$$

Where

$$Z_o' = \frac{V_o}{I_d}\Big|_{V_i = 0}$$

* Apply KVL to the Output circuit

$$V_o = (I_d - g_m V_{gs})\, r_d + I_d R_s \qquad -(1)$$

* Apply KVL to the input circuit

$$V_{gs} = V_{in} - I_d R_s$$

$\because V_{in} = 0$

$$V_{gs} = -I_d R_s \qquad -(2)$$

sub eqn (2) in (1)

$$V_o = [I_d - g_m(-I_d R_s)]\, r_d + I_d R_s$$

$$= (I_d + g_m I_d R_s)\, r_d + I_d R_s$$

$$= I_d r_d + g_m I_d R_s r_d + I_d R_s$$

$$= I_d [r_d + g_m R_s r_d + R_s]$$

$$\therefore Z_o' = \frac{V_o}{I_d} = \frac{I_d [r_d + g_m R_s r_d + R_s]}{I_d}$$

$\because \mu = g_m r_d$

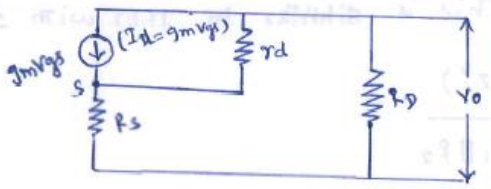
$$\therefore Z_o' = r_d + \mu R_s + R_s = \underline{r_d + R_s(\mu+1)}$$

$$Z_o = Z_o' \| R_D = \underline{[r_d + R_s(\mu+1)] \| R_D}$$

3. Voltage gain (A_v)

$$A_v = \frac{V_o}{V_i}$$

* W.K.T $V_o = -I_d R_D$



* Apply KVL to the Output of this circuit.

$$(I_d - g_m V_{gs}) r_d + I_d R_s + I_d R_D = 0 \quad -③$$

W.K.T $V_{gs} = V_{in} - I_d R_s \quad -④$ ($V_{in} \downarrow V_i$)

Sub ④ in ③

$$[I_d - g_m (V_i - I_d R_s)] r_d + I_d R_s + I_d R_D = 0$$

$$I_d r_d - g_m V_i r_d + g_m I_d R_s r_d + I_d R_s + I_d R_D = 0$$

$$I_d r_d + g_m I_d R_s r_d + I_d R_s + I_d R_D = g_m V_i r_d$$

$$I_d (r_d + g_m R_s r_d + R_s + R_D) = g_m V_i r_d$$

$$I_d = \frac{g_m V_i r_d}{r_d + g_m R_s r_d + R_s + R_D} \quad -⑤$$

$$V_o = -I_d R_D$$

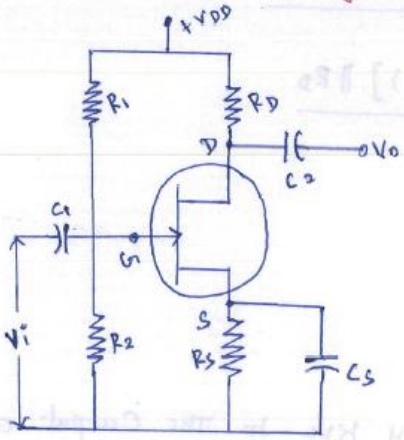
$$= \frac{-g_m V_i r_d R_D}{r_d + g_m R_s r_d + R_s + R_D}$$

$$\therefore A_v = \frac{V_o}{V_i} = \frac{-g_m V_i r_d R_D}{r_d + g_m R_s r_d + R_s + R_D} \Big/ V_i = \frac{-g_m r_d R_D}{r_d \left[1 + g_m R_s + \frac{R_s + R_D}{r_d}\right]}$$

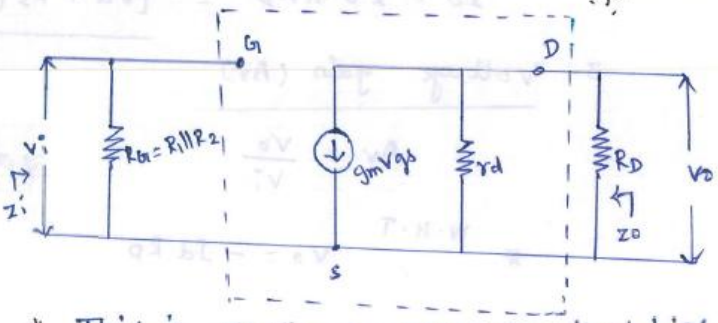
$$A_v = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}} \quad \because r_d >> R_s + R_D$$

$$\boxed{A_v = \frac{-g_m R_D}{1 + g_m R_s}} \quad ⑥$$

4. JFET with Voltage Divider Bias (Bypassed R_S)



Ac Equivalent circuit :- ·X· 2 Mark



* This is similar to JFET with fixed bias.

1. Input Impedance (Z_i)

$$Z_i = R_G = R_1 \| R_2$$

2. Output Impedance (Z_o)

$$Z_o = r_d \| R_D$$

if $r_d \gg R_D$

$$Z_o \simeq R_D$$

4. Voltage Gain (A_V)

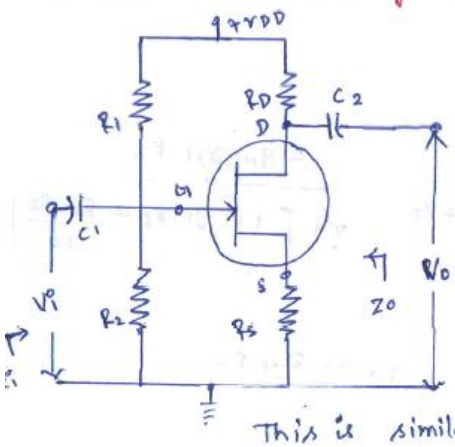
$$A_V = -g_m (r_d \| R_D)$$

if $r_d \gg R_D$

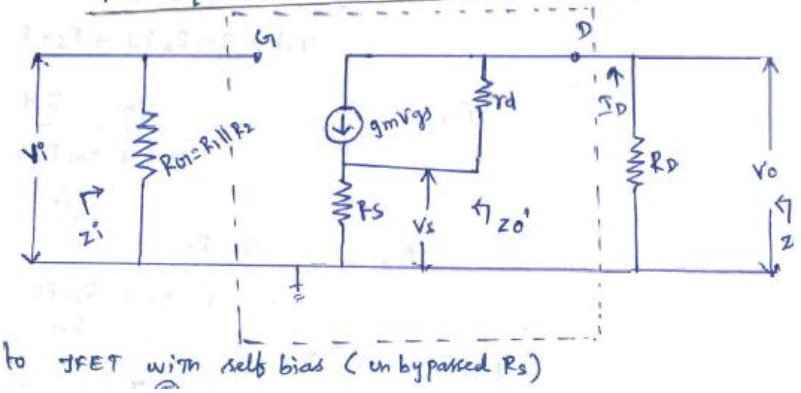
$$A_V = -g_m R_D$$

* Negative sign indicate the 180° phase shift between the input & output Voltages.

5. JFET with Voltage Divider Bias (Unbypassed R_S)



Ac Equivalent Circuit :- ·X· 2 Mark



This is similar to JFET with self bias (unbypassed R_S)

1. Input Impedance (z_i)

$$z_i = R_G = R_1 \| R_2$$

2. Output Impedance (z_o)

$$z_o' = r_d + g_m R_s r_d + R_s \quad (or) \quad z_o' = r_d + R_s(\mu+1)$$

$$z_o = [r_d + g_m R_s r_d + R_s] \| R_D \quad (or) \quad z_o = [r_d + R_s(\mu+1)] \| R_D$$

3. Voltage gain (A_V)

$$A_V = \frac{-g_m R_D}{1 + g_m R_s + \frac{R_s + R_D}{r_d}} \quad (or) \quad A_V = \frac{-g_m R_D}{1 + g_m R_s}$$

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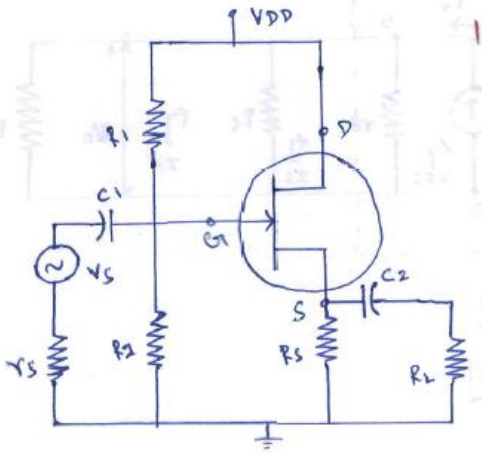
2. Common Drain circuit Analysis / Source Follower



1. JFET with voltage divider bias

* The output voltage developed across the source resistor (R_s).

* The External load (R_L) is capacitively coupled to the Source Terminal & The gate voltage (V_G) is derived from V_{DD} by means of voltage divider resistors R_1 & R_2.

* No resistor is connected in series with the drain terminal & no source bypass capacitor is employed.

* V_G is constant & the source voltage is

$$V_s = V_G + V_{GS}$$

* When an ac signal is applied to the gate via capacitor C_1, the V_G is increased & decreased as the instantaneous level of the signal voltage raises & falls.

* V_{GS} remains substantially constant, so the V_s increases & decreases with the V_G.