



SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution



Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A+' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

16EC303–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 1 –MOS TRANSISTOR PRINCIPLE

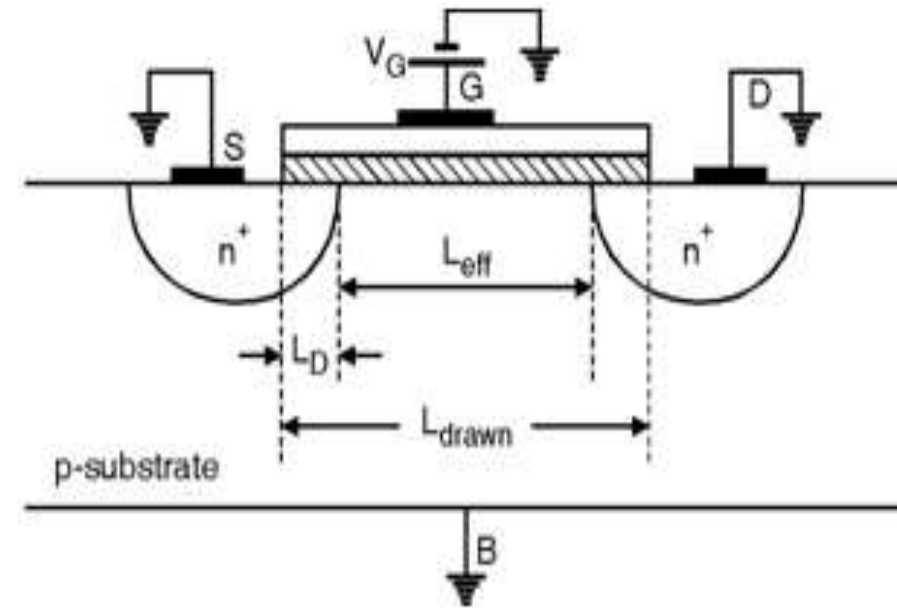
TOPIC 7 –CV CHARACTERISTICS



MOS C-V CHARACTERISTICS



- ❖ Consider the terminal connections of n-channel MOSFET which consists of $V_S = 0$, $V_D = 0$ and $V_B = 0$ and a bias is applied to the gate terminal. Depending upon the gate bias there are different regions of operation in C-V curve that are accumulation, depletion and strong inversion.



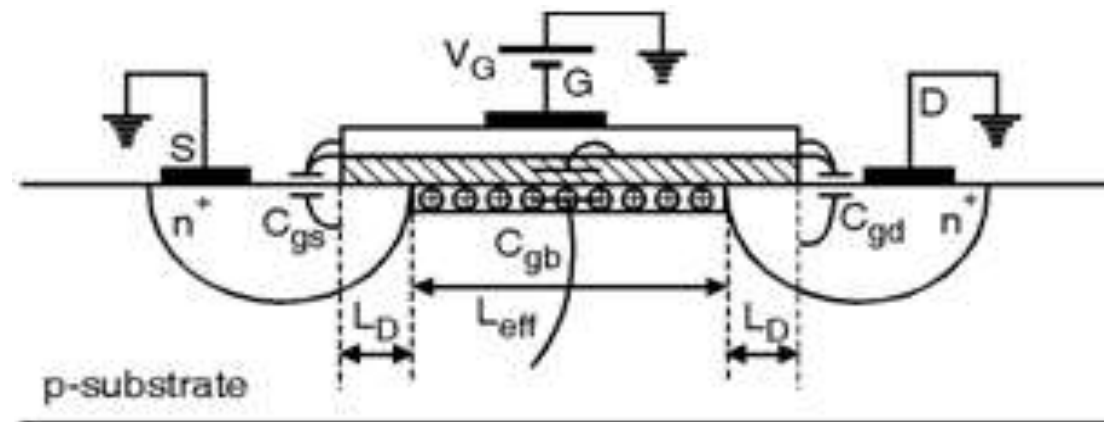
NMOS terminal connections for C-V characteristics



Accumulation Region



- In this region of operation the gate to source bias is negative because of this the holes from the substrate are attracted under the gate region



MOSFET in accumulation



Accumulation Region



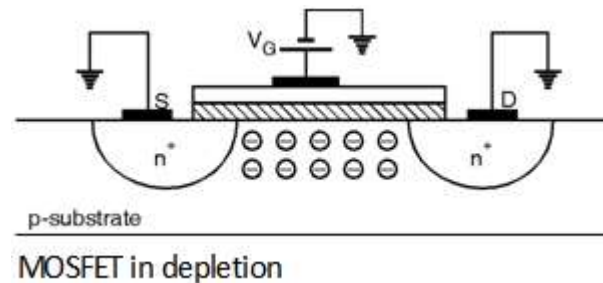
- There are three types of capacitances
 1. capacitance between gate electrode and substrate (C_{gb})
 2. capacitance between gate and drain terminals (C_{gd})
 3. capacitance between gate and source terminals (C_{gs}).
- If t_{ox} is the oxide thickness the C_{gb} is given as $C_{gb} = \frac{\epsilon_{ox} \epsilon_0 W L_{drawn}}{t_{ox}}$
Where ϵ_{ox} is dielectric constant of the gate oxide,
 W is the drawn width and
 $L_{drawn} - 2L_D$ is the effective channel length,
 L_D is lateral diffusion length and L_{drawn} is actual design length.
The capacitance between gate and drain is given by, $C_{gd} = \frac{\epsilon_{ox} \epsilon_0 W L_{drawn}}{t_{ox}}$
The C_{gd} is also called as gate-drain overlap capacitance.
Similarly the capacitance between gate and source is given by $C_{gs} = \frac{\epsilon_{ox} \epsilon_0 W L_{drawn}}{t_{ox}}$
The C_{gs} is also called as gate-source overlap capacitance.
The total capacitance of MOSFET between gate and ground is the sum of C_{gd} , C_{gs} and C_{gb} and is given by, $C_{ox} = \frac{\epsilon_{ox} \epsilon_0 W L_{drawn}}{t_{ox}}$



Depletion Region



- Consider the case that V_{GS} is positive but less than V_{TH} for some terminal biases shown in Figure below.
- Under these conditions the surface under the gate is depleted because as the holes under the gate are displaced and leave negative immobile ions that contribute to negative charge as shown in Fig. 3.6.3.
- In this region of operation the capacitance between the gate and the source/drain is simply overlap capacitance while the capacitance between the gate and substrate is the oxide capacitance in series with depletion capacitance of the formed depletion region.
- The MOSFET operated in this region is said to be in weak inversion or the sub threshold region.

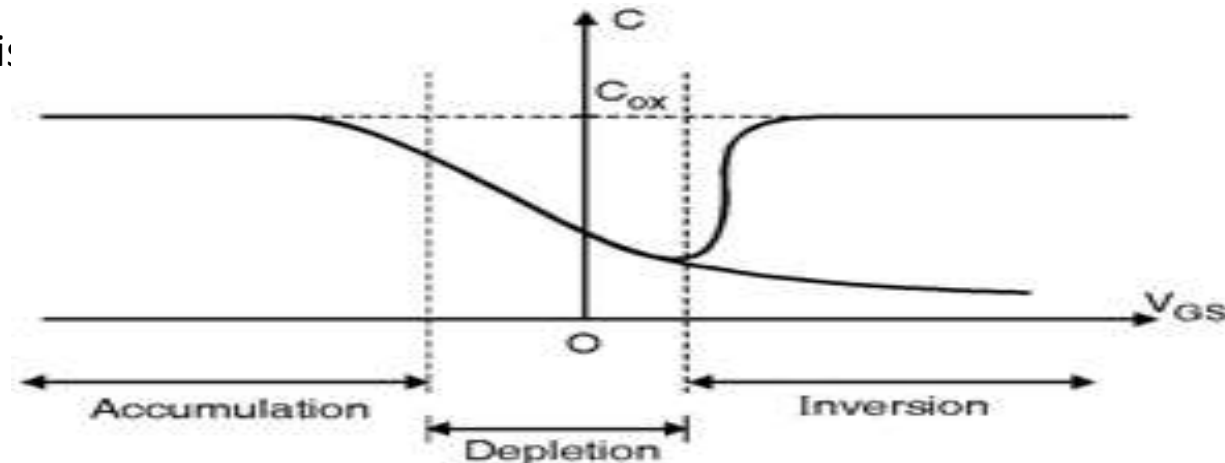




Strong Inversion Region



- When V_{GS} is sufficiently positive and is larger than V_{TH} then a large number of electrons are attracted under the gate and the surface is said to be inverted.
- MOSFET makes a very good capacitor when $V_{GS} > V_{TH} + \text{few hundred mV}$. In integrated circuits the capacitor based on MOSFETs are designed in this region of operation.
- The complete C-V characteristics are shown in Figure below.



C-V characteristics of MOSFET



Thank You