SNS COLLEGE OF TECHNOLOGY

Coimbatore-35
An Autonomous Institution

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DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

16EC303–VLSI DESIGN

III YEAR/ V SEMESTER

UNIT 1 –MOS TRANSISTOR PRINCIPLE

TOPIC 6 –MOS- NON IDEAL IV CHARACTERISTICS

OUTLINE

- TRANSISTOR I-V REVIEW
- NONIDEAL TRANSISTOR BEHAVIOR
  - VELOCITY SATURATION
  - CHANNEL LENGTH MODULATION
  - BODY EFFECT
  - LEAKAGE
  - TEMPERATURE SENSITIVITY
  - ACTIVITY
- PROCESS AND ENVIRONMENTAL VARIATIONS
  - PROCESS CORNERS
- ASSESSMENT
- SUMMARY

IDEAL TRANSISTOR I-V

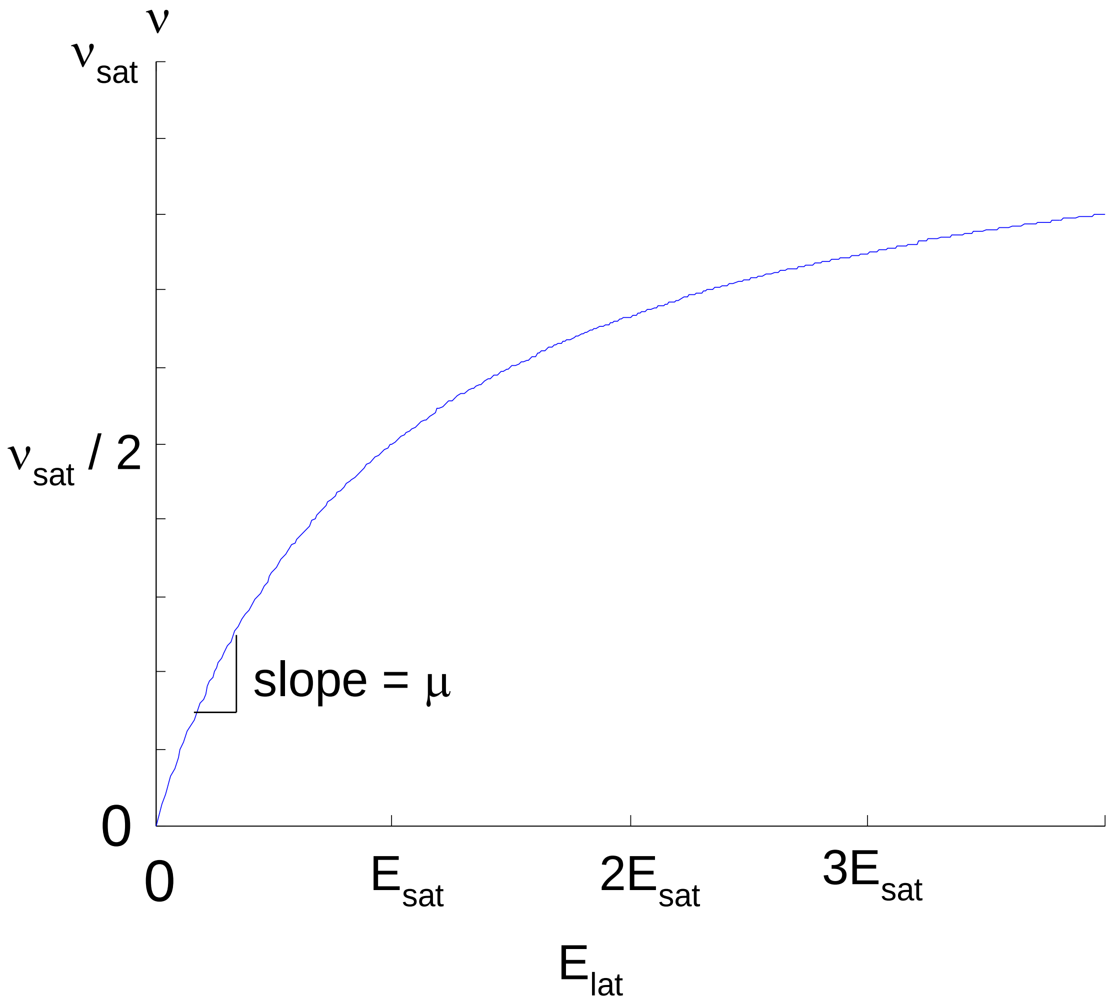
Shockley 1st order transistor models

Y

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ \beta\left(V_{gs} - V_t - {}^{V_{ds}}\!/_{2}\right)V_{ds} & V_{ds} < V_{dsat} & \text{linear} \\ \dfrac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

VELOCITY SATURATION

- We assumed carrier velocity is proportional to E-field
  - $v = \mathrm{mE_{lat}} = \mathrm{mV_{ds}/L}$
- At high fields, this ceases to be true
  - Carriers scatter off atoms
  - Velocity reaches v_{sat}
    - Electrons: 6-10 x 10^6 cm/s
    - Holes: 4-8 x 10^6 cm/s
  - Better model



VELOCITY SATURATION I-V EFFECTS

- Ideal transistor ON current increases with V_{DD}^2

$$I_{ds} = \mu C_{ox} \frac{W}{L} \frac{(V_{gs} - V_t)^2}{2} = \frac{\beta}{2}(V_{gs} - V_t)^2$$

- Velocity-saturated ON current increases with V_{DD}

$$I_{ds} = C_{ox} W \left(V_{gs} - V_t\right) v_{max}$$

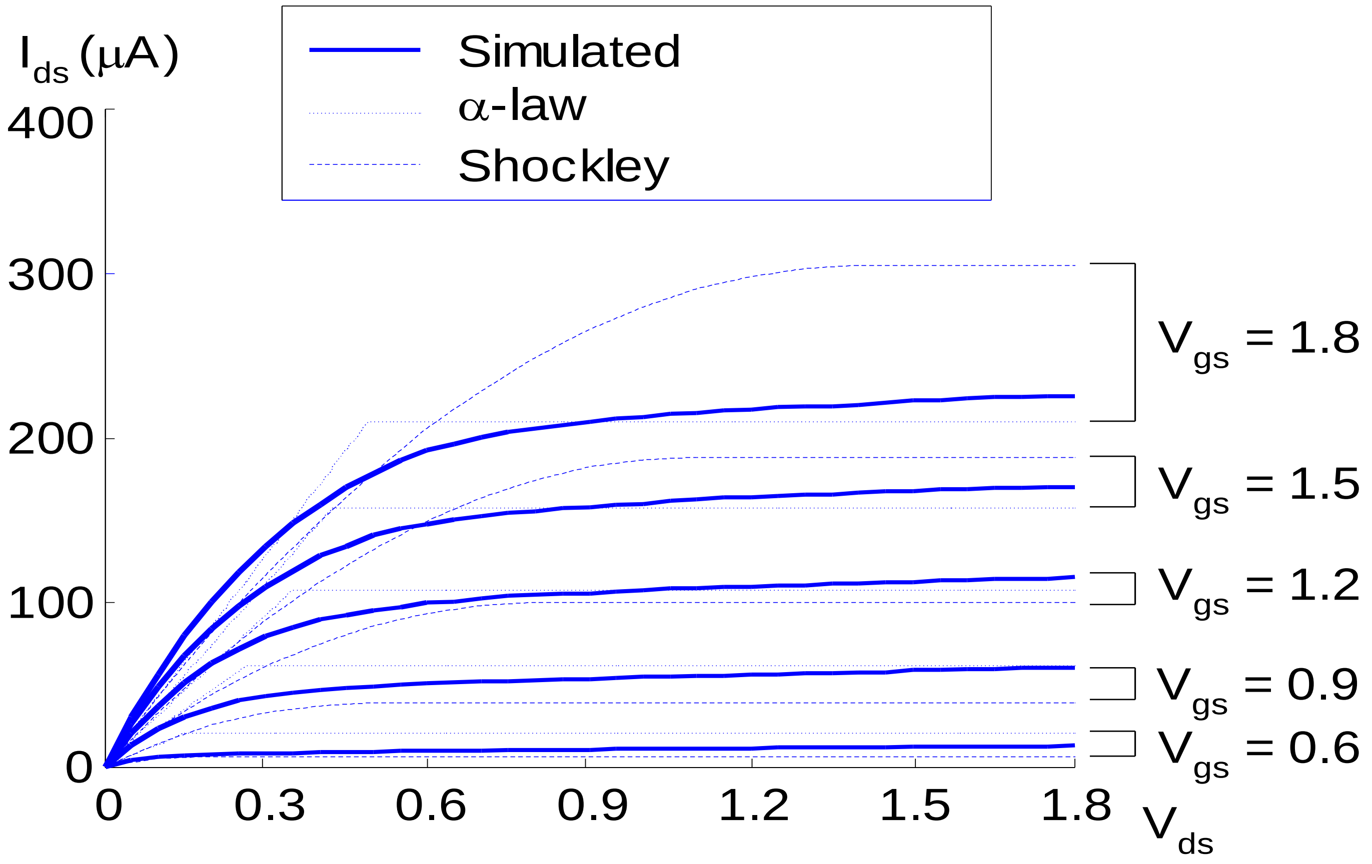
- Real transistors are partially velocity saturated
  - Approximate with a-power law model
  - $I_{ds} \propto V_{DD}^a$
  - $1 < a < 2$ determined empirically

α- POWER MODEL

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{cutoff} \\ I_{dsat} \dfrac{V_{ds}}{V_{dsat}} & V_{ds} < V_{dsat} & \text{linear} \\ I_{dsat} & V_{ds} > V_{dsat} & \text{saturation} \end{cases}$$

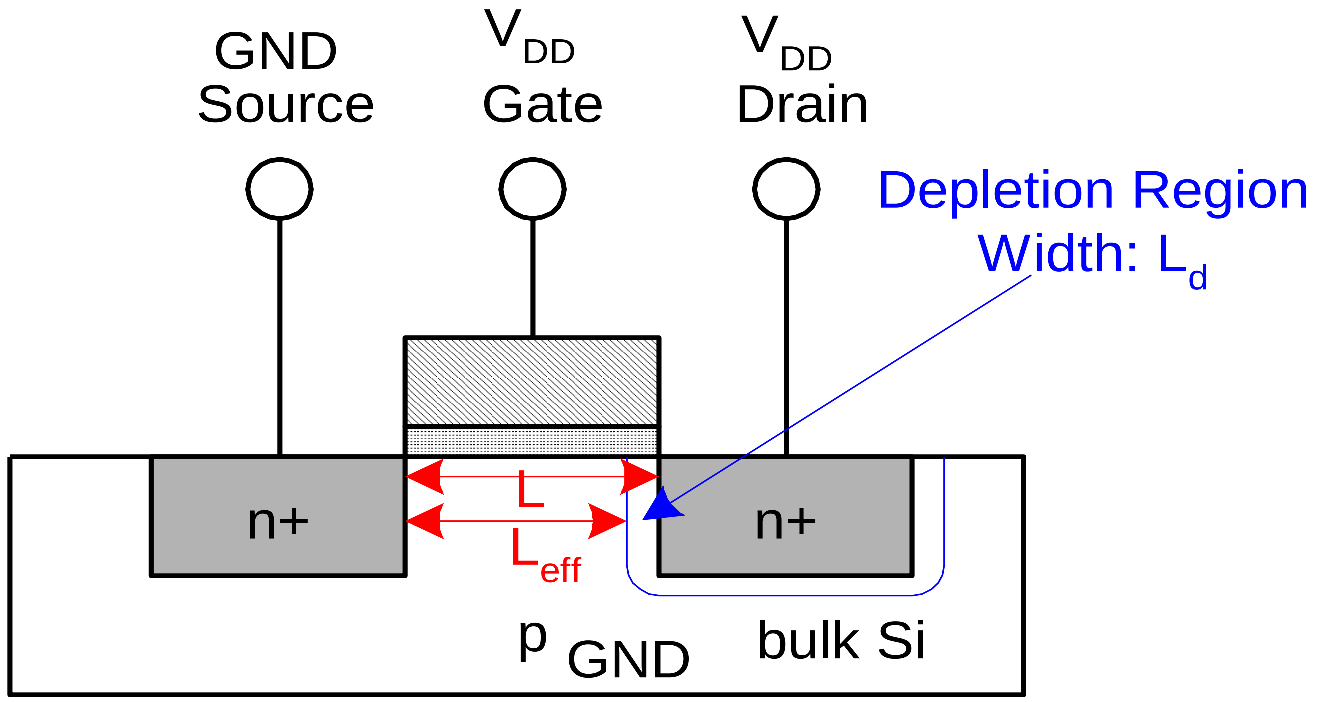
$$I_{dsat} = P_c \frac{\beta}{2} \left(V_{gs} - V_t\right)^{\alpha}$$

$$V_{dsat} = P_v \left(V_{gs} - V_t\right)^{\alpha/2}$$



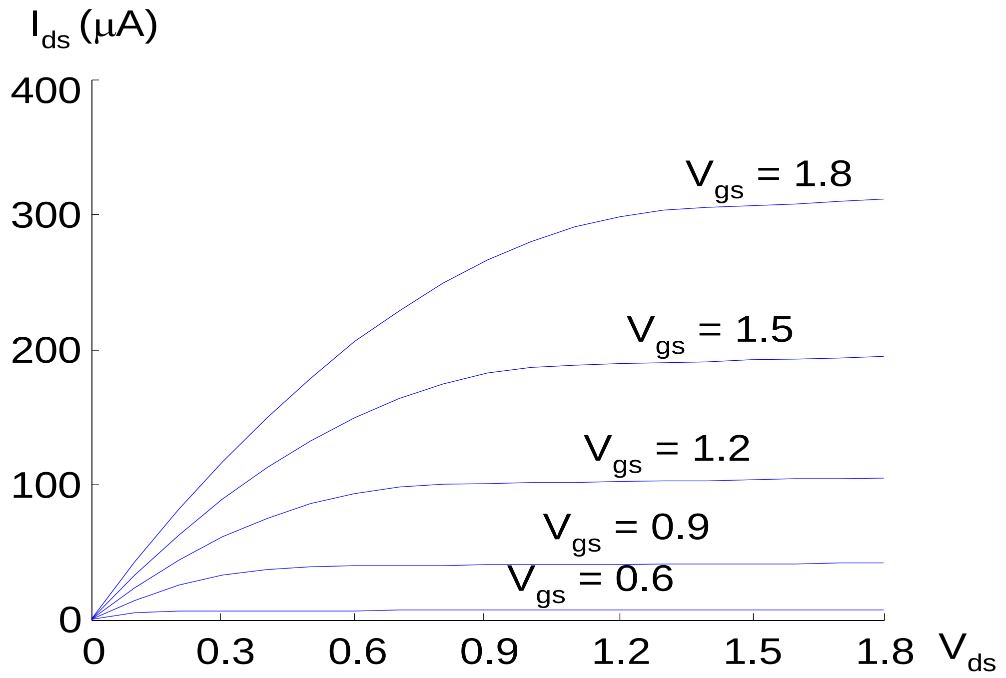
CHANNEL LENGTH MODULATION

- Reverse-biased p-n junctions form a depletion region
  - –Region between n and p with no carriers
  - –Width of depletion L_d region grows with reverse bias
  - –$L_{eff} = L – L_d$
- Shorter L_{eff} gives more current
  - –I_{ds} increases with V_{ds}
  - –Even in saturation



CHAN.LENGTH MOD I-V

$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 \left(1 + \lambda V_{ds}\right)$$



λ = channel length modulation coefficient

- not feature size
- Empirically fit to I-V characteristics

BODY EFFECT & BODY EFFECT MODEL

- V_t: gate voltage necessary to invert channel
- Increases if source voltage increases because source is connected to the channel
- Increase in V_t with V_s is called the body effect

$$V_t = V_{t0} + \gamma\left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s}\right)$$

- f_s = *surface potential* at threshold

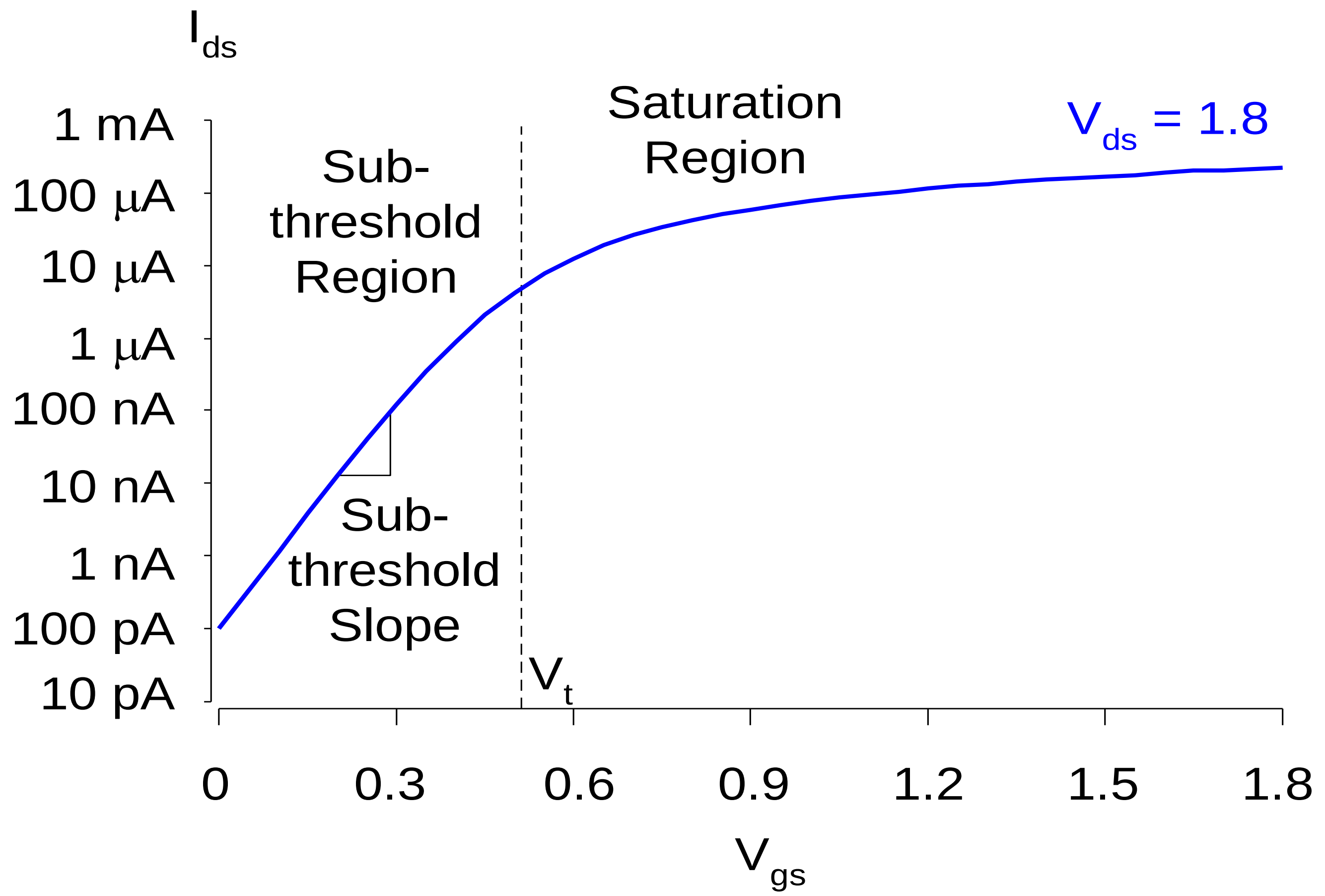
$$\phi_s = 2v_T \ln \frac{N_A}{n_i}$$

  - Depends on doping level N_A
  - intrinsic carrier concentration n_i
- γ = body effect coefficient

$$\gamma = \frac{t_{\mathrm{ox}}}{\varepsilon_{\mathrm{ox}}}\sqrt{2\mathrm{q}\varepsilon_{\mathrm{si}}N_A} = \frac{\sqrt{2\mathrm{q}\varepsilon_{\mathrm{si}}N_A}}{C_{\mathrm{ox}}}$$

OFF TRANSISTOR BEHAVIOR

- What about current in cutoff?
- Simulated results
- What differs?
  - Current doesn't go to 0 in cutoff



LEAKAGE SOURCES

- Subthreshold conduction
  - Transistors can’t abruptly turn ON or OFF
- Junction leakage
  - Reverse-biased PN junction diode current
- Gate leakage
  - Tunneling through ultrathin gate dielectric

- Subthreshold leakage is the biggest source in modern transistors

ACTIVITY

Quick! Count the number of times that the letter F appears in the following sentence:

“Finished files are the result of years of scientific study combined with the experience of years.”

SUBTHRESHOLD LEAKAGE

- Subthreshold leakage exponential with V_{gs}

$$I_{ds} = I_{ds0} e^{\frac{V_{gs}-V_t}{nv_T}} \left(1 - e^{\frac{-V_{ds}}{v_T}}\right) \qquad I_{ds0} = \beta v_T^2 e^{1.8}$$

- n is process dependent, typically 1.4-1.5

DRAIN-INDUCED BARRIER LOWERING
DIBL

- Drain-Induced Barrier Lowering
  - Drain voltage also affect V_t

$$V_t' = V_t - \eta V_{ds}$$

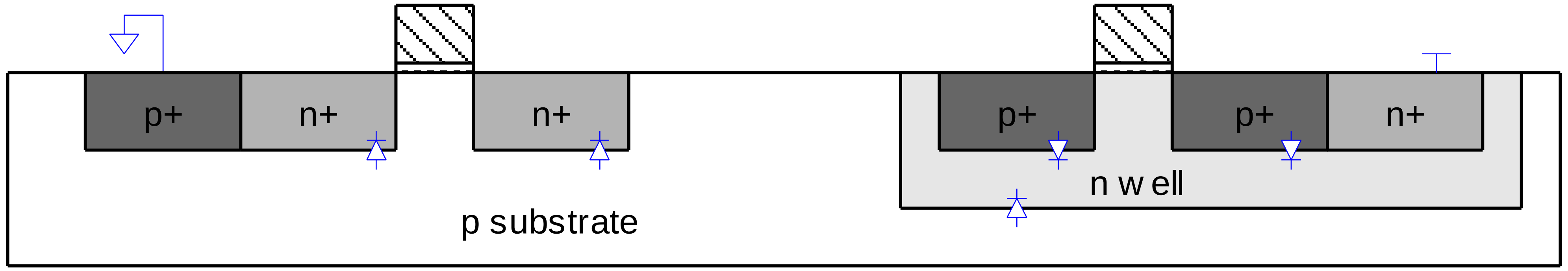
  - High drain voltage causes sub threshold leakage to increase.

JUNCTION LEAKAGE

- Reverse-biased p-n junctions have some leakage

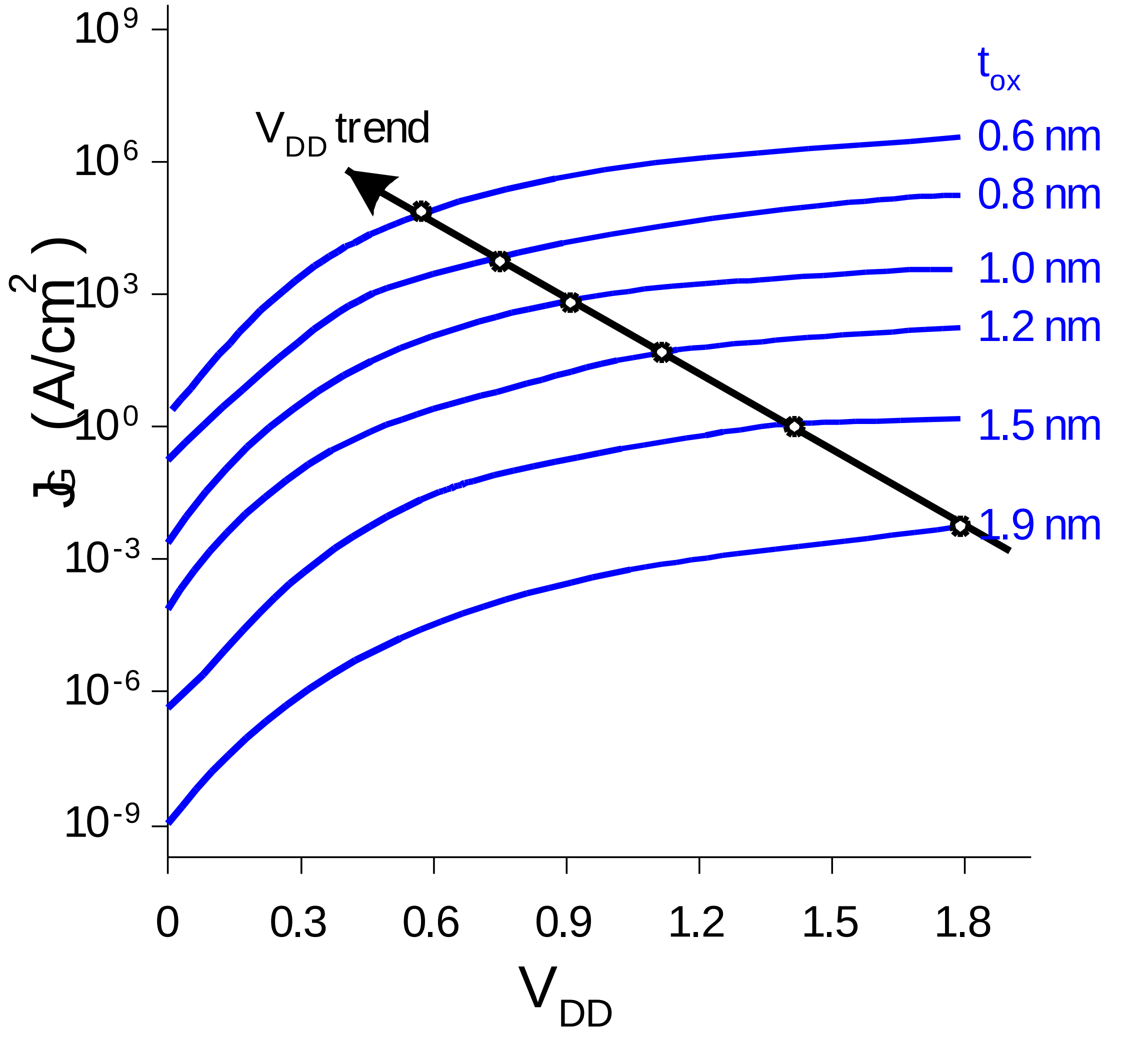
$$I_D = I_S\left(e^{\frac{V_D}{v_T}} - 1\right)$$

- I_s depends on doping levels
  - –And area and perimeter of diffusion regions
  - –Typically < 1 fA/mm^2



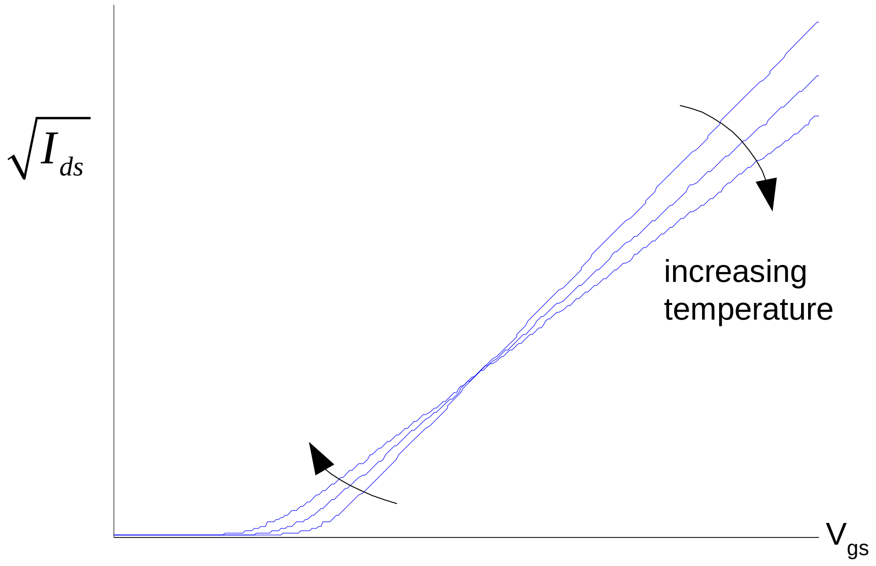
GATE LEAKAGE

- Carriers may tunnel thorough very thin gate oxides
- Predicted tunneling current
- Negligible for older processes
- May soon be critically important



TEMPERATURE SENSITIVITY

- Increasing temperature
  - Reduces mobility
  - Reduces V_t
- I_{ON} decreases with temperature
- I_{OFF} increases with temperature

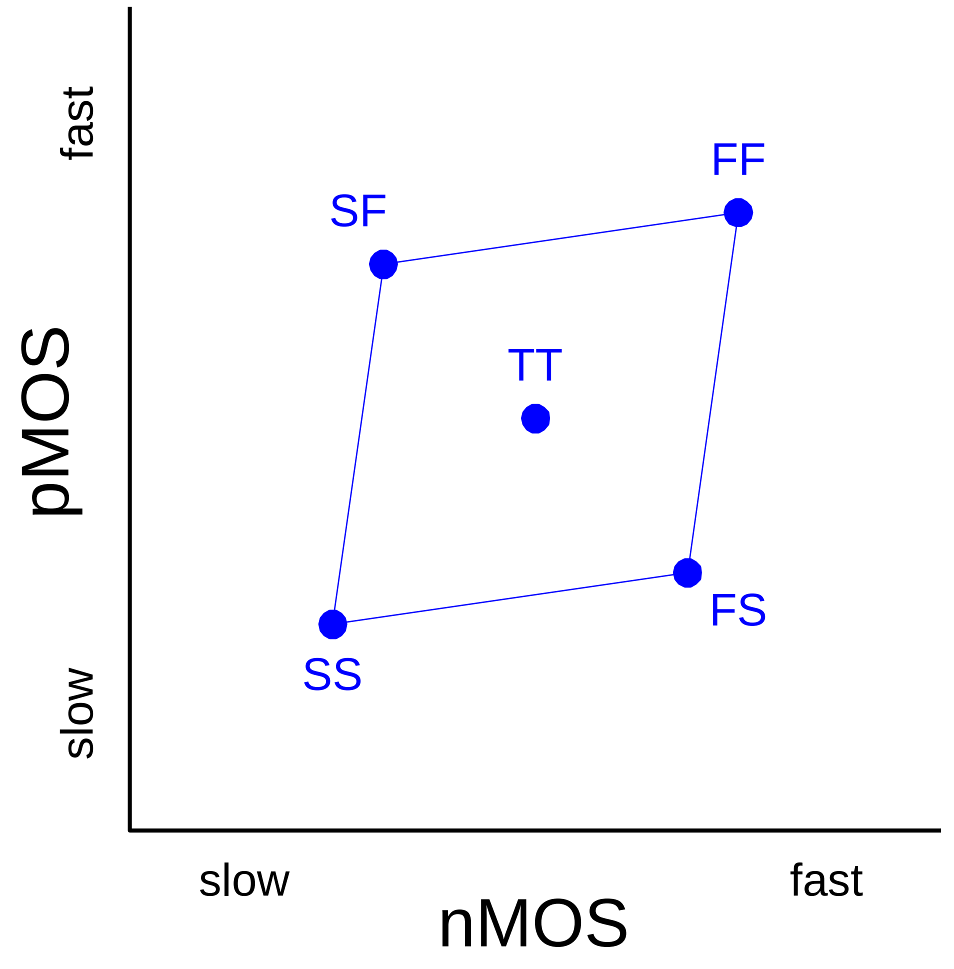


SO WHAT?

- So what if transistors are not ideal?
  - They still behave like switches.
- But these effects matter for…
  - Supply voltage choice
  - Logical effort
  - Quiescent power consumption
  - Pass transistors
  - Temperature of operation

PARAMETER VARIATION

- Transistors have uncertainty in parameters
  - Process: L_{eff}, V_t, t_{ox} of nMOS and pMOS
  - Vary around typical (T) values
- Fast (F)
  - L_{eff}: short
  - V_t: low
  - t_{ox}: thin
- Slow (S): opposite
- Not all parameters are independent for nMOS and pMOS



ENVIRONMENTAL VARIATION

- V_{DD} and T also vary in time and space
- Fast:
  - –V_{DD}: high
  - –T: low

Corner	Voltage	Temperature
F	1.98	0 C
T	1.8	70 C
S	1.62	125 C

PROCESS CORNERS

- Process corners describe worst case variations
  - If a design works in all corners, it will probably work for any variation.
- Describe corner with four letters (T, F, S)
  - nMOS speed
  - pMOS speed
  - Voltage
  - Temperature

IMPORTANT CORNERS

Some critical simulation corners include

Purpose	**nMOS**	**pMOS**	**V_{DD}**	**Temp**
Cycle time	S	S	S	S
Power	F	F	F	F
Subthrehold leakage	F	F	F	S
Pseudo-nMOS	S	F	?	?

ASSESSMENT

1.Write the CHANNEL LENGTH MODULATION equation

2. Write the body effect derivation with its factors

3.In parameter Variation

- Fast (F)
  - L_{eff}: ---------------- V_t: ---------------- t_{ox}: ---------------

4.

Purpose	nMOS	pMOS	V_{DD}	Temp
Cycle time	?	?	?	?
Power	?	?	?	?
Subthrehold leakage	?	?	?	?
Pseudo-nMOS	?	?	?	?

SUMMARY & THANK YOU