SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

PIC16F877-Addressing Modes

Dr.G.Arthy
Assistant Professor
Department of EEE
SNS College of Engineering

Addressing Modes of PIC16F877

- 1. Immediate addressing mode
- 2. Register operand addressing mode
- 3. Memory operand addressing mode
- 4. Direct addressing
- 5. Indirect addressing.

Immediate addressing mode

The operand is a number or constant not an address.

Example:

MOVLW 32h

ADDLW 12h

Register operand addressing mode

The operand is a Register which holds the data to be executed.

Example: CLR W

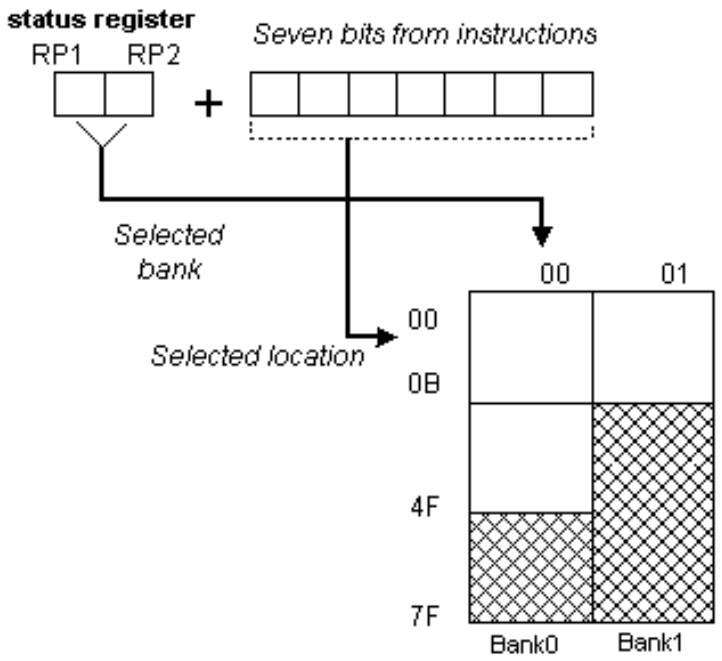
Memory operand addressing mode

The operand is an address of Memory location which holds the data to be executed.

Example: CLRF 13h

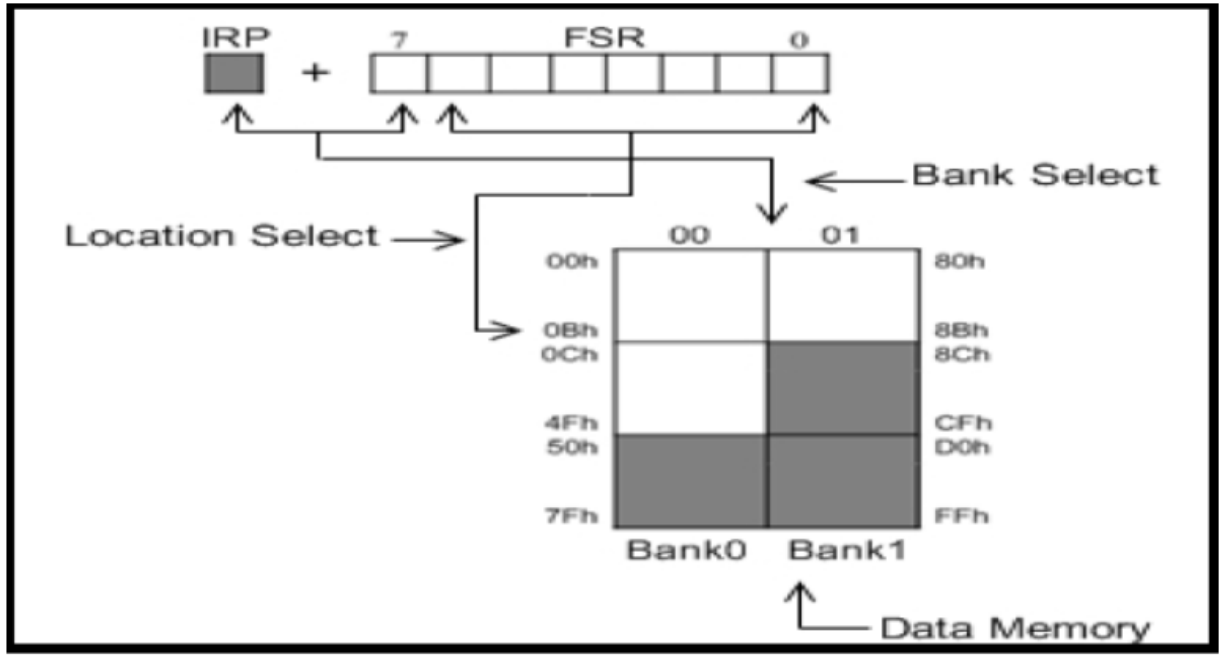
Direct Addressing

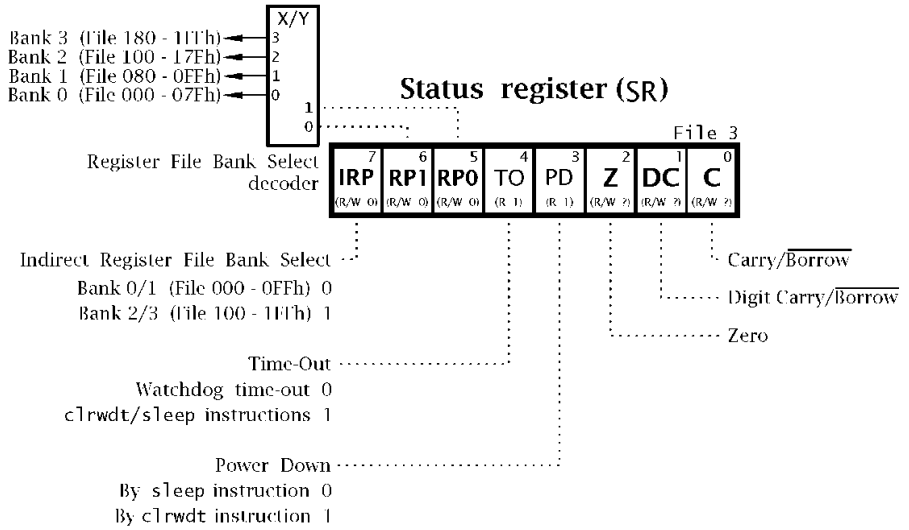
- ✓ Direct Addressing is done through a 9-bit address.
- ✓ This address is obtained by connecting 7th bit of direct address.
- ✓ By using an instruction with two bits (RP1, RP0) from STATUS register bank is selected



Indirect Addressing

- ✓ It does not take an address from an instruction.
- ✓ But it derives from IRP bit of STATUS and FSR registers.
- ✓ Addressed location is accessed through INDF register.





Example

ADDWF INDF

Special Function Registers

Uses a series of “Special Function Registers” for controlling peripherals and PIC behaviours.

- ✓ STATUS → Bank select bits, ALU bits (zero, borrow, carry)
- ✓ INTCON → Interrupt control: interrupt enables, flags, etc.
- ✓ OPTION_REG → contains various control bits to configure the TMR0 prescaler/WDT postscaler ,the External INT Interrupt, TMR0 and the weak pullups on PORTB

DATA MEMORY

Bank 0	File Address	Bank 1	File Address	Bank 2	File Address	Bank 3	File Address
Indirect addr.(*)	00h	Indirect addr.(*)	80h	Indirect addr.(*)	100h	Indirect addr.(*)	180h
TMR0	01h	OPTION_REG	81h	TMR0	101h	OPTION_REG	181h
PCL	02h	PCL	82h	PCL	102h	PCL	182h
STATUS	03h	STATUS	83h	STATUS	103h	STATUS	183h
FSR	04h	FSR	84h	FSR	104h	FSR	184h
PORTA	05h	TRISA	85h		105h		185h
PORTB	06h	TRISB	86h	PORTB	106h	TRISB	186h
PORTC	07h	TRISC	87h		107h		187h
PORTD(1)	08h	TRISD(1)	88h		108h		188h
PORTE(1)	09h	TRISE(1)	89h		109h		189h
PCLATH	0Ah	PCLATH	8Ah	PCLATH	10Ah	PCLATH	18Ah
INTCON	0Bh	INTCON	8Bh	INTCON	10Bh	INTCON	18Bh
PIR1	0Ch	PIE1	8Ch	EEDATA	10Ch	EECON1	18Ch
PIR2	0Dh	PIE2	8Dh	EEADR	10Dh	EECON2	18Dh
TMR1L	0Eh	PCON	8Eh	EEDATH	10Eh	Reserved(2)	18Eh
TMR1H	0Fh		8Fh	EEADRH	10Fh	Reserved(2)	18Fh
T1CON	10h		90h		110h		190h
TMR2	11h	SSPCON2	91h		111h		191h
T2CON	12h	PR2	92h		112h		192h
SSPBUF	13h	SSPADD	93h		113h		193h
SSPCON	14h	SSPSTAT	94h		114h		194h
CCPR1L	15h		95h		115h		195h
CCPR1H	16h		96h		116h		196h
CCP1CON	17h		97h	General Purpose Register 16 Bytes	117h	General Purpose Register 16 Bytes	197h
RCSTA	18h	TXSTA	98h		118h		198h
TXREG	19h	SPBRG	99h		119h		199h
RCREG	1Ah		9Ah		11Ah		19Ah
CCPR2L	1Bh		9Bh		11Bh		19Bh
CCPR2H	1Ch		9Ch		11Ch		19Ch
CCP2CON	1Dh		9Dh		11Dh		19Dh
ADRESH	1Eh	ADRESL	9Eh		11Eh		19Eh
ADCON0	1Fh	ADCON1	9Fh		11Fh		19Fh
	20h		A0h		120h		1A0h
General Purpose Register 96 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes		General Purpose Register 80 Bytes	
	7Fh	accesses 70h-7Fh	EFh F0h FFh	accesses 70h-7Fh	16Fh 170h 17Fh	accesses 70h - 7Fh	1EFh 1F0h 1FFh

Unimplemented data memory locations, read as '0'.
* Not a physical register.

Note 1: These registers are not implemented on the PIC16F876.
2: These registers are reserved, maintain these registers clear.

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR
Bank 0										
00h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000
01h	TMR0	Timer0 Module Register								xxxx xxxx
02h(3)	PCL	Program Counter (PC) Least Significant Byte								0000 0000
03h(3)	STATUS	IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	0001 1xxx
04h(3)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
05h	PORTA	—	—	PORTA Data Latch when written: PORTA pins when read						--0x 0000
06h	PORTB	PORTB Data Latch when written: PORTB pins when read								xxxx xxxx
07h	PORTC	PORTC Data Latch when written: PORTC pins when read								xxxx xxxx
08h(4)	PORTD	PORTD Data Latch when written: PORTD pins when read								xxxx xxxx
09h(4)	PORTE	—	—	—	—	—	RE2	RE1	RE0	---- -xxx
0Ah(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000
0Bh(3)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
0Ch	PIR1	PSPIF(3)	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000
0Dh	PIR2	—	(5)	—	EEIF	BCLIF	—	—	CCP2IF	-r-0 0--0
0Eh	TMR1L	Holding register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx
0Fh	TMR1H	Holding register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000
11h	TMR2	Timer2 Module Register								0000 0000
12h	T2CON	—	TOUTPS3	TOUTPS2	TOUTPS1	TOUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000
13h	SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx
14h	SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000
15h	CCPR1L	Capture/Compare/PWM Register1 (LSB)								xxxx xxxx
16h	CCPR1H	Capture/Compare/PWM Register1 (MSB)								xxxx xxxx
17h	CCP1CON	—	—	CCP1X	CCP1Y	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x
19h	TXREG	USART Transmit Data Register								0000 0000
1Ah	RCREG	USART Receive Data Register								0000 0000
1Bh	CCPR2L	Capture/Compare/PWM Register2 (LSB)								xxxx xxxx
1Ch	CCPR2H	Capture/Compare/PWM Register2 (MSB)								xxxx xxxx
1Dh	CCP2CON	—	—	CCP2X	CCP2Y	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000
1Eh	ADRESH	A/D Result Register High Byte								xxxx xxxx
1Fh	ADCON0	ADCS1	ADCS0	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	—	ADON	0000 00-0

TABLE 2-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR
Bank 1										
80h(3)	INDF	Addressing this location uses contents of FSR to address data memory (not a physical register)								0000 0000
81h	OPTION_REG	$\overline{\text{RBPU}}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111
82h(3)	PCL	Program Counter (PC) Least Significant Byte								0000 0000
83h(3)	STATUS	IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx
84h(3)	FSR	Indirect Data Memory Address Pointer								xxxx xxxx
85h	TRISA	—	—	PORTA Data Direction Register						--11 1111
86h	TRISB	PORTB Data Direction Register								1111 1111
87h	TRISC	PORTC Data Direction Register								1111 1111
88h(4)	TRISD	PORTD Data Direction Register								1111 1111
89h(4)	TRISE	IBF	OBF	IBOV	PSPMODE	—	PORTE Data Direction Bits			0000 -111
8Ah(1,3)	PCLATH	—	—	—	Write Buffer for the upper 5 bits of the Program Counter					---0 0000
8Bh(3)	INTCON	GIE	PEIE	T0IE	INTE	RBIE	T0IF	INTF	RBIF	0000 000x
8Ch	PIE1	PSPIE(2)	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000
8Dh	PIE2	—	(5)	—	EEIE	BCLIE	—	—	CCP2IE	-r-0 0--0
8Eh	PCON	—	—	—	—	—	—	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	---- --qq
8Fh	—	Unimplemented								—
90h	—	Unimplemented								—
91h	SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000
92h	PR2	Timer2 Period Register								1111 1111
93h	SSPADD	Synchronous Serial Port (I^2C mode) Address Register								0000 0000
94h	SSPSTAT	SMP	CKE	D/$\overline{\text{A}}$	P	S	R/$\overline{\text{W}}$	UA	BF	0000 0000
95h	—	Unimplemented								—
96h	—	Unimplemented								—
97h	—	Unimplemented								—
98h	TXSTA	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010
99h	SPBRG	Baud Rate Generator Register								0000 0000
9Ah	—	Unimplemented								—
9Bh	—	Unimplemented								—
9Ch	—	Unimplemented								—
9Dh	—	Unimplemented								—
9Eh	ADRESL	A/D Result Register Low Byte								xxxx xxxx
9Fh	ADCON1	ADFM	—	—	—	PCFG3	PCFG2	PCFG1	PCFG0	0--- 0000

File Address	Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit2	Bit 1	Bit 0	Value on Power-On Reset	Value on Other Resets
Bank 0											
0x00	INDF	Uses contents of FSR to address data memory (not a physical register)								---- ----	---- ----
0x01	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
0x02	PCL	Least Significant 8 bits of the Program Counter (PC)								0000 0000	0000 0000
		b7	b6	b5	b4	b3	b2	b1	b0		
0x03	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	000q quuu
0x04	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
0x05	PORTA	-	-	-	RA4/ T0CKI	RA3	RA2	RA1	RA0	---x xxxx	---u uuuu
0x06	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
0x07	Unimplemented	Unimplemented location, read as '0'								---- ----	---- ----
0x08	EEDATA	EEPROM data register								xxxx xxxx	uuuu uuuu
0x09	EEADR	EEPROM address register								xxxx xxxx	uuuu uuuu
0x0A	PCLATH	-	-	-	Most Significant 5 Bits of the PC					---0 0000	---0 0000
					b12	b11	b10	b9	b8		
0x0B	INTCON	GIE	EEIE	T0IE	INT E	RBIE	T0IF	INTF	RBIF	0000 000x	0000 000u
Bank 1											
0x80	INDF	Uses contents of FSR to address data memory (not a physical register)								---- ----	---- ----
0x81	OPTION	RBPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
0x82	PCL	Least Significant 8 bits of the Program Counter (PC)								0000 0000	0000 0000
0x83	STATUS	IRP	RP1	RP0	TO	PD	Z	DC	C	0001 1xxx	000q quuu
0x84	FSR	Indirect data memory address pointer 0								xxxx xxxx	uuuu uuuu
0x85	TRISA	-	-	-	PORTA data direction register					---1 1111	---1 1111
					b4	b3	b2	b1	b0		
0x86	TRISB	PORTB data direction register								1111 1111	1111 1111
		b7	b6	b5	b4	b3	b2	b1	b0		
0x87	Unimplemented	Unimplemented location, read as '0'								---- ----	---- ----
0x88	EECON1	-	-	-	EEIF	WRERR	WREN	WR	RD	---0 x000	---0 q000
0x89	EECON2	EEPROM control register 2 (not a physical register)								---- ----	---- ----

How Registers are called?

```
STATUS      equ 03h
TRISA       equ 85h
PORTA       equ 05h

            bsf     STATUS,5
            movlw   00h
            movwf   TRISA
            bcf     STATUS,5

Start       movlw   02h
            movwf   PORTA
            movlw   00h
            movwf   PORTA
            goto    Start
```

Special Function Registers

STATUS Register

IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C

bit 7 bit 0

bit 7 **IRP:** Register Bank Select bit (used for indirect addressing)
1 = Bank 2, 3 (100h-1FFh)
0 = Bank 0, 1 (00h-FFh)

bit 6-5 **RP1:RP0**: Register Bank Select bits (used for direct addressing)
11 = Bank 3 (180h-1FFh)
10 = Bank 2 (100h-17Fh)
01 = Bank 1 (80h-FFh)
00 = Bank 0 (00h-7Fh)
Each bank is 128 bytes.

bit 4 $\overline{\textbf{TO}}$: Time-out bit
1 = After power-up, CLRWDT instruction or SLEEP instruction
0 = A WDT time-out occurred

bit 3 $\overline{\textbf{PD}}$: Power-down bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction

bit 2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit carry/$\overline{\text{borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)
(for $\overline{\text{borrow}}$, the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0 **C**: Carry/$\overline{\text{borrow}}$ bit (ADDWF, ADDLW, SUBLW, SUBWF instructions)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Special Function Registers

SFR-INTCON Register

GIE	PEIE	TMR0IE	INTE	RBIE	TMR0IF	INTF	RBIF
bit 7							bit 0

bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all unmasked interrupts
0 = Disables all interrupts

bit 6 **PEIE**: Peripheral Interrupt Enable bit
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts

bit 5 **TMR0IE**: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 interrupt
0 = Disables the TMR0 interrupt

bit 4 **INTE**: RB0/INT External Interrupt Enable bit
1 = Enables the RB0/INT external interrupt
0 = Disables the RB0/INT external interrupt

bit 3 **RBIE**: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt

bit 2 **TMR0IF**: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow

bit 1 **INTF**: RB0/INT External Interrupt Flag bit
1 = The RB0/INT external interrupt occurred (must be cleared in software)
0 = The RB0/INT external interrupt did not occur

bit 0 **RBIF**: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state; a mismatch condition will continue to set the bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared (must be cleared in software).
0 = None of the RB7:RB4 pins have changed state

Special Function Registers
PIC Peripherals: Ports (Digital I/O)

- Ports are basically digital I/O pins which exist in all PICs

- The PIC16F877A have the following ports:
  - PORT A has 6 bit wide, Bidirectional
  - PORT B,C,D have 8 bit wide, Bidirectional
  - PORT E has 3 bit wide, Bidirectional

- Ports have 2 control registers
  - TRISx sets whether each pin is an input (1) or output (0)
  - PORTx sets their output bit levels or contain their input bit levels

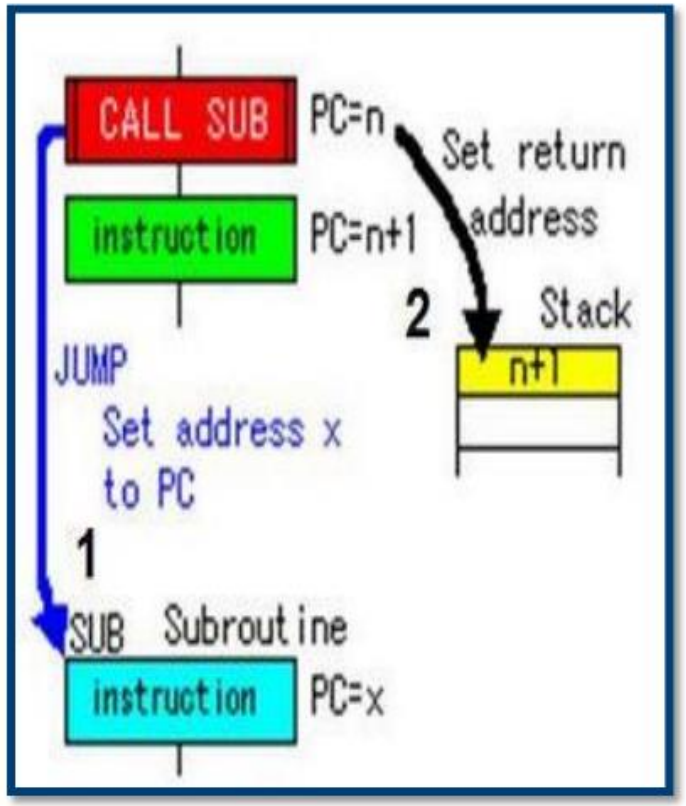
- Pin functionality “overloaded” with other features
- Most pins have 25mA source/sink thus it can drive LEDs directly

Stack & Subroutine

Instructions for subroutine and stack:

call k:

- Call subroutine.
- k: literal field.
- the function:
  1. Jump to the subroutine after call.
  2. Add 1 to PC and save the result in stack.
  3. No change in flags.
  4. Has 2 cycles.

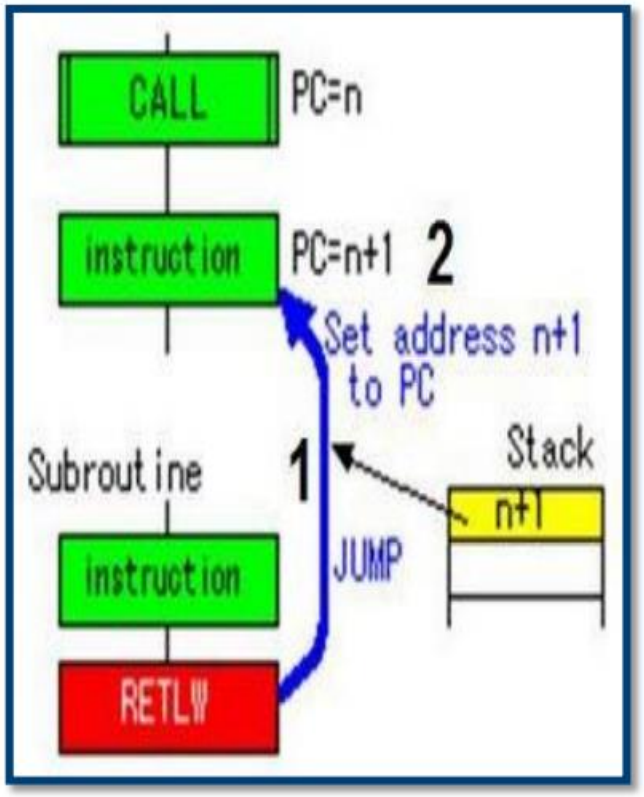


Stack & Subroutine

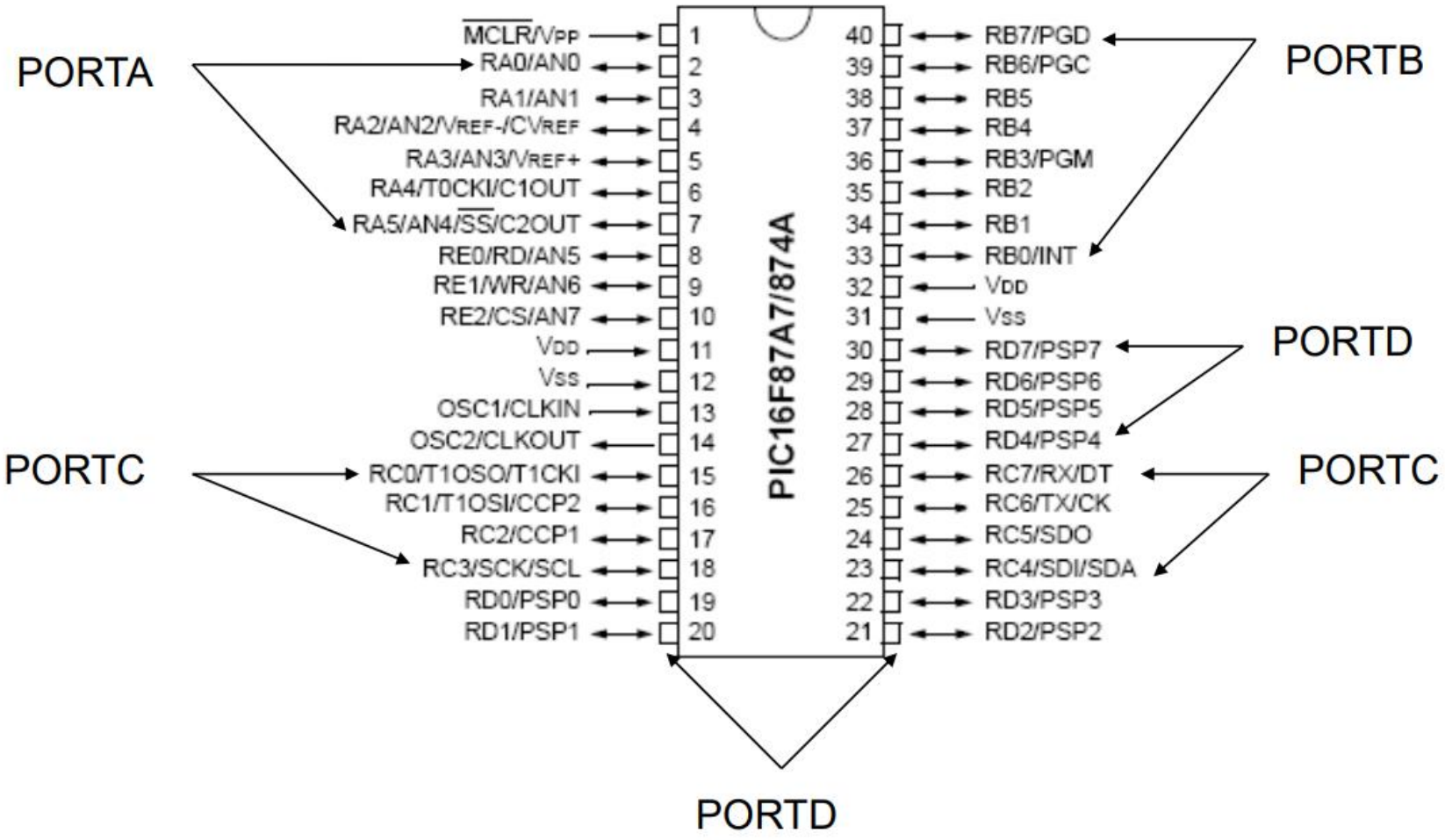
Instructions for subroutine and stack:

return -:

- Return from subroutine.
- No operand.
- the function:
  1. Return without any condition from the subroutine.
  2. Upload the final value of the PC was saved in stack.
  3. No change in flags.
  4. Has 2 cycles.



INPUT/OUTPUT PORTS



Interrupts sources in the PIC 16F877

Interrupt Source	Interrupt trigger event	CCS C Interrupt label
	TIMERS	
Timer 0	Timer 0 register overflow	INT_TIMER0
Timer 1	Timer 1 register overflow	INT_TIMER1
CCP 1	Timer 1 capture or compare detected	INT_CCP1
Timer 2	Timer 2 register overflow	INT_TIMER2
CCP2	Timer 2 capture or compare detected	INT_CCP2
	PORTS	
RB0/INT pin	Change on single pin RB0	INT_EXT
Port B pins	Change on any of four pins RB4 – RB7	INT_RB
Parallel Slave Port	Data received at PSP (write input active)	INT_PSP
Analog Converter	A/D conversion completed	INT_AD
Analog Comparator	Voltage compare true	INT_COMP
	SERIAL	
UART Serial Port	Received data available	INT_RDA
UART Serial Port	Transmit data buffer empty	INT_TBE
SPI Serial Port	Data transfer completed (read or write)	INT_SSP
I2C Serial Port	Interface activity detected	INT_SSP
I2C Serial Port	Bus collision detected	INT_BUSCOL
	MEMORY	
EEPROM	Non-volatile data memory write complete	INT_EEPROM