



SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

An Autonomous Institution

Accredited by NBA – AICTE and Accredited by NAAC – UGC with 'A' Grade
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ARM-Pipelining

Dr.G.Arthy
Assistant Professor
Department of EEE
SNS College of Engineering

ARE YOU USING THIS? (RECAP)



Toshiba PD RM4



Lexmark Z52
Color Jetprinter



InCard MoKard



BOSCH



SONICblue RIO Digital Audio



EXFO FTB-100



Creative Nomad
Jukebox



Intel Pocket Concert



Wherify GPS
watch



Galleo Communicator



D-Link Wireless LAN



Zoom Cable
Modem



Alcatel ADSL
Modem



Efficient Networks
ADSL Router



Alcatel Speed
Touch Wireless



G.Mate Yopy



Nokia Communicator



Compaq iPAQ



Ericsson
T68



Trium
Eclipse



Sendo Z100



Nokia 8310



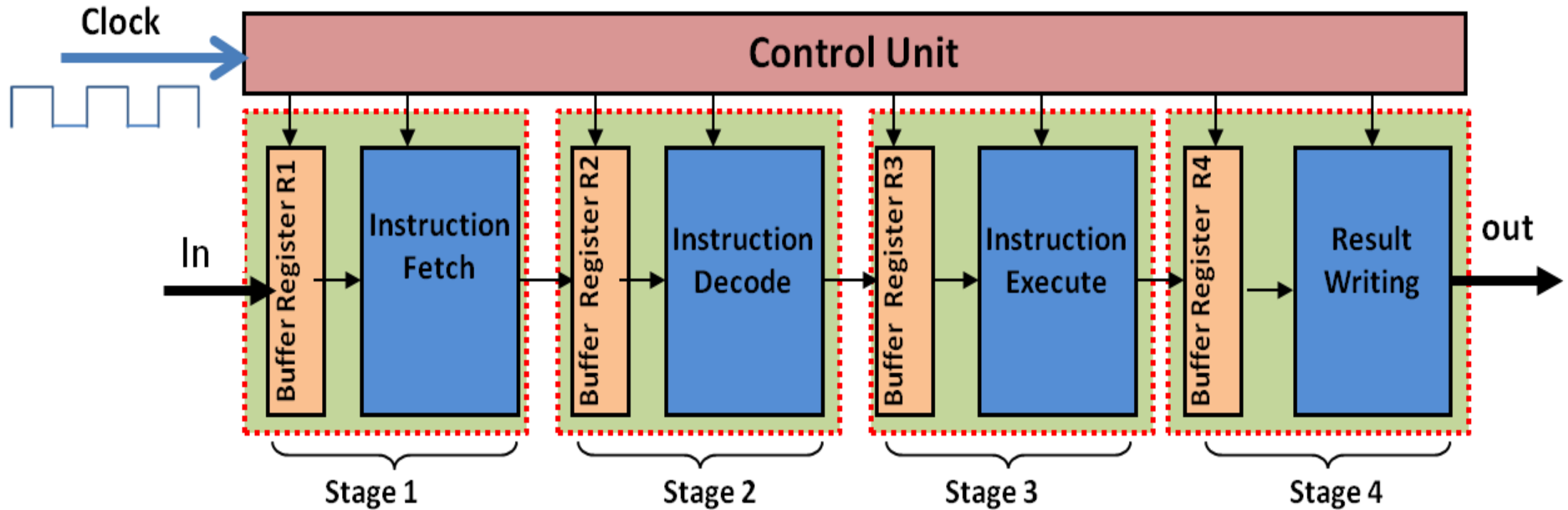
RECAP



- ARM Features
- ARM Architecture
- ARM Registers

PIPELINING

- Storing and prioritizing instructions.





WHY PIPELINING?



- Improves the efficiency
- Pipelining in ARM boosts execution speed.



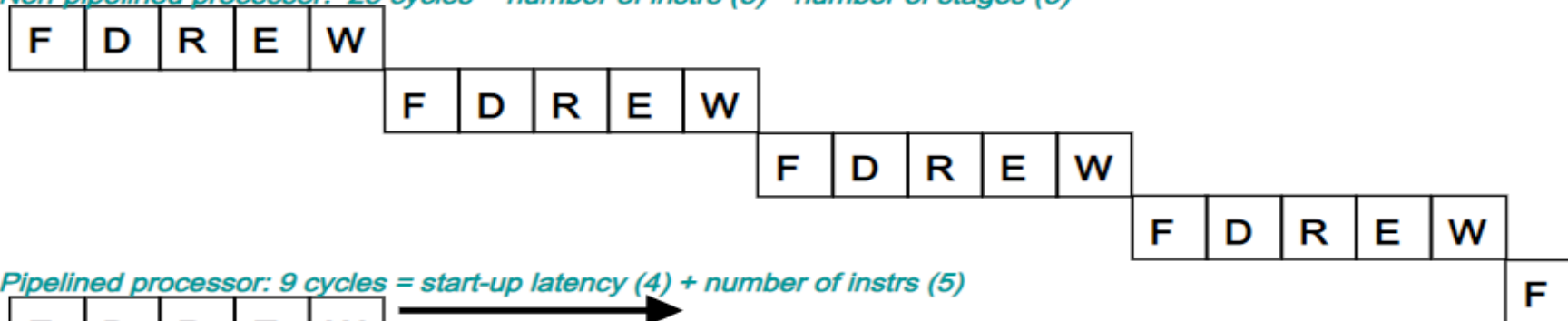
HOW PIPELINING WORKS?



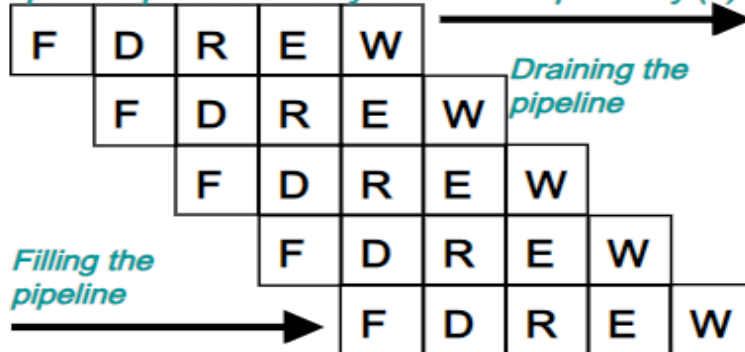
```
LD R1 <- A
ADD R5, R3, R4
LD R2 <- B
SUB R8, R6, R7
ST C <- R5
```

5 stage pipeline:
Fetch – Decode – Read – Execute - Write

Non-pipelined processor: 25 cycles = number of instrs (5) * number of stages (5)



Pipelined processor: 9 cycles = start-up latency (4) + number of instrs (5)



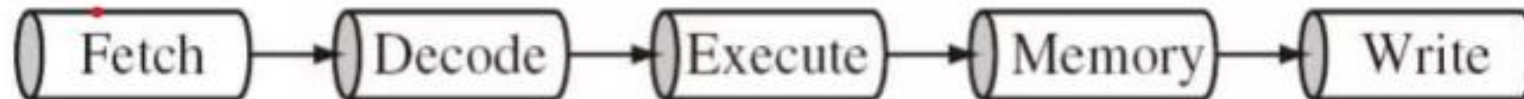
PIPELINE STAGES

- ARM implements different pipeline stages in its architectures.

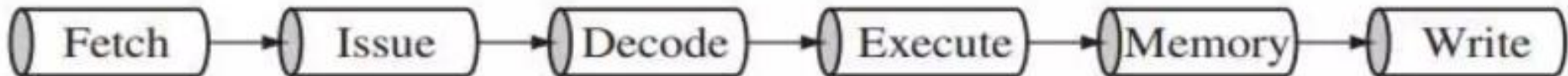
- ARM 7- 3 stage Pipeline



- ARM 9- 5 stage Pipeline

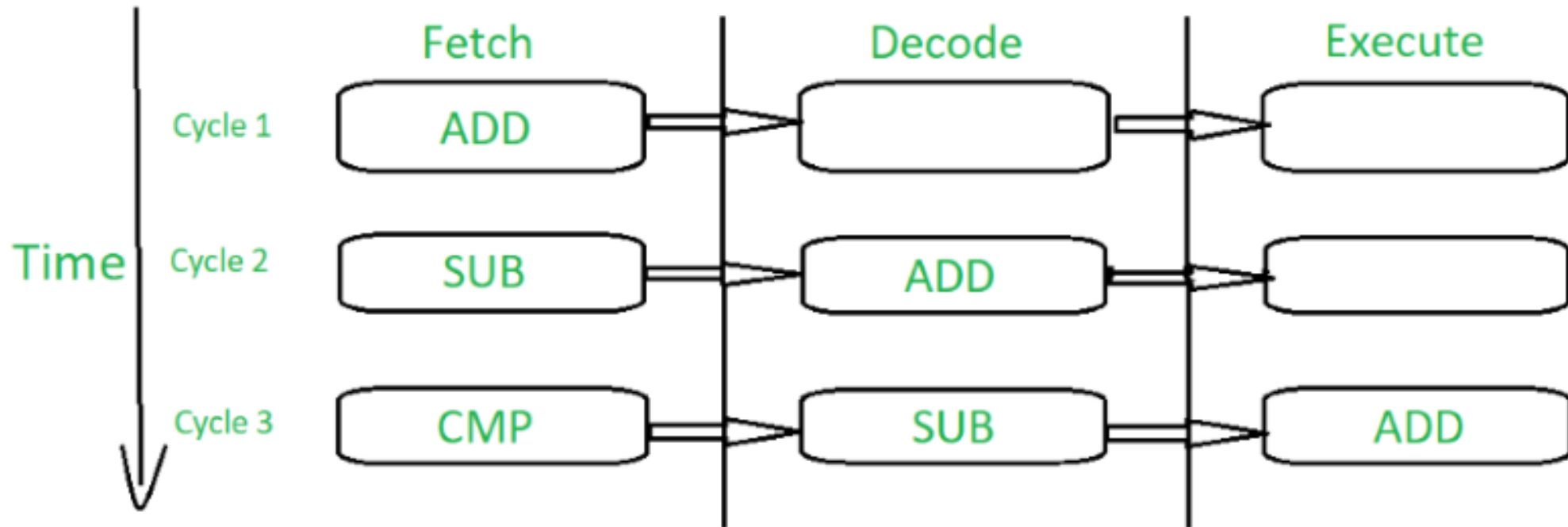


- ARM 10- 6 stage Pipeline





PIPELINING IN ARM 7





ROLE PLAY





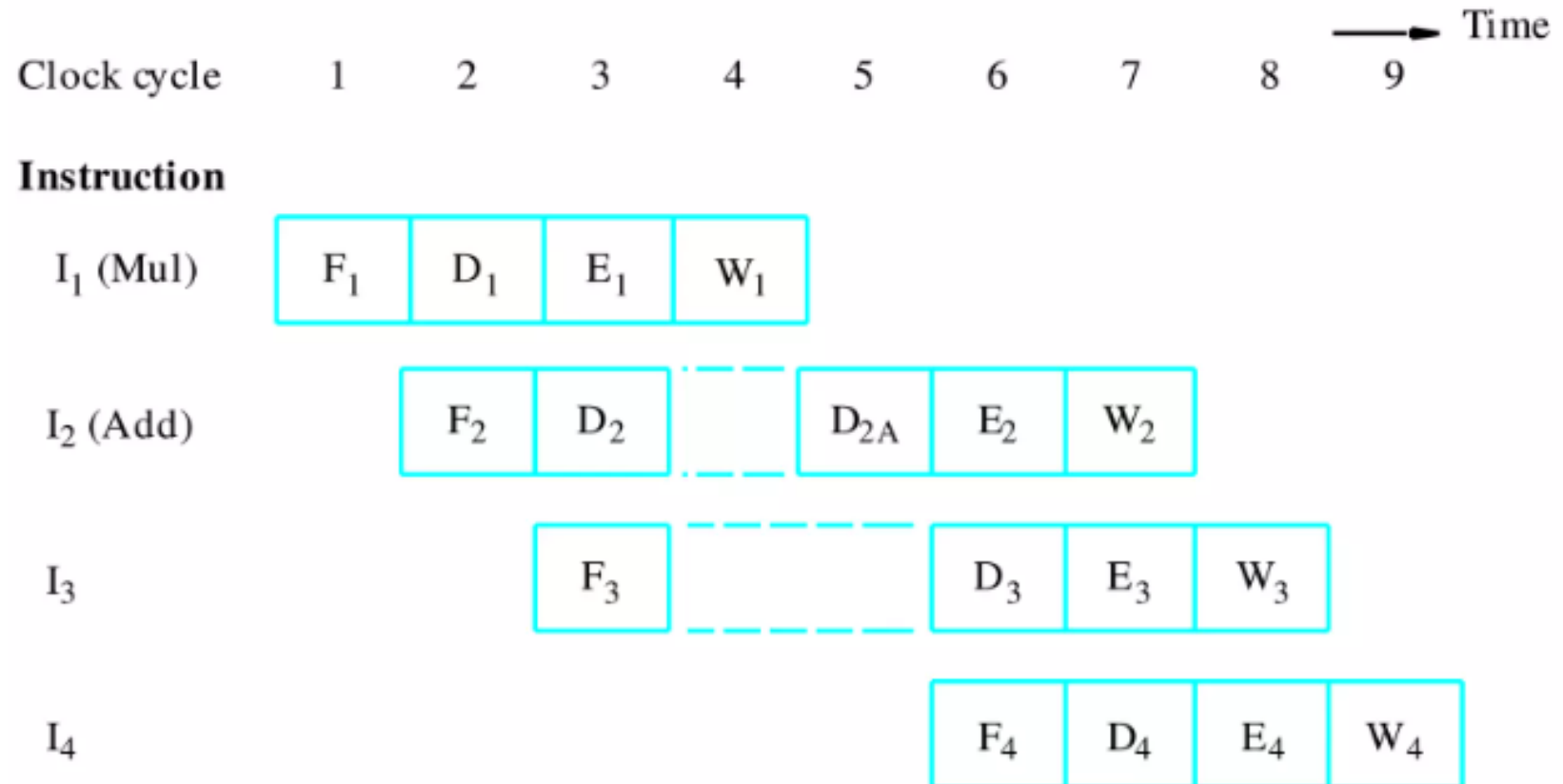
HAZARDS



- Data Hazards
- Instruction Hazards

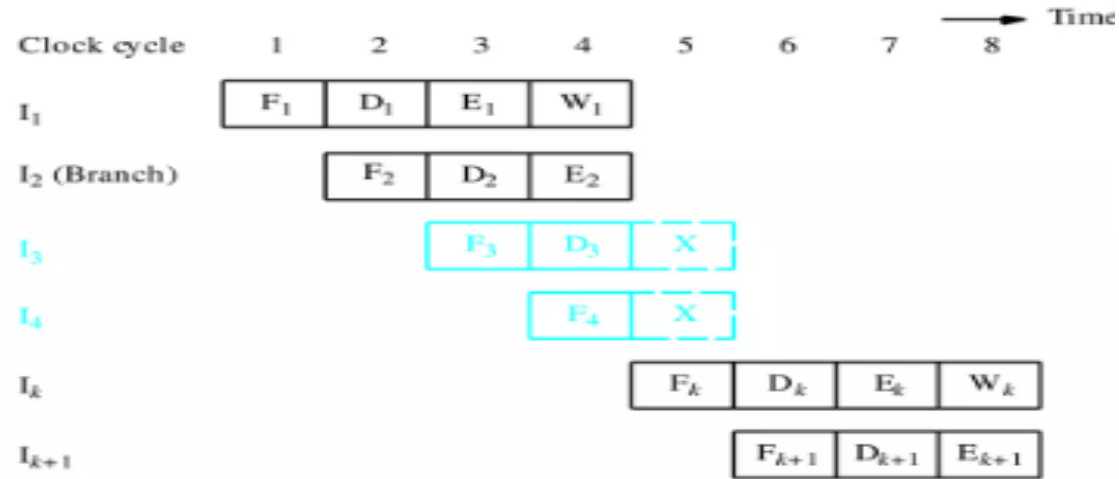


DATA HAZARDS

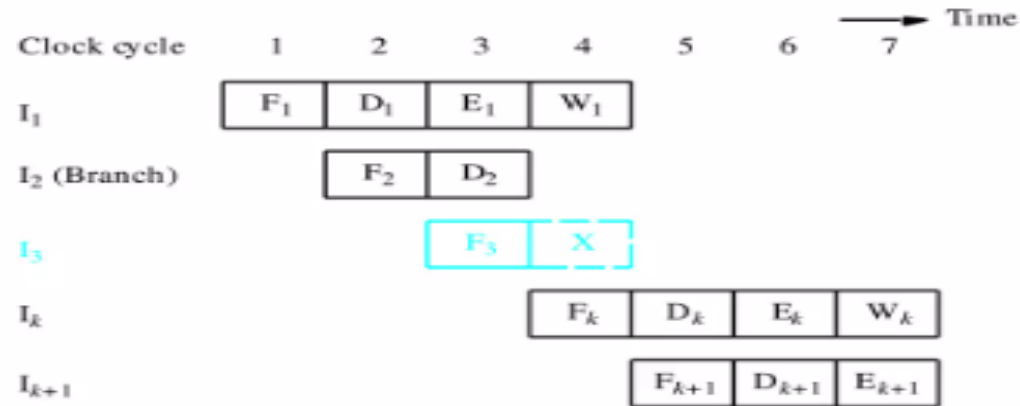




INSTRUCTION HAZARD



(a) Branch address computed in Execute stage



(b) Branch address computed in Decode stage



IMPROVING EFFICIENCY

LOOP	Shift_left	R1
	Decrement	R2
	Branch=0	LOOP
NEXT	Add	R1,R3

(a) Original program loop

LOOP	Decrement	R2
	Branch=0	LOOP
	Shift_left	R1
NEXT	Add	R1,R3

(b) Reordered instructions



ASSESSMENT



1. How many stages of pipelining was there in ARM 9?

a) 3

b) 5

c) 7

d) None

2. List the types of Hazards in pipelining.

