SNS COLLEGE OF ENGINEERING

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

ARM-Registers

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ARE YOU USING THIS?

REGISTERS

- ARM processors have 37 registers.
- The registers are arranged in partially overlapping banks.
- There is a different register bank for each processor mode.
- The banked registers give rapid context switching for dealing with processor exceptions and privileged operations.

REGISTERS

- Thirty general-purpose registers (32 bit each)
- The Program Counter (PC)
- The Application Program Status Register (APSR)
- Saved Program Status Registers (SPSRs).
- Current Program Status Registers (CPSRs).

ARM-OPERATING MODES

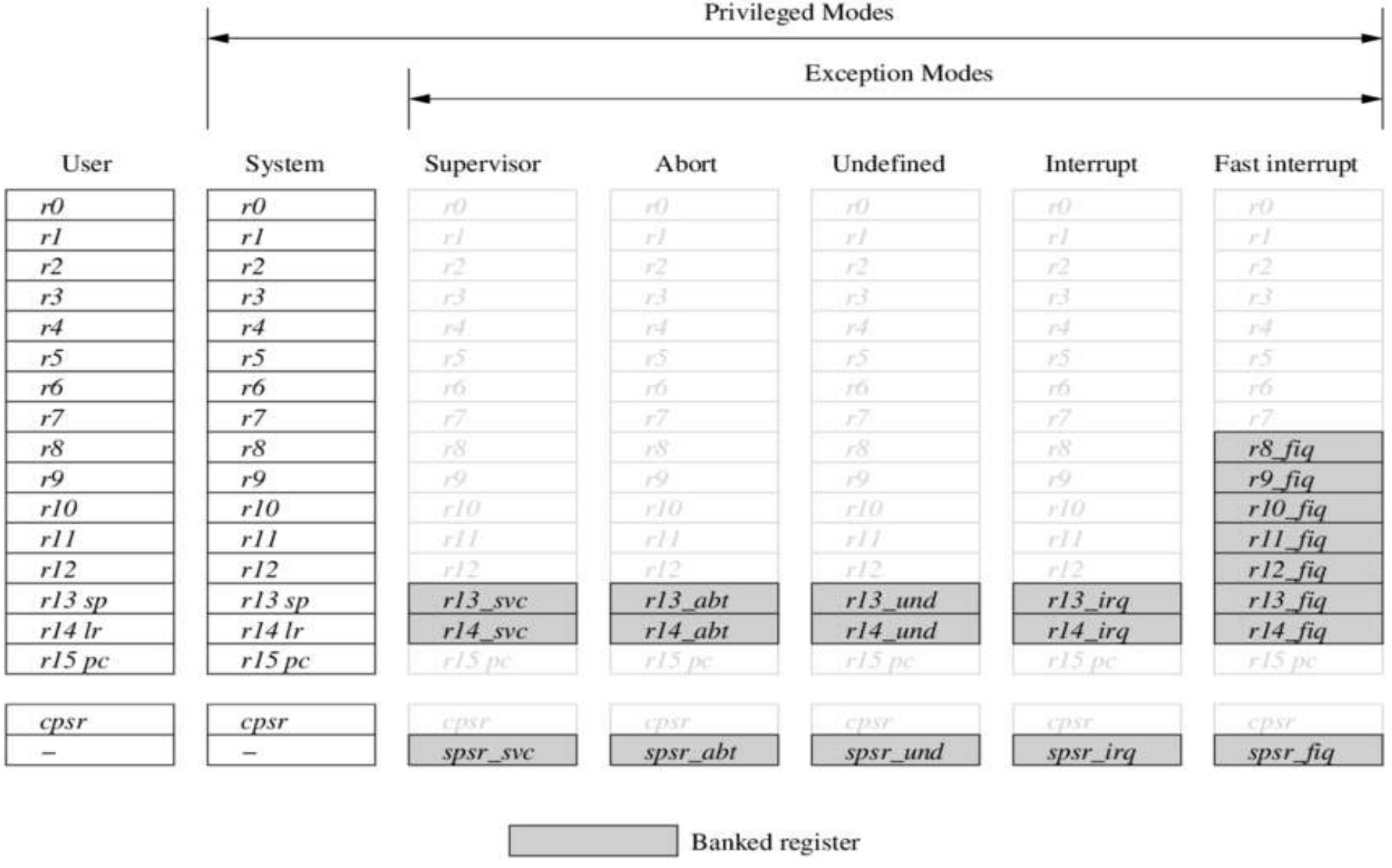
Mode	Privileged	Purpose
User	No	Normal operating mode for most programs (tasks)
Fast Interrupt (FIQ)	Yes	Used to handle a high-priority (fast) interrupt
Interrupt (IRQ)	Yes	Used to handle a low-priority (normal) interrupt
Supervisor	Yes	Used when the processor is reset, and to handle the software interrupt instruction `swi`
Abort	Yes	Used to handle memory access violations
Undefined	Yes	Used to handle undefined or unimplemented instructions
System	Yes	Uses the same registers as User mode

Table 1: ARM Processor Operating Modes

EXECUTION MODES

- A **privileged execution** has access to all resources.
- **Unprivileged execution** limits or excludes access to some resources.

REGISTERS


Privileged Modes
Exception Modes
User
System
Supervisor
Abort
Undefined
Interrupt
Fast interrupt
r0
r1
r2
r3
r4
r5
r6
r7
r8
r9
r10
r11
r12
r13 sp
r14 lr
r15 pc
cpsr
–
r13_svc
r14_svc
spsr_svc
r13_abt
r14_abt
spsr_abt
r13_und
r14_und
spsr_und
r13_irq
r14_irq
spsr_irq
r8_fiq
r9_fiq
r10_fiq
r11_fiq
r12_fiq
r13_fiq
r14_fiq
spsr_fiq
Banked register

LINK REGISTER

- r14 or lr – In user mode, used as a link register to store the return address when a subroutine call is made.

- r14 or lr – In exception mode, lr holds the return address for the exception, or a subroutine return address if subroutine calls are executed within an exception.

PROGRAM COUNTERS

- Program Counter is accessed as pc (or r15).

- It is incremented by one word (four bytes) for each instruction.
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- Branch instructions load the destination address into pc.

Application Program Status Register (APSR)

- APSR holds copies of the Arithmetic Logic Unit (ALU) status flags.

- They are used to determine whether conditional instructions are executed or not.

Saved Program Status Registers (SPSRs)

- The SPSRs are used to store the CPSR when an exception is taken.
- User mode and System mode do not have an SPSR because they are not exception handling modes.

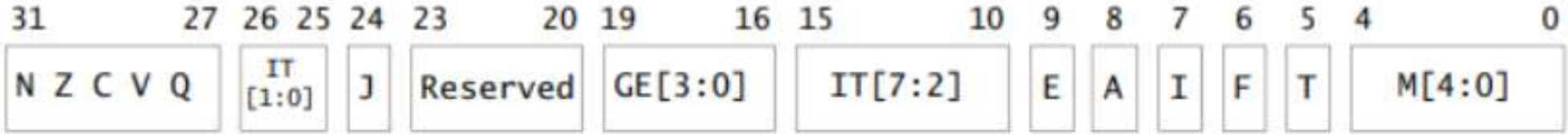
Current Program Status Register (CPSR)

The CPSR holds:

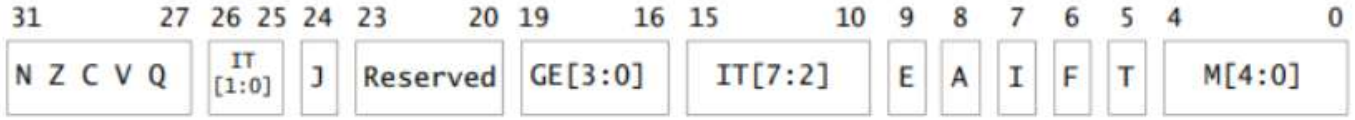
- The APSR flags
- The current processor mode
- Interrupt disable flags
- Current processor state (ARM, Thumb, or Jazelle)

Current Program Status Register (CPSR)

- CPSR to monitor and control internal operations.
- The CPSR is a dedicated 32-bit register and resides in the register file.



Current Program Status Register (CPSR)



- • N – Negative result from ALU.
- • Z – Zero result from ALU.
- • C – ALU operation Carry out.
- • V – ALU operation oVerflowed.
- • Q – cumulative saturation (also described as sticky).
- • J – indicates whether the core is in Jazelle state.
- • GE – used by some SIMD instructions.
- • IT [7:2] – If-Then conditional execution of Thumb-2 instruction groups.
- • E bit controls load/store endianness.
- • A bit disables asynchronous aborts.
- • I bit disables IRQ.
- • F bit disables FIQ.
- • T bit – indicates whether the core is in Thumb state.
- • M[4:0] – specifies the processor mode

EXCEPTIONS