SNS COLLEGE OF ENGINEERING

Kurumbapalayam (PO), Coimbatore – 641 107
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DEPARTMENT OF INFORMATION TECHNOLOGY

COURSE NAME: 19IT301 COMPUTER ORGANIZATION AND ARCHITECTURE

II YEAR/ III SEM

Unit 3 : Processor and Pipelining

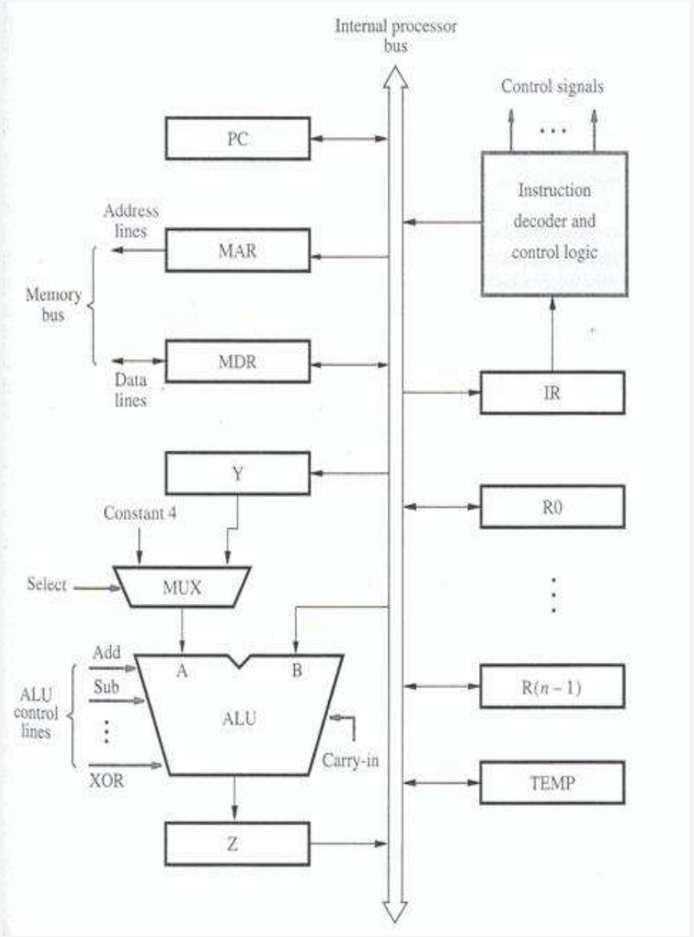
Topic 3.2: Execution of a Complete Instruction – Multiple bus organization

Execution of a Complete Instruction

Sequence of elementary operations to execute Add (R3), R1 requires the following actions:

- Fetch the instruction
- Fetch the first operand (the contents of the memory location pointed to by R3)
- Perform the addition
- Load the result into R1

Execution of a Complete Instruction



Control Sequence for execution of the instruction Add (R3), R1 in a single-bus architecture

Step	Action	
1	PC_{out}, MAR_{in}, Read, Select4, Add, Z_{in}	Fetch Phase
2	Z_{out}, PC_{in}, Y_{in} WMF C	
3	MDR_{out}, IR_{in}	
4	$R3_{out}$, MAR_{in}, Read	Execution Phase
5	$R1_{out}$, Y_{in}, WMFC	
6	MDR_{out}, SelectY, Add, Z_{in}	
7	Z_{out}, $R1_{in}$, End	

Execution of Branch Instructions

- A branch instruction replaces the contents of PC with the branch target address, which is usually obtained by adding an offset X given in the branch instruction.
- The offset X is usually the difference between the branch target address and the address immediately following the branch instruction.
- UnConditional branch

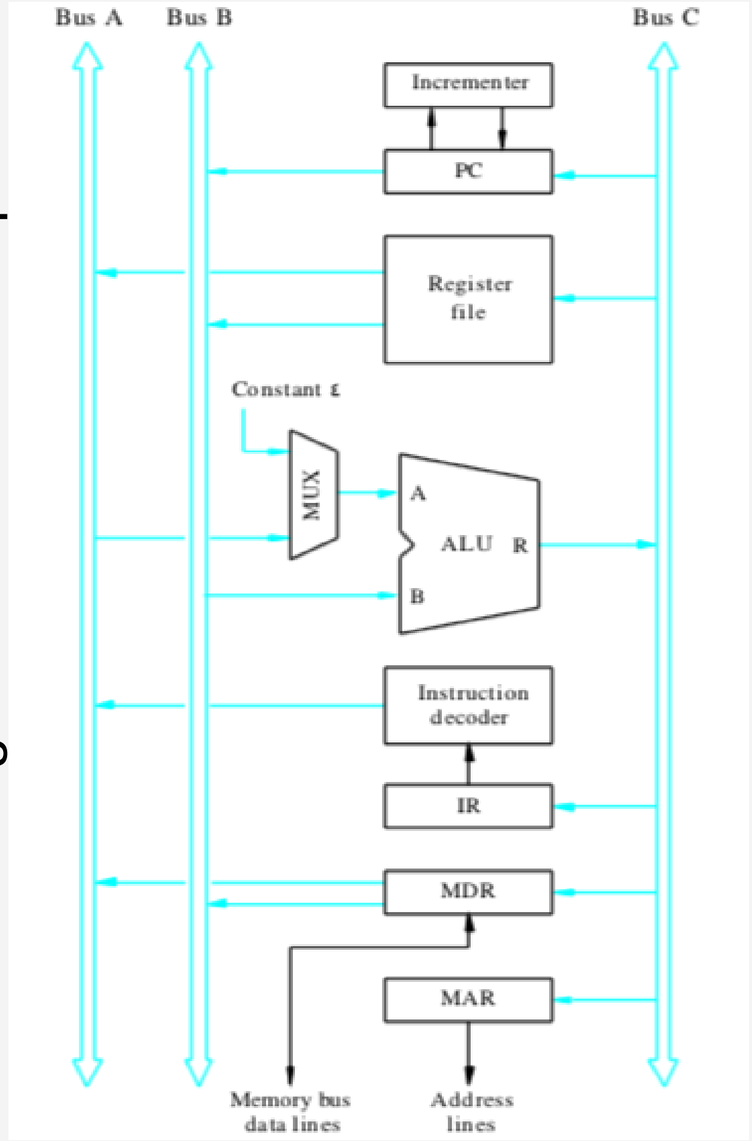
Control sequence for an unconditional branch instruction

Step	Action
1	PC_{out}, MAR $_{in}$, Read, Select4, Add, Z_{in}
2	Z_{out}, PC_{in}, Y_{in}, WMF C
3	MDR_{out}, IR_{in}
4	Offset-field-of-IR_{out}, Add, Z_{in}
5	Z_{out}, PC_{in}, End

PC=2000, Target address=2050
X = 46

Multiple-Bus Organization

Threebus organization of the datapath



- Allow the contents of two different registers to be accessed simultaneously and have their contents placed on buses A and B.
- Allow the data on bus C to be loaded into a third register during the same clock cycle.
- Incrementer unit.
- ALU simply passes one of its two input operands unmodified to bus C

→ control signal: R=A or R=B

Multiple-Bus Organization

- General purpose registers are combined into a single block called ***register file.***
- Register file has 3 ports, 2 outputs ports –access two different registers and have their contents on buses A and B
- Third port allows data on bus C during same clock cycle.
- Buses A & B are used to transfer the source operands to A & B inputs of the ALU.
- ALU operation is performed.
- The result is transferred to the destination over the bus C.

Multiple-Bus Organization

- ALU may simply pass one of its 2 input operands unmodified to bus C.
- The ALU control signals for such an operation R=A or R=B.
- Incrementer unit is used to increment the PC by 4.
- Using the incrementer eliminates the need to add the constant value 4 to the PC using the main ALU.
- The source for the constant 4 at the ALU input multiplexer can be used to increment other memory address such as loadmultiple & storemultiple instructions

Control sequence for the instruction Add R4,R5,R6, for the three-bus organization

Step	Action	
1	PC_{out}, R=B, MAR_{in}, Read, IncPC	Fetch Phase
2	WMFC	
3	MDR_{outB}, R=B, IR_{in}	
4	$R4_{outA}$, $R5_{outB}$, SelectA, Add, $R6_{in}$, End	Execution Phase

Explanation

Step 1: The contents of PC are passed through the ALU using R=B control signal & loaded into MAR to start a memory read operation.

At the same time PC is incrementer by 4

Step 2: The processor waits for MFC

Step 3: Loads the data ,received into MDR ,then transfers them to IR.

Step 4: The execution phase of the instruction requires only one control step to complete.

Advantage: Reduction in the number of clock cycles to execute an instruction

Assessment

What is the control sequence for execution of the instruction

Add R1, R2

including the instruction fetch phase? (Assume single bus architecture)

Thank You