

Divide by N Counter

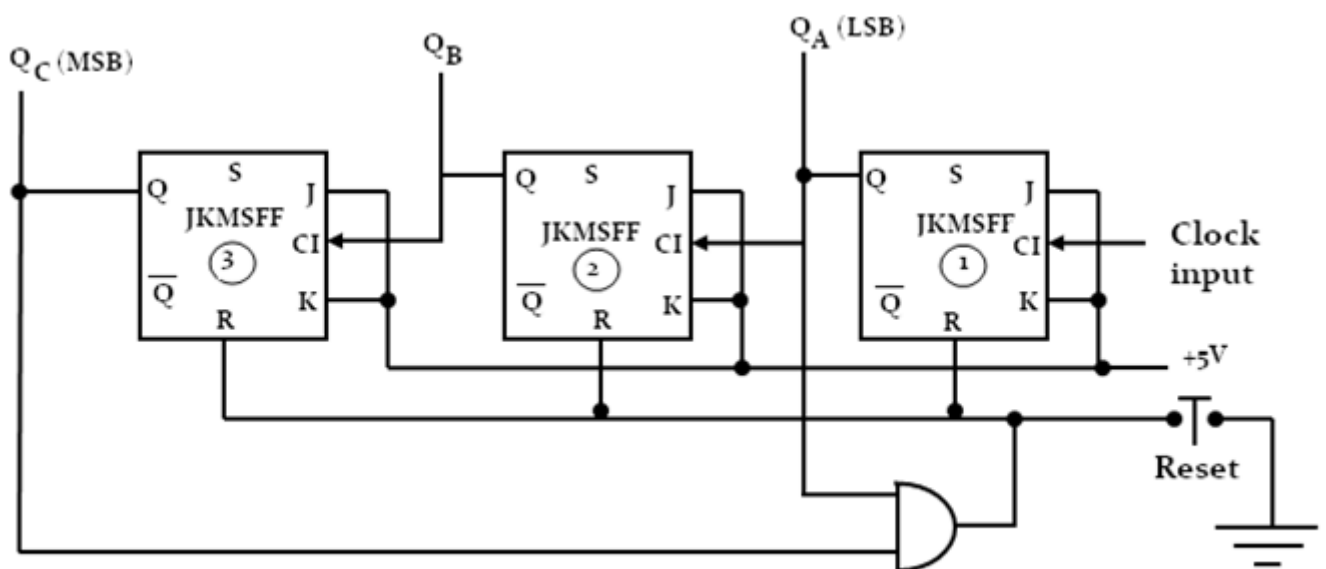
A counter, which is reset (makes the whole output as zeros) at the n^{th} clock pulse is called 'mod n counter' or divide by n^{th} counter'. Logic gates that are connected externally, make to reset the counter at the n^{th} clock pulse. An extra NAND gate is generally used for making divide by n counters. For this, which flip-flops output are actually is high (1) level in the n^{th} clock pulse. Then connect the outputs of that flip-flops to the input terminals of the NAND gate. The output terminal of the NAND gate.

The output terminal of the NAND gate is connected to the reset terminal of the counter. Thus at the n^{th} clock pulse, all inputs connected to the NAND gate are high, makes the output as 0, and to reset the counter. After applying the next clock pulse the counter will start the count from its initial level. The number of flip-flops needed, for this counter depends upon the 'n' value. A three bit counter, counts upto 7 ($=2^3-1$). Similarly an 'n' bit counter, counts up to 2^n-1 value.

Modulo 5 Counter

A counter which is reset at the fifth clock pulse is called Mod 5 counter or Divide by 5 counter. The circuit diagram of Mod 5 counter. This counter contains three JKMS flip-flop.

Logic Diagram:



Truth table:

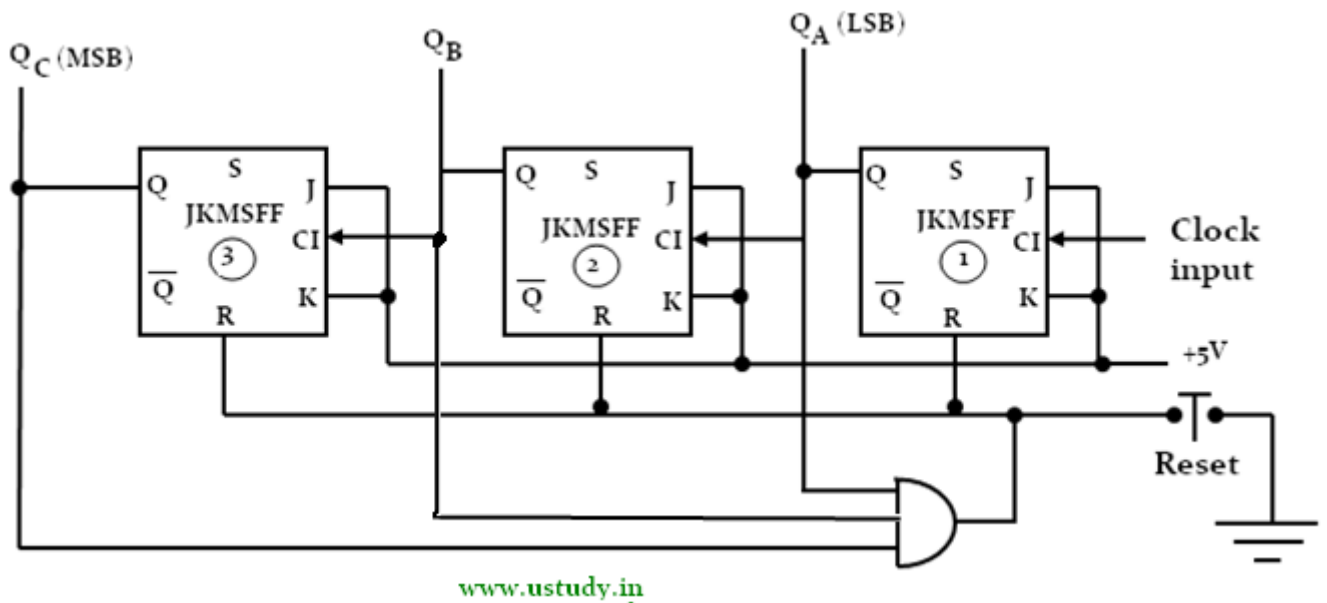
Clock	Q_c	Q_B	Q_A
Reset	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	0	0	0
6	0	0	1

- A 3 bit binary counter is normally counting from 000 to 111. The actual output of a 3 bit binary counter at the fifth clock pulse is 101.
- A two input NAND gate is used to make a Mod 5 counter.
- The outputs of the first and third flip flops (Q_A and Q_C) are connected to the input of the give NAND gate, and its output is connected to the RESET terminal of the counter,
- Hence the counter is reset at the fifth clock pulse, which produces the output Q_C,Q_B,Q_A as 000. It is called divide by 5thcounter or **mod 5 counter**.

Modulo 7 Counter

A three bit counter will count up to 7($2^3-1=7$). At the eighth clock pulse, its output goes to 000 automatically. Hence a 3 bit counter is called mode 8 counter. So it needs 3 flip flops for making a mode 7 counter. The actual output of the 7th clock pulse is 111. Hence a 3 input NAND gate is used in this counter. The Q output of all flip flops is connected to the input of NAND gage. The output of NAND gate is connected to the reset terminal of the counter. In the normal counting values, minimum one of the input of the NAND gate is zero, which makes the output as one. So the flip flop are not going to reset condition. The normal operation or flip-flop is not affected during this time.

Logic diagram:



Truth table:

Clock	QC	QB	QA
Reset	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	0	0	0
8	0	0	1

At the 7th clock pulse, the count value of this counter reaches 111. This value makes all the inputs of the NAND gate as high level, and produces its output as zero. Hence the counter is reset at the 7th clock pulse and produces the output as 000. It is called divided by 7th counter or **mod 7 counter**.