

SNS COLLEGE OF ENGINEERING

An Autonomous Institution

19IT402 - MICROCONTROLLER AND EMBEDDED SYSTEMS

4/9/2023

19IT401 / Microcontroller and Embedded Systems / Interfacing / R.Saranya / AP/ ECE / SNSCE



Kurumbapalayam(Po), Coimbatore – 641 107

- Accredited by NAAC-UGC with 'A' Grade
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Unit -2 – PERIPHERAL INTERFACING





Interface is the path for communication between two components. Interfacing is of two types, memory interfacing and I/O interfacing.



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Memory Interfacing

•To Execute a instruction, the microprocessor need to access the memory for reading instruction codes and the data stored in the memory.

• For this, both the memory and the microprocessor requires some signals to read from and write to registers.

•The interfacing process includes some key factors to match with the memory requirements and microprocessor signals.

•The interfacing circuit therefore should be designed in such a way that it matches the memory signal requirements with the signals of the microprocessor.

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I/O Interfacing

Need to interface the keyboard and other devices with the microprocessor by using latches and buffers.

This type of interfacing is known as I/O interfacing.



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Memory mapped I/O and I/O Mapped I/O

 \succ CPU uses two methods to perform input/output operations between the CPU and peripheral devices in the computer.

 \succ These two methods are called memory mapped IO and IO mapped IO

The main difference between memory mapped IO and IO mapped IO is

- Memory mapped IO uses the same address space for both memory and IO device
- IO mapped IO uses two separate address spaces for memory and IO device.





Memory Mapped I/O



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Address Bus

Data Bus

Control Bus





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Assessment

Difference between Memory mapped I/O and I/O mapped I/O?

Isolated I/O	
Memory and I/O have separate address space	Both have sa
All address can be used by the memory	Due to addit become less
Separate instruction control read and write operation in I/O and Memory	Same instruc Memory
In this I/O address are called ports.	Normal mem
More efficient due to separate buses	Lesser efficie
Larger in size due to more buses	Smaller in siz
It is complex due to separate logic is used to control both.	Simpler logic memory only



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Memory Mapped I/O

- me address space
- ion of I/O addressable memory for memory
- ctions can control both I/O and
- nory address are for both
- ent
- ze
- is used as I/O is also treated as ٧.



THANK YOU

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