SNS COLLEGE OF ENGINEERING

Kurumbapalayam (Po), Coimbatore – 641 107

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DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

COURSE NAME : 19EE101-BASIC ELECTRICAL & ELECTRONICS ENGINEERING

I YEAR /I SEMESTER MCT

Unit 5: Linear and Digital Electronics

UNIT V
LINEAR AND DIGITAL ELECTRONICS

Ideal OP-AMP characteristics, Inverting and Non-inverting Amplifiers, Applications: summer, clipper and clamper

Boolean Algebra-Theorems-Logic Gates - Half Adder and Full Adders - Flip flops,

A/D and D/A Conversion (Any one concept)

Boolean Algebra

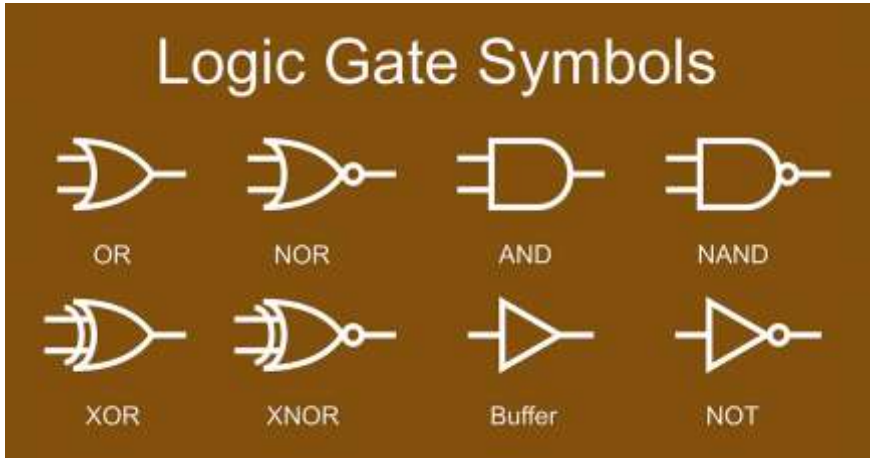
- **Boolean Algebra** is **used to** analyze and simplify the digital (logic) circuits.
- It **uses** only the binary numbers i.e. 0 and 1. It is also called as Binary **Algebra** or logical **Algebra**.

Laws and Theorems

Boundness law:	$A + 1 = 1$	$A \bullet 0 = 0$
Identity law:	$A + 0 = A$	$A \bullet 1 = 1$
Idempotent Theorem:	$A + A = A$	$A \bullet A = A$
Involution Theorem:	$(A')' = A$	
Theorem of complementarity:	$A + A' = 1$	$A \bullet A' = 0$
Commutative law:	$A + B = B + A$	$AB = BA$
Associative law:	$A + (B + C) = (A + B) + C$	$A(BC) = (AB)C$
Distributive law:	$A\,(B + C) = AB + AC$	$A + BC = (A+B)(A+C)$
DeMorgan's Theorem:	$(A + B)' = A'B'$	$(AB)' = A' + B'$
Absorption law:	$A + AB = A$	$A(A + B) = A$
Consensus Theorem:	$AB+BC+A'C = AB+A'C$	$(A+B)(B+C)(A'+C) = (A+B)(A'+C)$

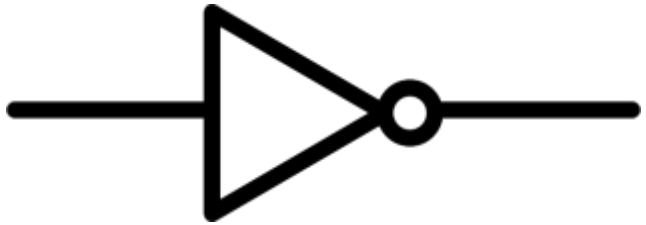
Logic Gates

- Logic gates are the basic building blocks of any digital system.
- It is an electronic circuit having one or more than one input and only one output.
- A truth table is a table showing the outputs for all possible combinations of inputs to a logic gate or circuit.
- When putting values into a truth table, we often write them as 1 or 0.
- These values are interchangeable with True and False: 1 is True, and 0 is False.



NOT Gate

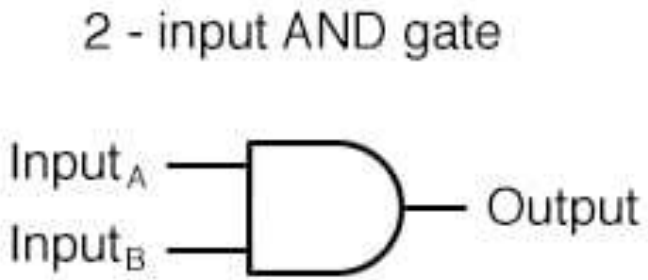
- The NOT operation flips a value to its opposite.
- If an input A has the value True, NOT A has the value False.



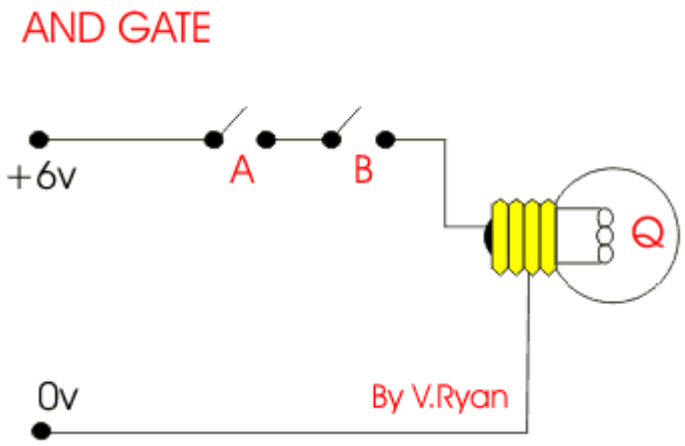
Input	Output
A	Y
0	1
1	0

AND Gate

- The AND operation only produces a True output if both inputs are True.



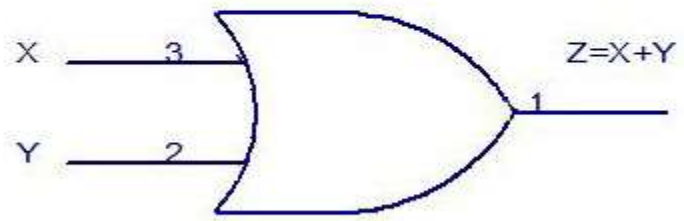
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1



OR Gate

- OR is True when any input is True — any one single input or both.
- + is the symbol used to represent OR in a Boolean expression.

2 Input OR Gate

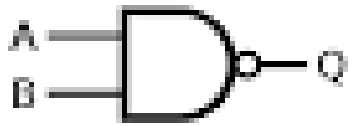


TRUTH TABLE

INPUTS		OUTPUT
X	Y	Z
0	0	0
0	1	1
1	0	1
1	1	1

NAND GATE

- To create a NAND gate, an AND gate is combined with a NOT gate.



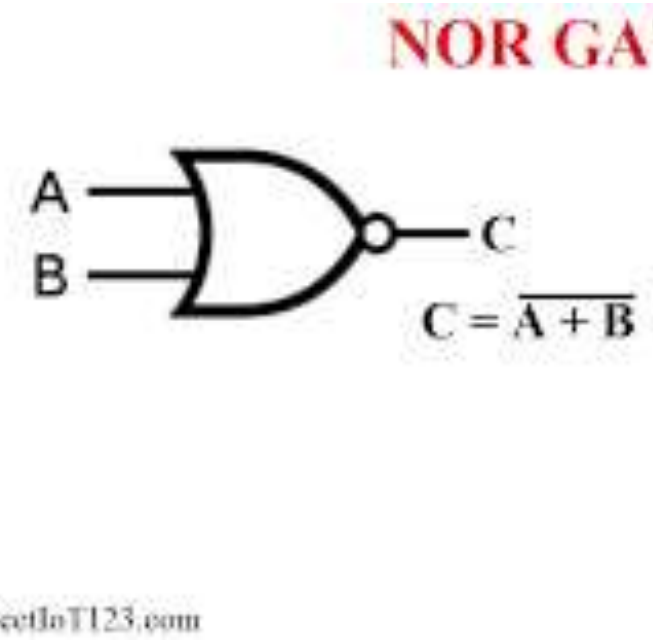
Q = A NAND B

Truth Table

Input A	Input B	Output Q
0	0	1
0	1	1
1	0	1
1	1	0

NOR Gate

To create a NOR gate, an OR gate is combined with a NOT gate.

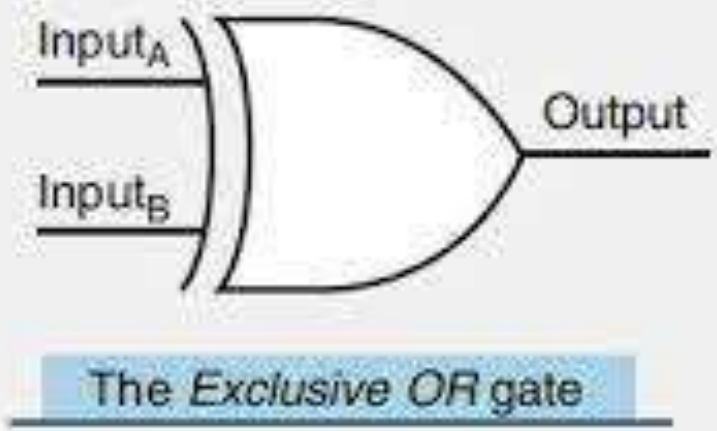


TRUTH TABLE

INPUT		OUTPUT
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

XOR Gate

- XOR or 'exclusive OR' is defined as being True when one input or the other is True, but **not when both are true**.
- $\oplus$ is the symbol used to represent XOR in a Boolean expression.



The *Exclusive OR* gate

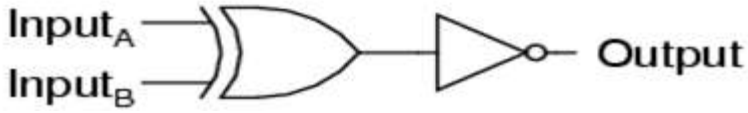
Input		Output
A	B	
0	0	0
0	1	1
1	0	1
1	1	0

X-NOR GATE

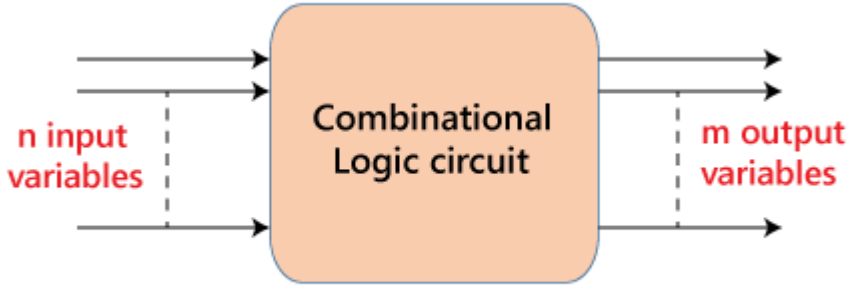
Exclusive-NOR gate

A	B	Output
0	0	1
0	1	0
1	0	0
1	1	1

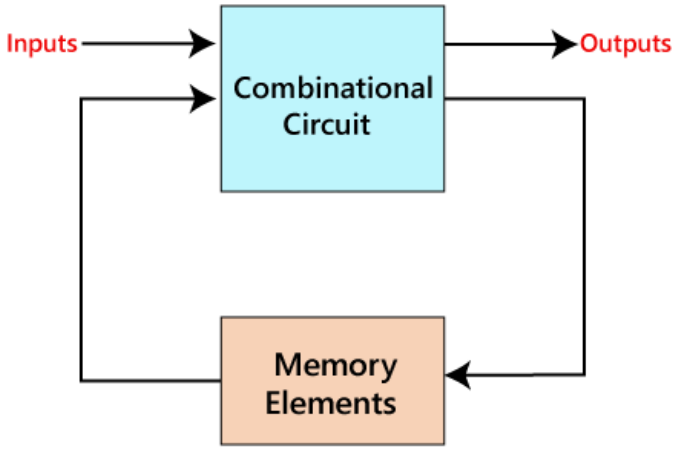
Equivalent gate circuit



Combinational Vs Sequential Circuit



Block diagram of a combinational circuit



Adder, Subtractor
Decoder, Encoder
Multiplexer, and De-multiplexer

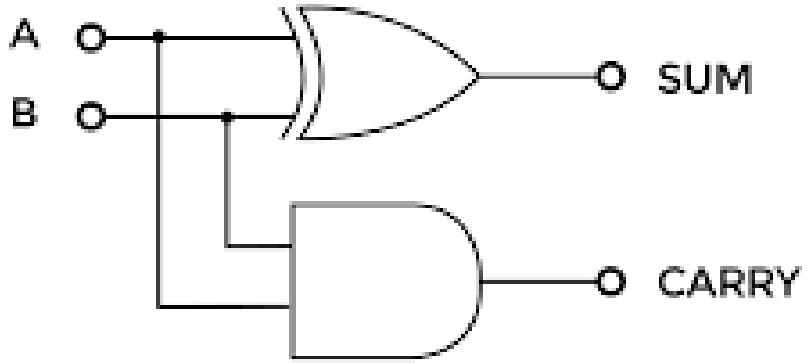
Flip Flops
Counters

Combinational Vs Sequential Circuit

1)	The outputs of the combinational circuit depend only on the present inputs.	The outputs of the sequential circuits depend on both present inputs and present state(previous output).
2)	The feedback path is not present in the combinational circuit.	The feedback path is present in the sequential circuits.
3)	In combinational circuits, memory elements are not required.	In the sequential circuit, memory elements play an important role and require.
4)	The clock signal is not required for combinational circuits.	The clock signal is required for sequential circuits.
5)	The combinational circuit is simple to design.	It is not simple to design a sequential circuit.

HALF ADDER

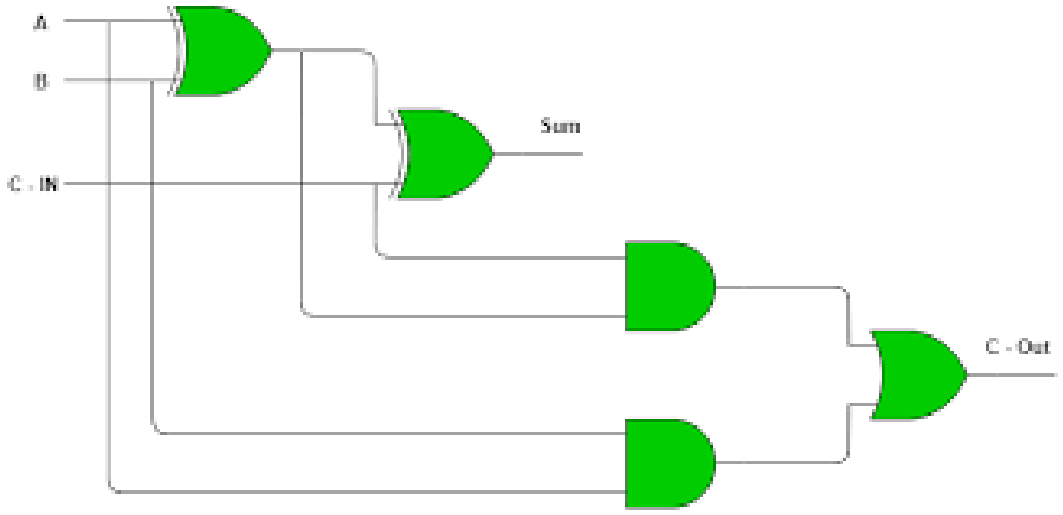
- A **half adder** is an **adder** which adds two binary digits together, resulting in a sum and a carry.
- Because this **adder** can only be used to add two binary digits, it cannot form a part of an **adder** circuit that can add two n-bit binary numbers.



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

FULL ADDER

- adds three inputs and produces two outputs
- eight inputs together to create a byte-wide **adder** and cascade the carry bit from one **adder** to the another.



Inputs			Outputs	
A	B	C_{in}	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

FLIP FLOP

- A circuit that has two stable states is treated as a **flip flop**.
- Flip-flops and latches are used as data storage elements.
- A flip-flop is a device which stores a single *bit* (binary digit) of data; one of its two states represents a "one" and the other represents a "zero".

SR flip-flop

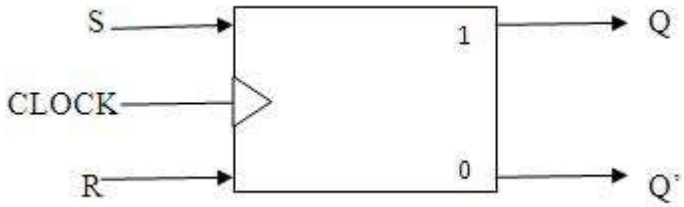
D flip-flop

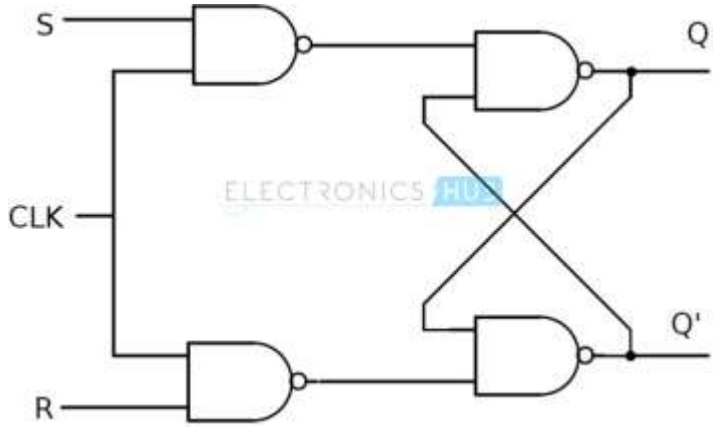
JK flip-flop

T flip-flop

SR Flip Flop

- the most common flip flop used in the digital system.

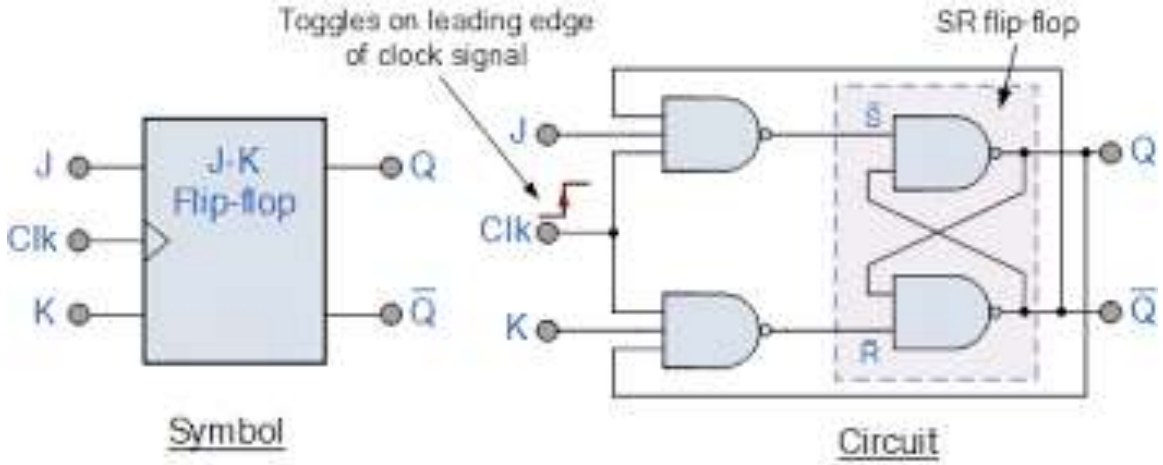




S	R	Q	STATE
0	0	PREVIOUS STATE	NO CHANGE
0	1	0	RESET
1	0	1	SET
1	1	?	FORBIDDEN

JK Flip Flop

- The JK flip flop is used to remove the drawback of the S-R flip flop, i.e., undefined states.
- formed by doing modification in the SR flip flop.

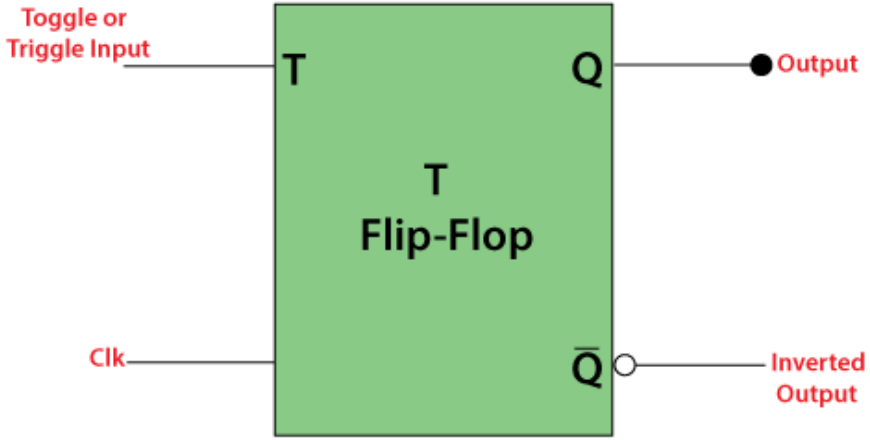


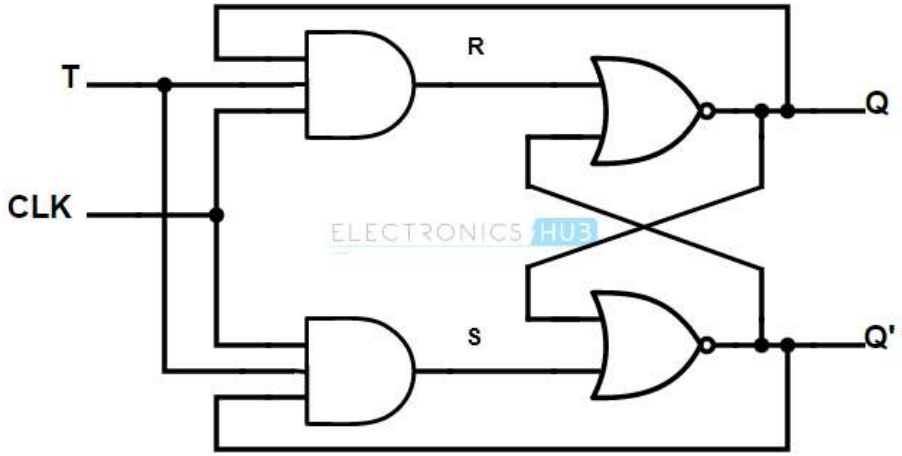
INPUT			OUTPUT	STATE
CLK	J	K	Q	
Not ↑	X	X	Q_{PREV}	Previous
↑	0	0	No Change	Previous
↑	0	1	1	Reset
↑	1	0	0	Set
↑	1	1	$\overline{Q}_{PREV}$	Toggle

T Flip Flop

- only a single input
- to avoid an intermediate state occurrence.

Input	Outputs	
	Present State	Next State
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

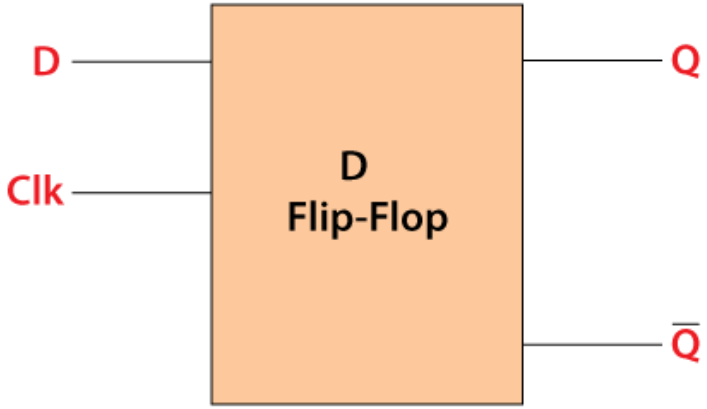


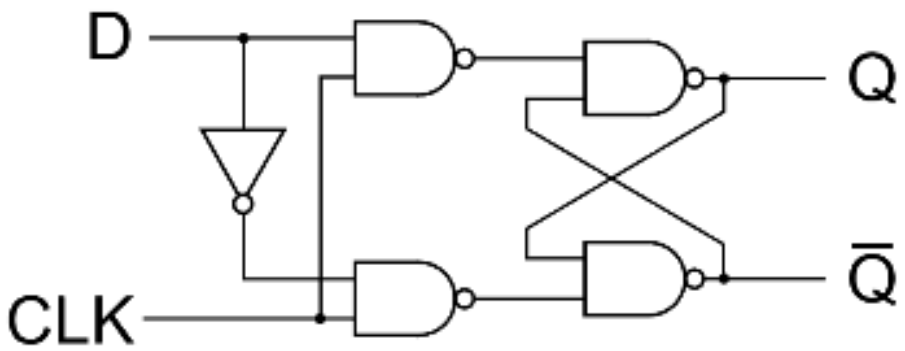


D Flip Flop

- connect the inverter between the Set and Reset inputs
- most important flip flop from other clocked types.
- ensures that at the same time, both the inputs, i.e., S and R, are never equal to 1.

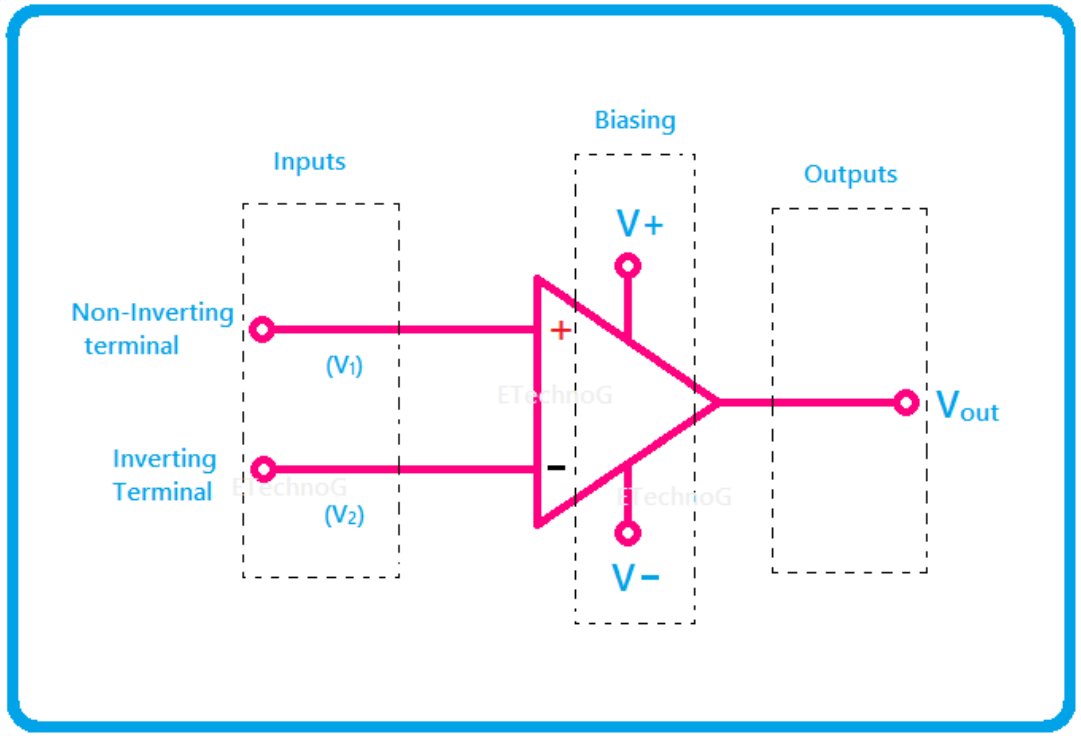
D Flip Flop		
Input	Output	
D	Q	Q^
0	0	1
1	1	0



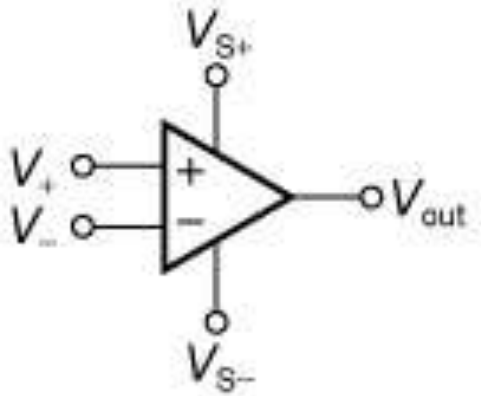


Operational Amplifier

- It is an integrated circuit that can amplify weak electric signals.
- has two input pins and one output pin.
- basic role is to amplify and output the voltage difference between the two input pins.

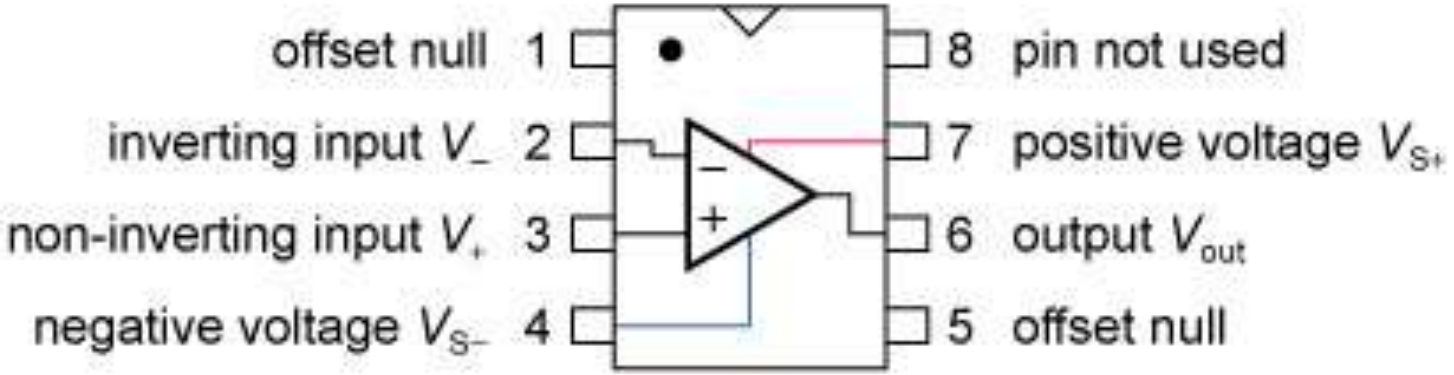


Pin configuration



(a)

(b)

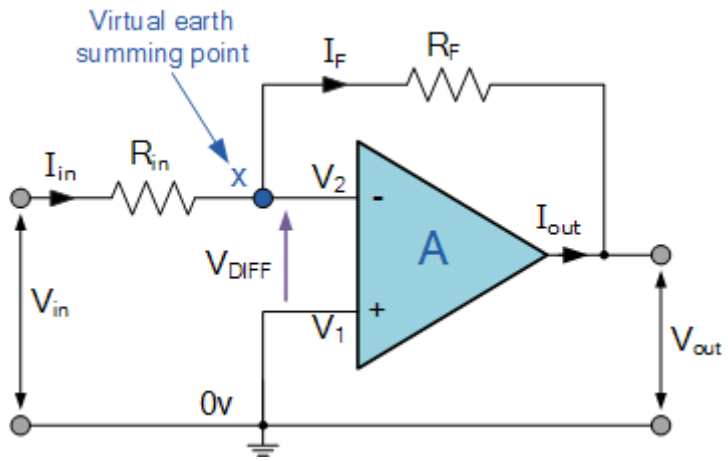


(c)

Ideal Op-Amp

- Infinite Input Resistance
- Zero Output Impedance
- Infinite Open-loop Gain
- Infinite Common-mode Rejection Ratio
- Infinite Bandwidth

Inverting Amplifier



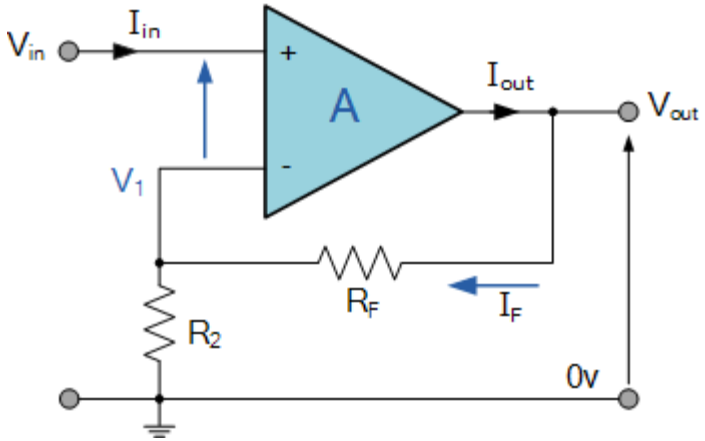
two very important rules to remember about **Inverting Amplifiers** or any operational amplifier

- No Current Flows into the Input Terminals
- The Differential Input Voltage is Zero as V1 = V2 = 0 (Virtual Earth)

$$\text{Gain (Av)} = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_{in}}$$

The negative sign in the equation indicates an inversion of the output signal with respect to the input as it is 180° out of phase.
This is due to the feedback being negative in value.

Non Inverting Amplifier



- virtual earth node, the resistors, Rf and R2 form a simple potential divider network across the non-inverting amplifier
- voltage gain of the circuit can be determined by the ratios of R2 and Rf

$$V_1 = \frac{R_2}{R_2 + R_F} \times V_{OUT}$$

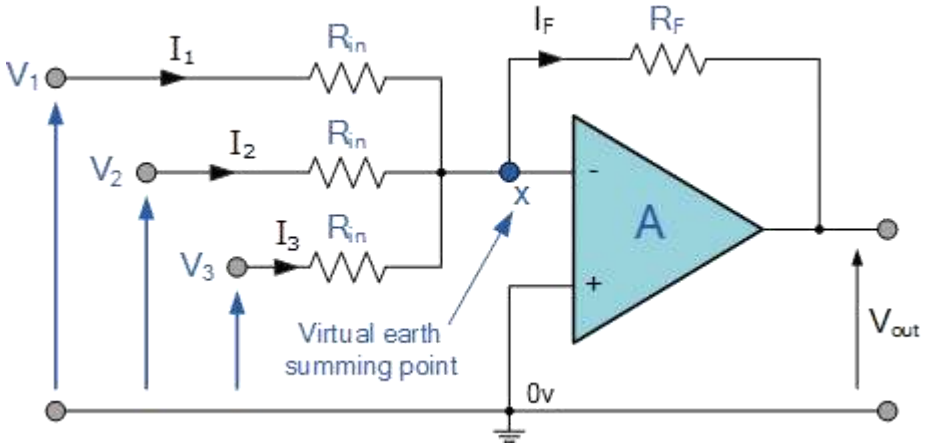
Ideal Summing Point: $V_1 = V_{IN}$

Voltage Gain, $A_{(V)}$ is equal to: $\frac{V_{OUT}}{V_{IN}}$

Then, $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2 + R_F}{R_2}$

Transpose to give: $A_{(V)} = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_F}{R_2}$

Op-Amp Application- Summing Amplifier



used to combine the voltages present on two or more inputs into a single output voltage.

$$I_F = I_1 + I_2 + I_3 = -\left[\frac{V1}{Rin} + \frac{V2}{Rin} + \frac{V3}{Rin}\right]$$

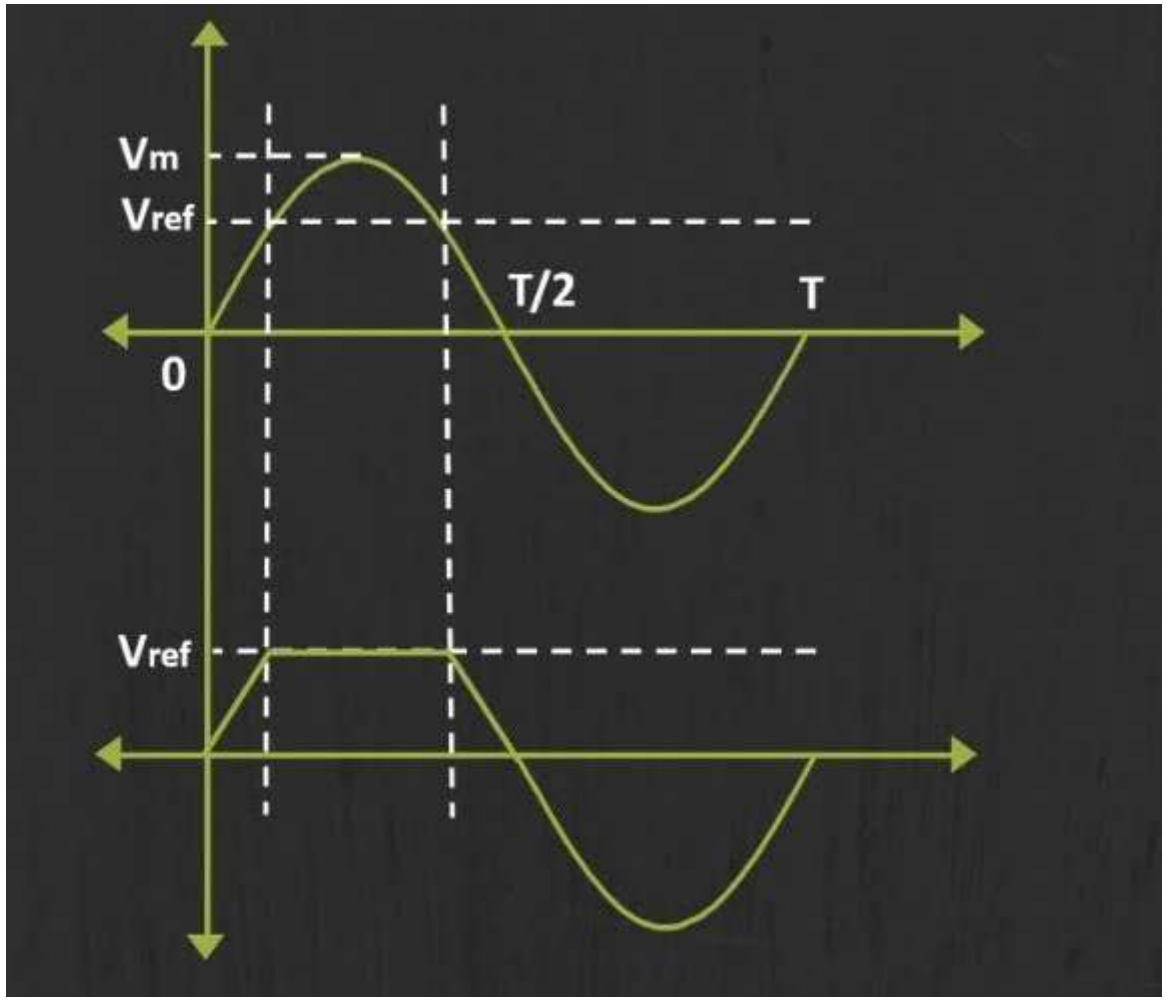
$$\text{Inverting Equation: } Vout = -\frac{Rf}{Rin} \times Vin$$

the output voltage, (Vout) now becomes proportional to the sum of the input voltages, V_1, V_2, V_3, etc.
the original equation for the inverting amplifier can be modified as:

$$\text{then, } -Vout = \left[\frac{R_F}{Rin}V1 + \frac{R_F}{Rin}V2 + \frac{R_F}{Rin}V3\right]$$

$$-Vout = \frac{R_F}{R_{IN}}\left(V1 + V2 + V3 \ldots . etc\right)$$

Op-Amp Application-



Op-Amp Application-Clipper

Wave shaping circuits are the electronic circuits, which produce the desired shape at the output from the applied input wave form. These circuits perform two functions –

- Attenuate the applied wave
- Alter the dc level of the applied wave.

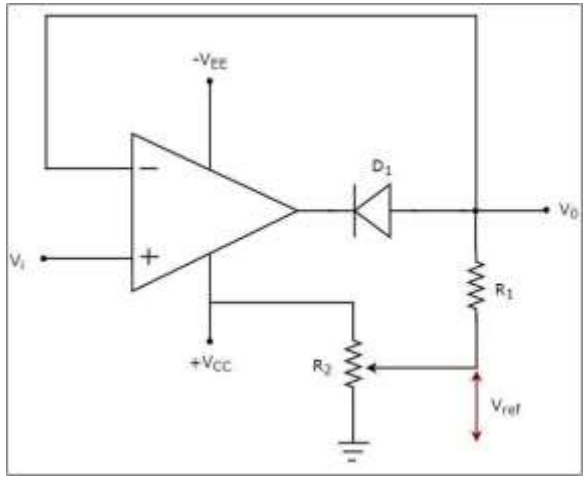
There are two types of wave shaping circuits:
Clippers and
Clampers.

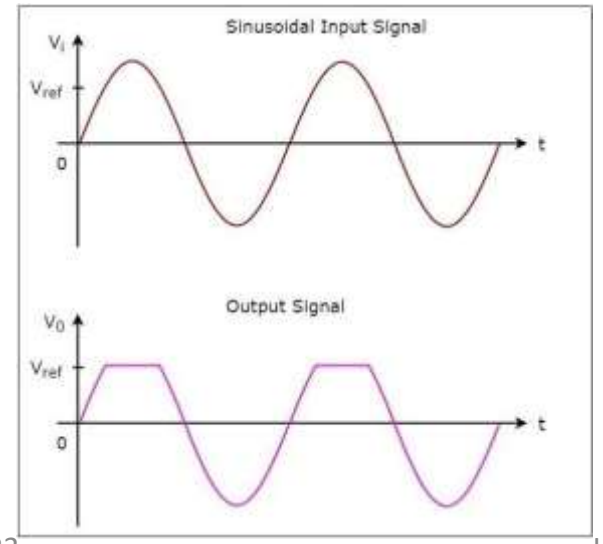
Op-Amp Application-Clipper

- an electronic circuit that produces an output by removing a part of the input above or below a reference value.
- the output of a clipper will be same as that of the input for other than the clipped part.
- The main advantage of clippers is that they eliminate the unwanted noise present in the amplitude of an ac signal.
- Clippers can be classified into the following two types based on the clipping portion of the input.
    - Positive Clipper
    - Negative Clipper

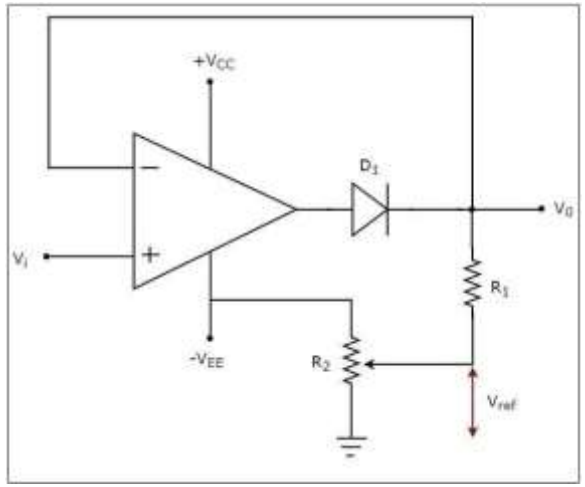
Op-Amp Application-

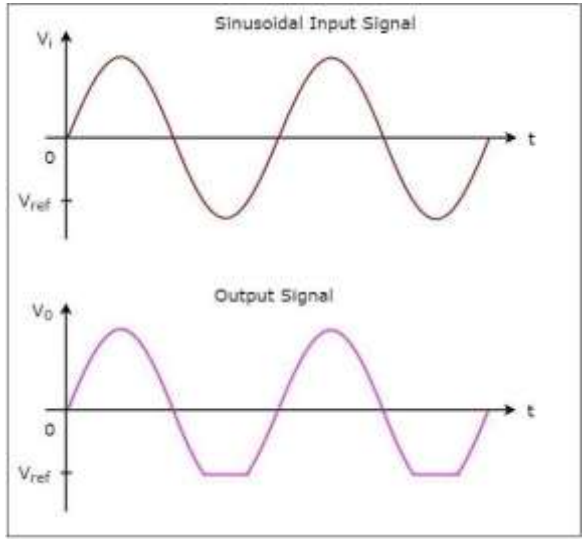
Positive Clipper





Negative Clipper





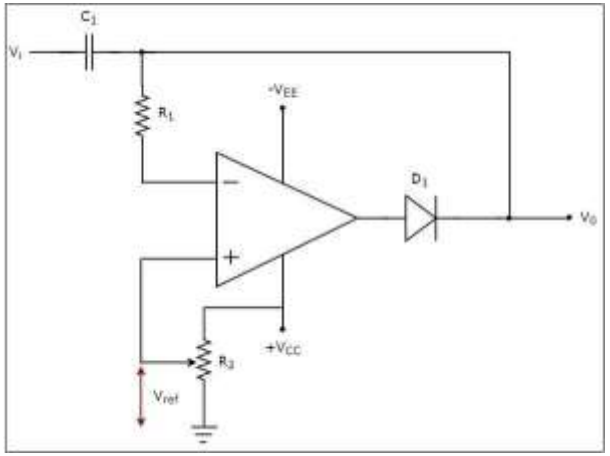
Op-Amp Application-Clampers

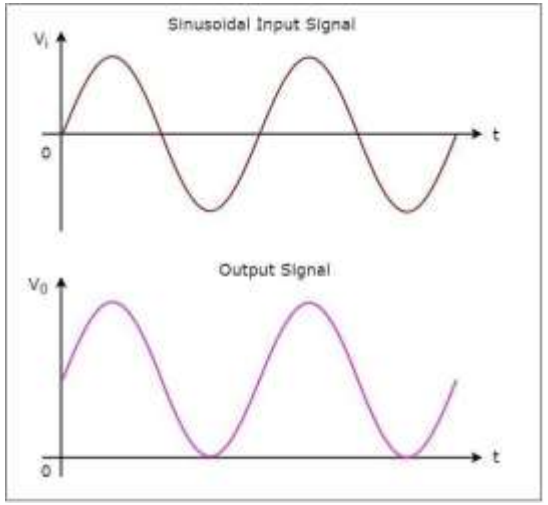
- an electronic circuit that produces an output, which is similar to the input but with a shift in the DC level.
- In other words, the output of a clamper is an exact replica of the input.
- peak to peak amplitude of the output of a clamper will be always equal to that of the input.
- Clampers are used to introduce or restore the DC level of input signal at the output.
- **two types** of op-amp based clampers
    - Positive Clamper
    - Negative Clamper

Op-Amp Application-

Positive Clamper

A positive clamper is a clamper circuit that produces an output in such a way that the input signal gets shifted vertically by a positive DC value.

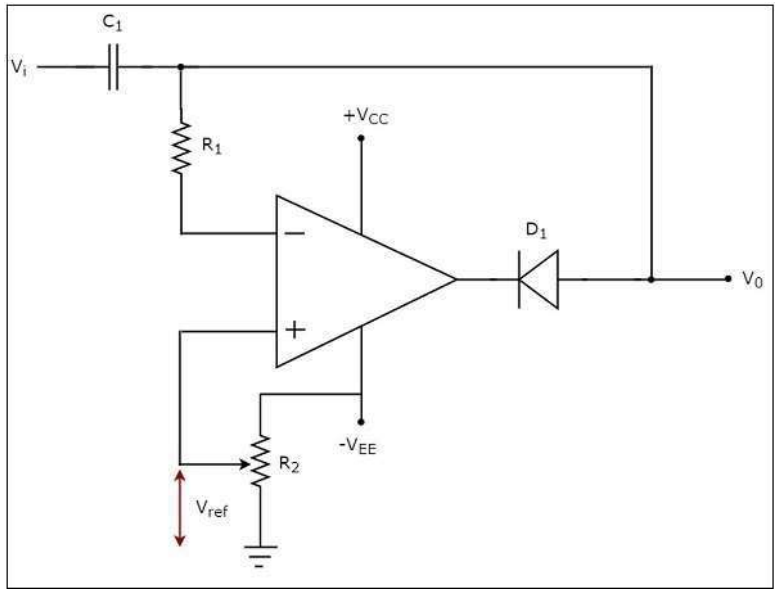


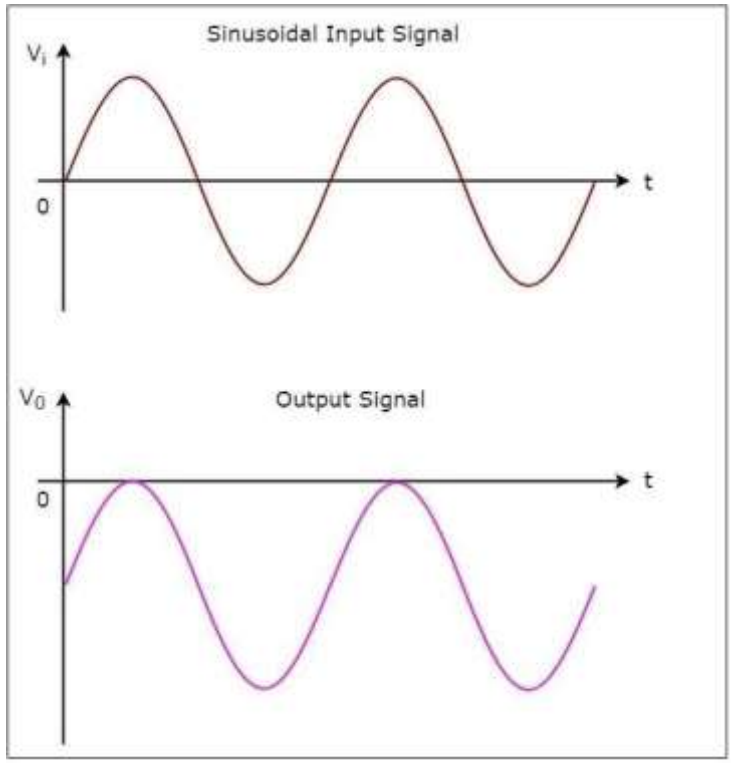


Op-Amp Application-

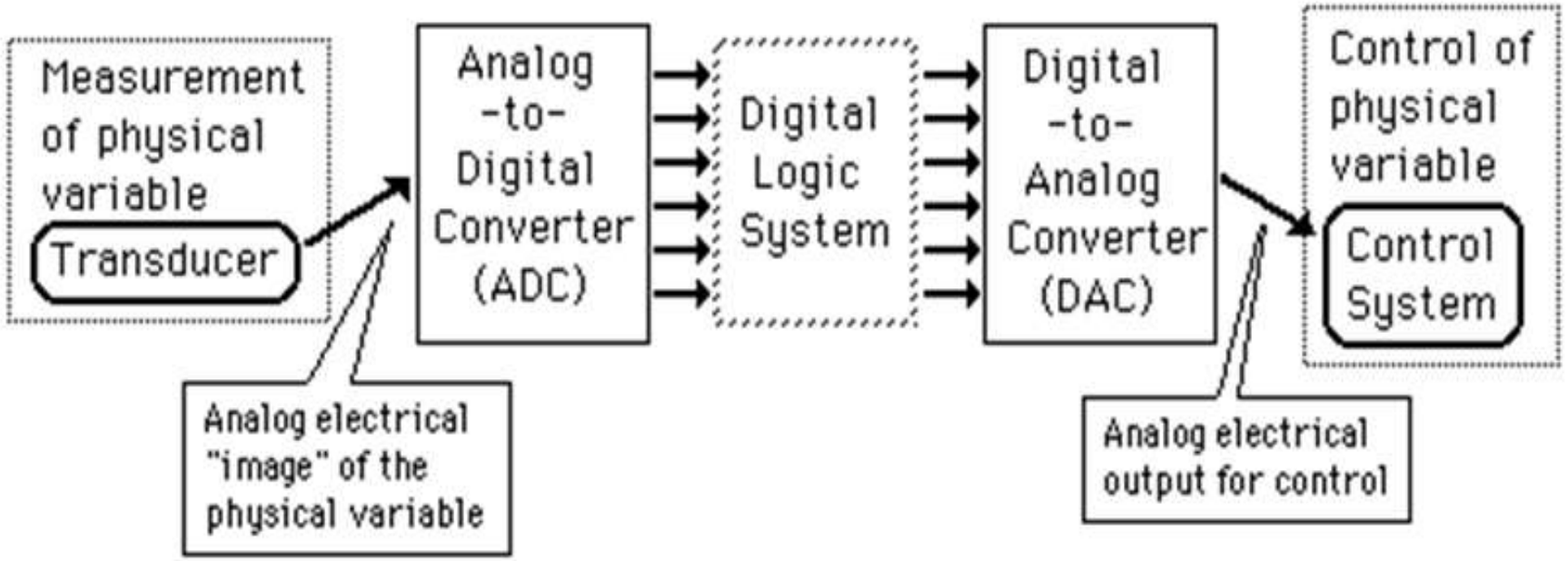
Negative Clamper

A **negative clamper** is a clamper circuit that produces an output in such a way that the input signal gets shifted vertically by a negative DC value.





A/Digital and D/A Converter

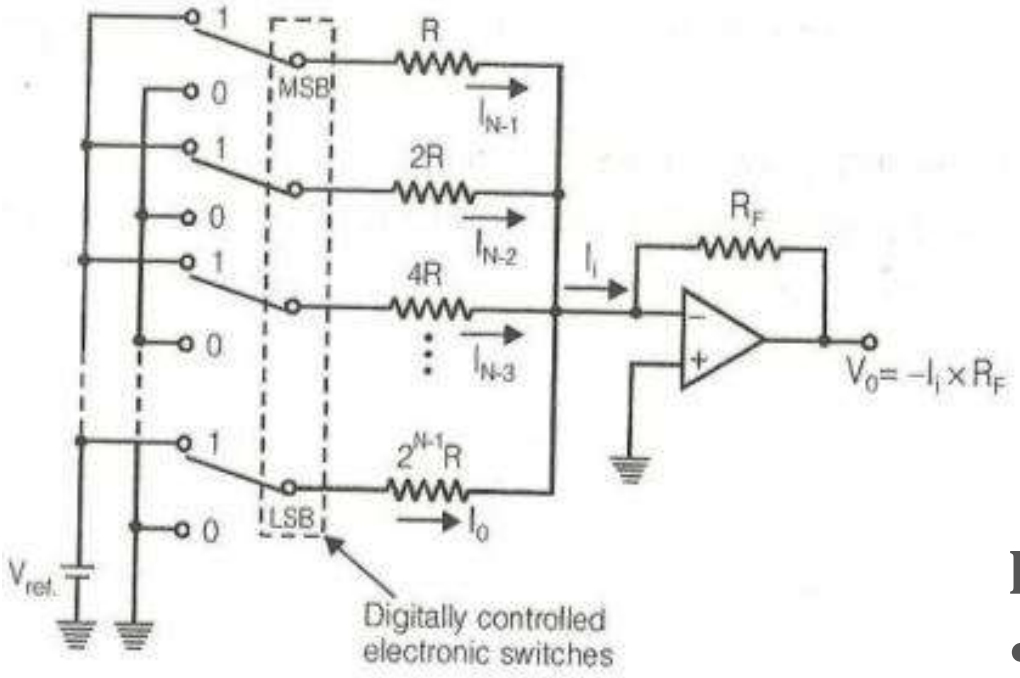


D/A Converter

There are two methods to convert digital to analog

- Weighted Summing Amplifier
- R-2R Network Approach

Weighted Summing Amplifiers



Weighted Resistor DAC

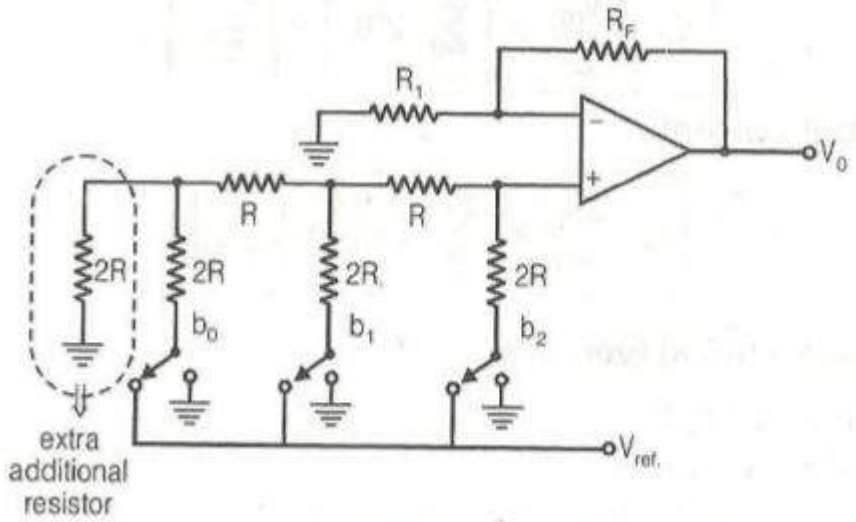
Advantages:

- It is Simple in Construction.
- It provides fast conversion.

Disadvantages:

- requires large range of resistors with necessary high precision for low resistors.
- Can be expensive.
- Hence resolution is limited to 8-bit size.

R-2R Network



R-2R non-inverting Ladder DAC

Disadvantages:

- It has slower conversion rate.

For N bit DAC:

- Number of different levels = 2^N
- Number of Steps = $2^N - 1$

Resolution or step size of DAC = Analog output/Number of steps = Va/($2^N - 1$)

% Resolution = (Step Size/Full scale output) x 100 %

$$V_{out} = \frac{R_f}{R} V_{ref} \left[\frac{D_0}{16} + \frac{D_1}{8} + \frac{D_2}{4} + \frac{D_3}{2} \right]$$

Advantages:

- Only two resistor values are used in R-2R ladder type.
- It does not need as precision resistors as Binary weighted DACs.
- It is cheap and easy to manufacture.

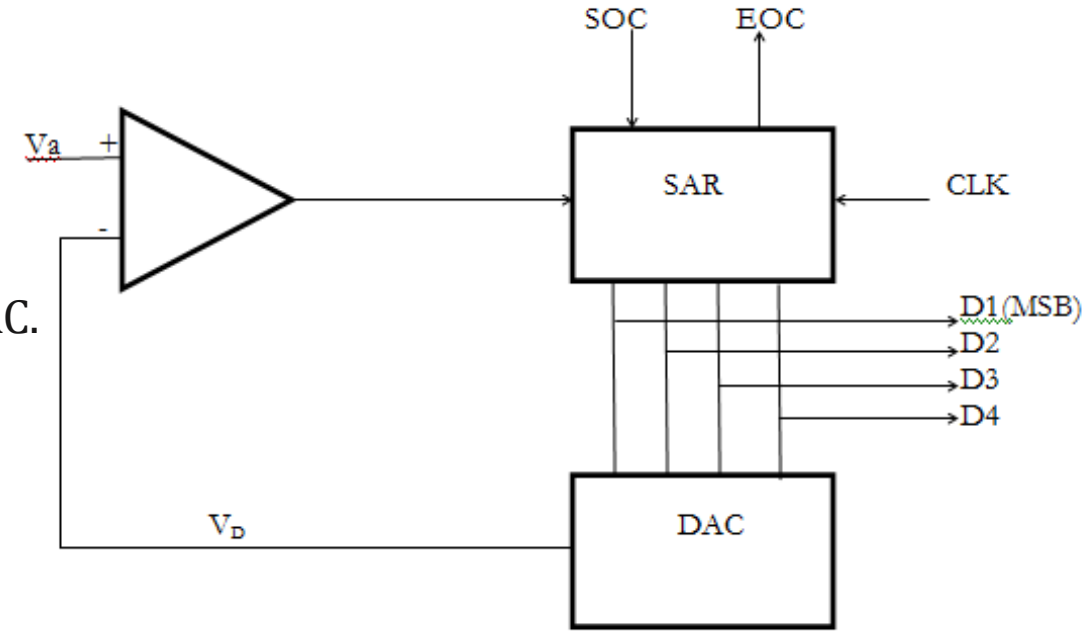
A/D Conversion

There are three types of analog to digital conversions

- Digital-Ramp ADC
- Successive Approximation ADC
- Flash ADC

SAR ADC

- (SAR), DAC and comparator.
- The output of SAR is given to n-bit DAC.



- The equivalent analog output voltage of DAC, VD is applied to the non-inverting input of the comparator.
- The second input to the comparator is the unknown analog input voltage VA.
- The output of the comparator is used to activate the successive approximation logic of SAR.
- When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.

SAR ADC

- most widely used and popular ADC
- conversion time is maintained constant and is proportional to the number of bits in the digital output
- unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB.
- operates by successively dividing the voltage range by half,

- The MSB is initially set to 1 with the remaining three bits set as 000.
- The digital equivalent voltage is compared with the unknown analog input voltage.
- If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1.
- Otherwise, the MSB is set to 0 and the second MSB is set to 1.
- Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

SAR ADC

- Let us assume that the 4-bit ADC is used and the analog input voltage is

VA = 11 V.
when the conversion starts, the MSB bit is set to 1.
Now VA = 11V > VD = 8V = [1000]2
the MSB is retained as 1 and the next MSB bit is set to 1 as follows
VD = 12V = [1100]2
Now VA = 11V < VD = 12V = [1100]2
Here now, the unknown analog input voltage VA is lower than the equivalent digital voltage VD. the second MSB is set to 0 and next MSB set to 1 as
VD = 10V = [1010]2
Now again VA = 11V > VD = 10V = [1010]2
VA>VD, hence the third MSB is retained to 1 and the last bit is set to 1.
The new code word is
VD = 11V = [1011]2
Now finally VA = VD , and the conversion stops.

SAR ADC

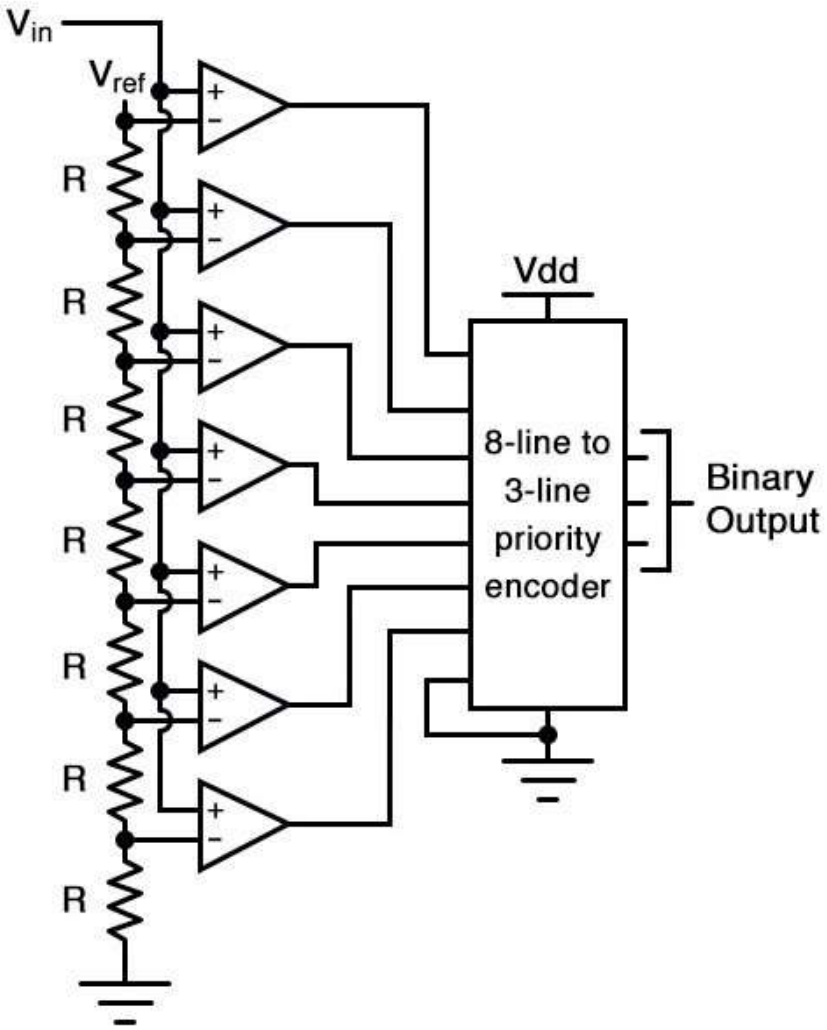
Advantages:

1 Conversion time is very small.
2 Conversion time is constant and independent of the amplitude of the analog input signal VA.

Disadvantages:

1 Circuit is complex.
2 The conversion time is more compared to flash type ADC.

FLASH ADC



- Also called the *parallel* A/D converter,
- simplest to understand.
- formed of a series of comparators, each one comparing the input signal to a unique reference voltage.
- The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output.
- The following illustration shows a 3-bit flash ADC circuit:

FLASH ADC

- V_{ref} is a stable reference voltage provided by a precision voltage regulator as part of the converter circuit, not shown in the schematic.
- As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state.
- The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

FLASH ADC

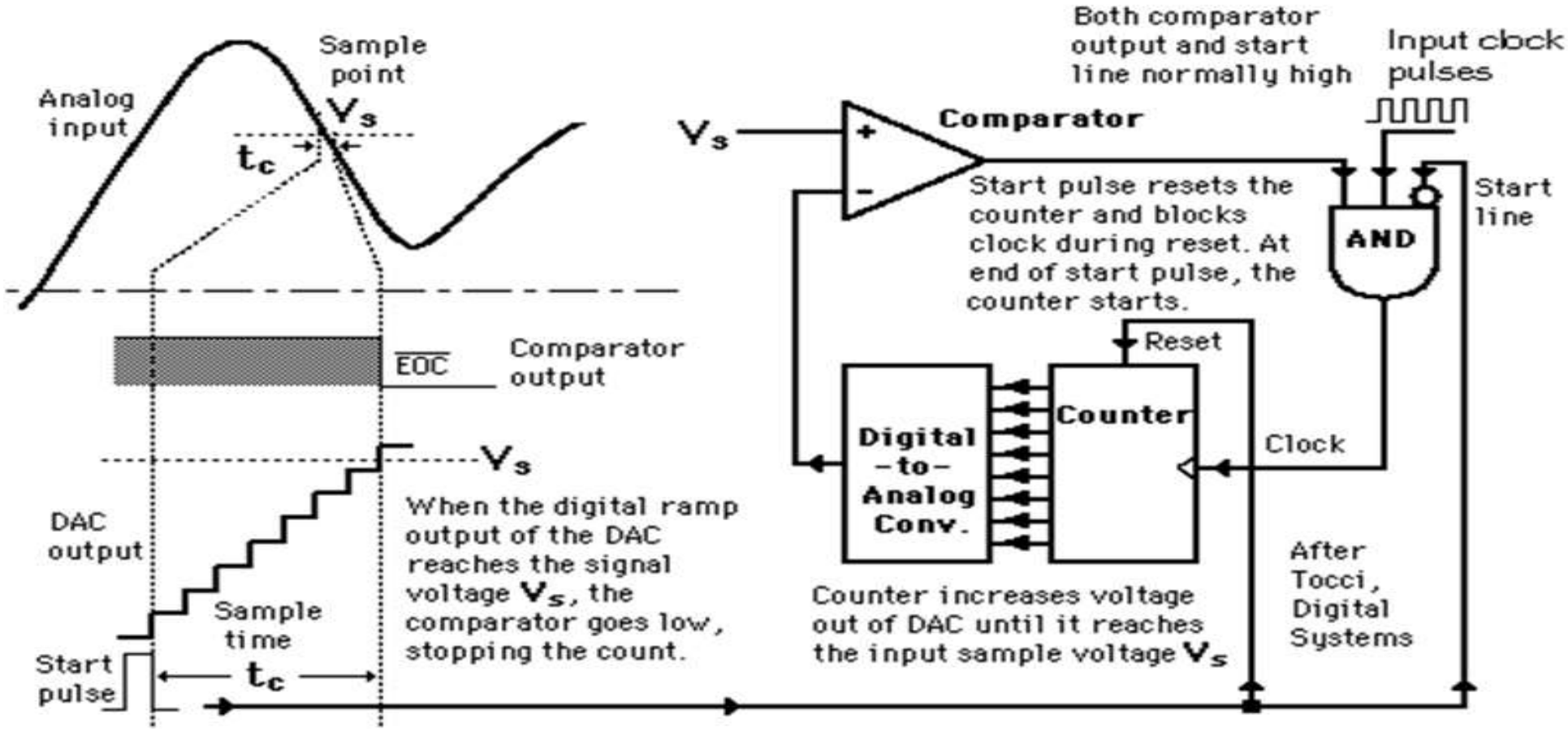
Advantages:

- Very Fast .
- Very simple operational theory .
- Speed is only limited by gate and comparator propagation delay .

Disadvantages:

- Expensive.
- Each additional bit of resolution requires twice the comparators.
- Prone to produce glitches in the output

Digital Ramp ADC



stairstep-ramp, or simply counter A/D converter

Digital Ramp ADC

- As the counter counts up with each clock pulse, the DAC outputs a slightly higher (more positive) voltage.
- This voltage is compared against the input voltage by the comparator.
- If the input voltage is greater than the DAC output, the comparator's output will be high and the counter will continue counting normally.
- Eventually, though, the DAC output will exceed the input voltage, causing the comparator's output to go low.
- This will cause two things to happen:
- first, the high-to-low transition of the comparator's output will cause the shift register to "load" whatever binary count is being output by the counter, thus updating the ADC circuit's output;
- secondly, the counter will receive a low signal on the active-low LOAD input, causing it to reset to 00000000 on the next clock pulse.

THANK YOU