

1) Prove the Boolean theorems: (a)  $x + x = x$  (b)  $x + xy = x$

Proof:

a)  $x + x = x$

LHS:  $x + x = (x + x) \cdot 1$  postulate 2(b)

$= (x + x) \cdot (x + x')$  5(a)

$= x + xx'$  4(b)

$= x + 0$  5(b)

$= x$  2(a)

b)  $x + xy = x$

LHS:  $x + xy = (x + 1) \cdot xy$  postulate 2(b)

$= x(1 + y)$  4(a)

$= x(y + 1)$  3(b)

$= x \cdot 1$  2(b)

$= x$  2(a)

2) Define – Noise-margin

Noise Margin is defined as the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts

3) State De-Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra.

They are:

i. The complement of a product is equal to the sum of the complements.

$$(AB)' = A' + B'$$

ii. The complement of a sum term is equal to the product of the complements.

$$(A + B)' = A'B'$$

4) What are don't care terms?

Minterms that have unspecified outputs for some input combinations are called don't care terms.

We denote them by variable 'x' or 'd'.

5) Apply De Morgan's theorem for the function  $(A + B + CD)'$ .

$$F = ((A+B+CD)D)'$$

$$= (A+B+C)' + D'$$

$$= A' \cdot B' \cdot C' + D'$$

6) State the two canonical forms of Boolean algebra.

The two canonical forms of Boolean algebra are:

i. Sum of products

ii. Products of Sum

7) Simplify:  $(X + X'Y)$

$$Z = X + X'Y = X + XY + X'Y \quad \text{since } X + XY = X$$

$$Z = X + Y(X + X') \quad \text{since } X + X' = 1$$

$$Z = X + Y$$

8) What is the complement of  $(A + BC + AB)$ ?

$$F = (A + BC + AB)$$

$$F' = (A + BC + AB)'$$

$$= A' \cdot (BC)'. (AB)'$$

$$= A' \cdot (B' + C') \cdot (A' + B')$$

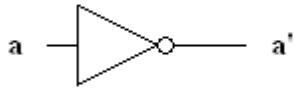
9) Prove that a bubbled input AND gate, functions like a NOR gate. [A/M – 04]

Truth Table for NOR Gate and bubbled input AND gate

A	A'	B	B'	A+B	$Y = (A+B)'$ (NOR Gate)	$Y = (A' \cdot B')$ (Bubbled input AND gate)
0	1	0	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0

10) How is NAND gate used as an inverter?

Logic Diagram for Inverter



The two input terminals of the NAND gate will be shorted and given as single input.



Now the above NAND gate act as a inverter